

Spectral estimation for long-term evolution transceivers using low-complex filter banks

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Abstract: For mobile user equipments (UEs), a careful power management is essential. Despite this fact, quite an amount of energy is wasted in today's UEs' analogue (AFEs) and digital frontends (DFEs). These are engineered for extracting the wanted signal from a spectral environment defined in the corresponding communication standards with their extremely tough requirements. These requirements define a worst-case scenario still ensuring reliable communication. In a typical receiving process the actual requirements can be considered as less critical. Knowledge about the actual environmental spectral conditions allows to reconfigure both frontends to the actual needs and to save energy. In this paper, the authors present a highly efficient generic spectrum sensing approach, which allows to collect information about the actual spectral environment of an UE. This information can be used to reconfigure both the AFE and DFE, thus endowing them with increased intelligence. A low-complex multiplier free filter bank extended by an efficient power calculation unit will be introduced. They also present simulation results, which illustrate the performance of the spectrum sensing approach and a complexity comparison with different well-known implementations is given. Furthermore, estimates on the chip area and power consumption based on a 65 nm CMOS technology database are provided, considering the Smarti4G chip as a reference.

1 Introduction

In the recent years, research on cognitive radio (CR) has gained great interest. The concept of CR, for example, described in [1], allows the user equipment (UE) to scan its relevant environment with respect to the instantaneous spectrum allocation. In the original context of CR, this information is used for efficient spectrum usage by different UEs using various radio access technologies. However, knowledge about the environmental spectral composition can also be extremely valuable for the operation of the receive path of an UE [2–5]. The main idea is as follows: if the UE detects many interferences, then both the analogue (AFEs) and digital frontends (DFEs) of the receive path have to provide full performance, for example, highly linear amplifiers, filters of high order etc. In the remainder of this paper these interferences will be called blockers. Full performance of the AFE and DFE results in high energy consumption of the UE. If, on the other hand, there are only few blockers present, which additionally contain little energy, the receive path does not have to run in full performance mode, resulting in power saving. An extensive discussion of worst case against realistic blocker allocations around an UE has already been given in [6–8] and will therefore not be part of this paper. A concept handling the spectrum sensing task for the universal mobile telecommunications system (UMTS) test case has been described in [9, 10], whereas different implementation approaches for the long-term evolution (LTE) test case have been given in [11, 12]. These approaches have been designed and optimised to fulfil the very specific blocker allocation given in the 3GPP specification [13]. In this paper, we present an efficient generic spectrum sensing approach, which is not limited to a specific communication standard. The approach is based on a dyadic tree-structured filter chain in combination with a low-complex power calculation unit (PCU). The filter chain itself has been introduced in [14], whereas the idea of the extension by the efficient PCU is further developed in this paper.

This paper is structured as follows. Section 2 describes the implementation of an example filter chain for blocker detection. We give an overview on the basic filter properties, filter design criteria,

a complexity estimation and a comparative discussion with well-known estimation methods. A method for optimising the design process is given in [15], using [16–24]. Section 3 introduces an efficient method for calculating the power of each of the individual filter outputs, the PCU. Section 4 provides information about the chip area and power consumption of the blocker detection unit (BDU) methods introduced in [11, 14]. Finally, Section 5 shows simulation results for the given filter bank approach, demonstrating the detection performance of the generic spectrum sensing approach for different blocker power levels. The section contains simulation results including a comparison of the power calculation methods discussed before. Furthermore, a performance analysis for bit true simulations of the proposed approaches is given.

2 DFE-based BDU

A method, which allows to gain information about the spectral environment of an UE, is desired. This information can be used to reconfigure the AFE and DFE of the receive path. The focus of this paper is on the development of a power and area efficient approach. In any case, the BDU must consume less power than the power saved by the reconfigured AFE and DFE.

2.1 Basic properties of the BDU

The method we use is a tree-structured subband processing technique. Subband transforms have first been introduced in the 1970s by Croiser *et al.* in [25, 26], and have been further developed in the 1980s by Smith and Barnwell [27], Grenet [28], Mintzer [29], Vetterli [30] and Vaidyanathan [31–34]. An overview of the main contributions of those authors can be found in [35, 36]. The used tree-structured technique has a very close relationship to the wavelet transform (WT). More particularly, the discrete WT can be interpreted as a dyadic tree-structured subband transform. Therefore such structures are usually referred to as wavelet-based schemes [35, 37]. The basic idea and also a method for estimating the complexity in such a system has already been given in [6, 11, 12, 38, 39] for a less general approach.

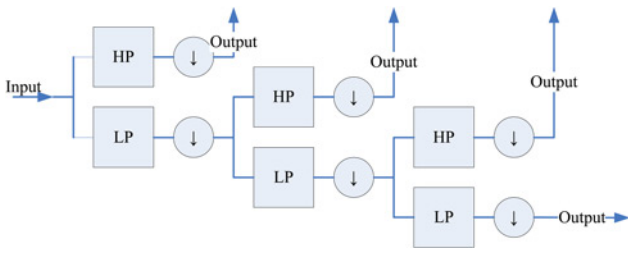


Fig. 1 Block diagram of the dyadic filter chain approach

Fig. 1 illustrates the initial concept of the approach we use in this paper. As can be seen, the filter chain consists only of high-pass (HP) filters, low-pass (LP) filters and downsampling units. A specialised class of infinite impulse response (IIR) filters is used in the actual system, which can be implemented in hardware very efficiently [40, 41]. Furthermore, these filters can provide LP and HP functionality at the same time with almost no additional cost. In this concept, downsampling is crucial. The basic idea relies on two facts:

- (1) Downsampling decreases system complexity because of the lower sampling rate after each stage (for both LP and HP output).
- (2) Subsampling the HP output allows to fold the spectral part located there towards DC.

As a consequence of the dyadic structure, where downsampling by a factor of two after each filter stage is destined, each of the filters need to have a cutoff frequency of $f_s/4$, with f_s the sampling frequency of the signal. This fact allows to use half band filters with decreased complexity, legitimating the complexity reduced design of the chosen filters. The downsampling process results also in a reduced sampling frequency for the next filter stage, which coincides with lower energy consumption after each stage compared with the earlier one. The achieved frequency resolution is logarithmic towards higher frequencies. To achieve linear resolution the

filter chain has to be extended as shown in Fig. 2, whereas only the first three filter stages are shown. In the final system described in this paper seven stages are present, resulting in $2^7 = 128$ outputs.

2.2 Complexity estimation of the filter chain

As can be seen from the LP/HP filter structure of the approach shown in Fig. 2, the one-sided spectrum of the real input signal is divided into 2^N sections. With $N=7$, the number of filter stages used in the actual system leads to 128 subbands. Each of the outputs provides a time domain signal containing only distinct portions of the original spectrum. $P_j = (1/K) \sum_k |x_j[k]|^2$, where $x_j[k]$ is the j th output signal, corresponds to the power of the j th subband. As only the relative power of the j th subband w.r.t. the first subband is of interest, and also all filter outputs are of the same length, the factor $1/K$ can be neglected as discussed again later in this paper. Considering all outputs in the described manner, the system builds up a spectrum estimator with 256 points in frequency domain, as each of the filter outputs contains both the positive and negative frequency parts in a spectral analysis. Note, that we assume real input signals. In [14] it has been shown that this assumption can be considered being valid.

For an efficient implementation, filters of extremely low complexity are needed. A special class of IIR filters has been chosen to implement each of the filter blocks shown in Fig. 2. The basic structure of those filters can be seen in Fig. 3. A performance comparison of these filters with other filter types is given in [15].

Neglecting the shift and delay elements, each filter block consists of 37 real adders only, while no multipliers are needed. This is the case, as the binary pattern representation of each of the coefficients is sparse. Here sparse means, that the number of ones in the representation is very low compared with the zeros. In the final stage, 64 of these blocks are present. As shown in [38] because of continuous downsampling after each stage, those filters have the same relative complexity w.r.t. the number of needed operations in a certain time-window like the one in the first stage. The complexity therefore results to $C_{\text{output}} = 37ND/2 = 16\,576$ real additions per output

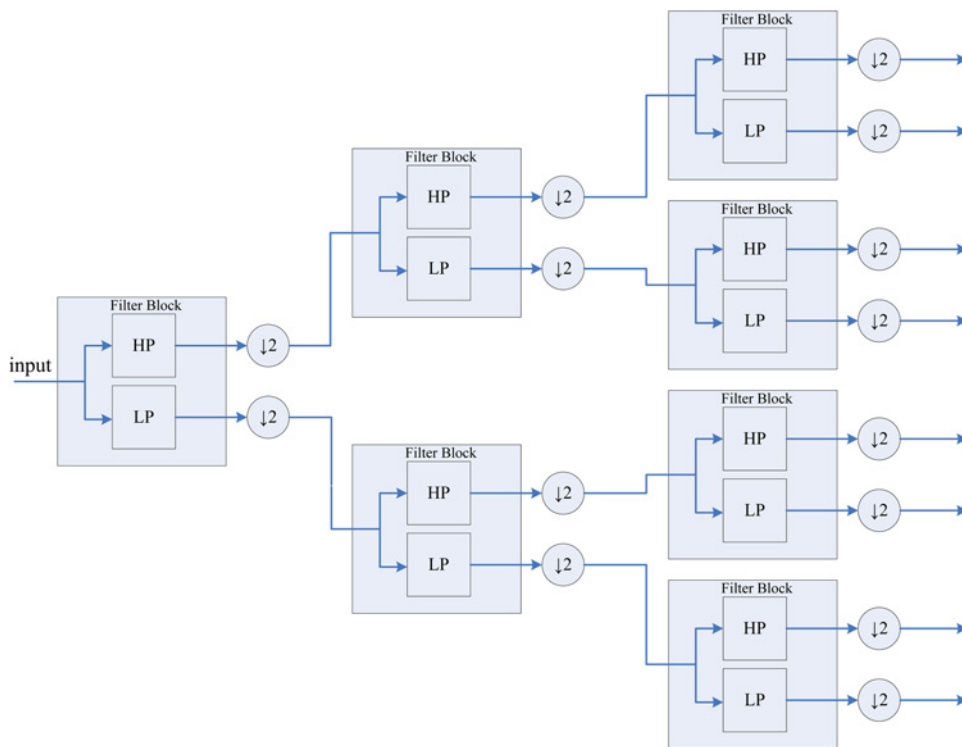
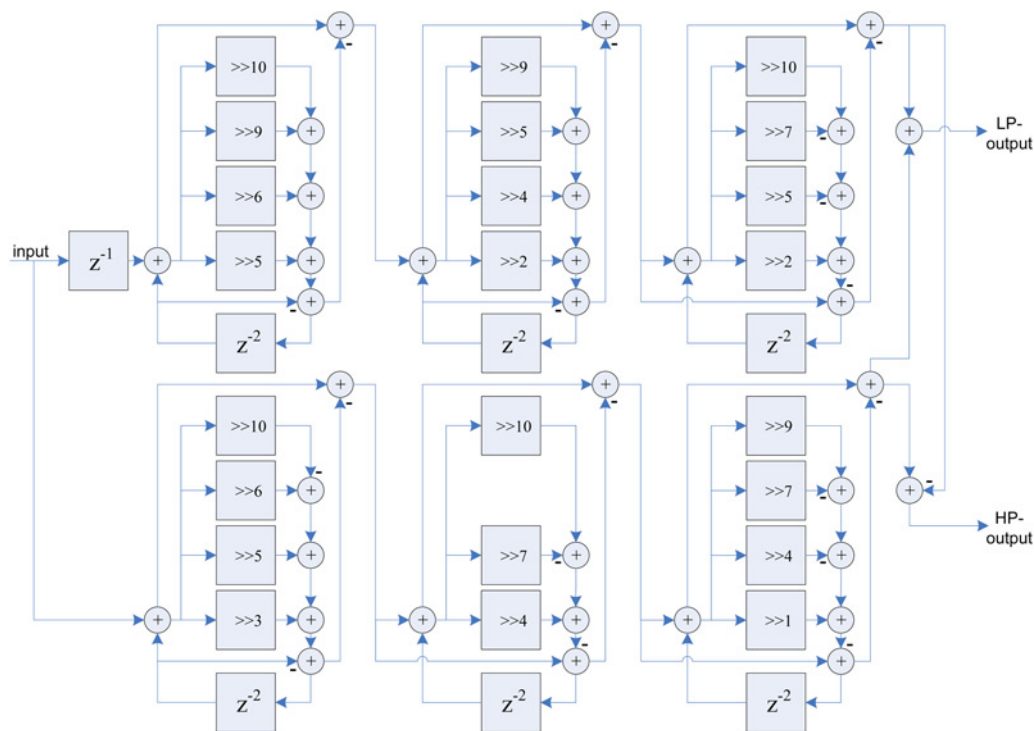


Fig. 2 Block diagram of the modified dyadic filter chain approach



sampling interval, with $N=7$ the number of stages and $D=2^N$ the overall downsampling factor. Additionally, as can be seen from Fig. 3, the whole structure can be implemented using a polyphase decomposition, as the upper and lower branches of the filter can be written as a function of z^2 , yielding in an additional reduction in complexity. The same frequency resolution can be achieved by a 256-point-fast-Fourier-transformation (FFT) implementation, as positive and negative frequencies need to be considered. However, this approach would need $2^N \log_2 2^{N+1} = 1024$ complex multiplications and $2^{N+1} \log_2 2^{N+1} = 2048$ complex additions per output sampling interval. From the illustration in Fig. 4, adopted from [42], it can be seen, that for bit widths used in real systems the filter bank-based approach is less complex compared with the FFT-based approach, even if a coordinate rotation digital computer (CORDIC) implementation is used. The unroll factor UF refers to the maximum number of micro rotations using the

CORDIC. For both concepts, a unit calculating a power estimate of the signal has to be added. In the case of the FFT-based approach for this purpose, the Welch method with zero overlap is assumed, which is for example described in [43]. Estimating the power from averaging a number of periodograms can be considered as equally complex as calculating P_i from the results of the filter bank-based approach. For this reason for a complexity comparison of both approaches, only one FFT operation and the number of operations needed for one output sample in each frequency section of the filter bank-based approach is relevant.

2.3 Comparison to other non-parametric estimation methods

Several other spectrum sensing approaches can be derived, like the Goertzel algorithm, for example, described in [44, 45] or the chirp-z-transform, for example, described in [46–53]. Both of the approaches are only interesting in applications, where just a very limited number of spectral components are needed or a zoom into a specific part of the spectrum is desired. However, both approaches are getting more complex than a classic FFT, if the number of spectral components to be calculated exceeds $\log_2 K$, where K is the length of the FFT. As our approach is even less complex than the FFT-based approach, it outperforms both methods for our application.

Another issue to be treated is the time-frequency resolution, for example, important in time division multiple access systems. A classic FFT does not provide any information about the timely occurrence of a blocker in a certain FFT window. If information about the time is needed, the short time-window FFT (SFFT), for example, described in [54–56] can be used. However, the SFFT does not provide decreased complexity compared with the FFT and additionally the DWT, which our system is based on, provides better properties covering this issue. Therefore also the SFFT can be outperformed by our approach.

A third issue to cover is the latency of the output signal. Using an FFT, each new FFT window has to be calculated on a blockwise basis. If rapidly an update of the instantaneous estimate is desired, then many overlapping windows would have to be

Table 1 Complexity estimation for the DFT and its sliding derivatives

Algorithms		Single $S_n[k]$ computation		Next $S_n[k+g]$ computation	
	Input	Real mults	Real adds	Real mults	Real adds
DFT	compl.	$2 \cdot 2KM$	$2 \cdot 2KM$	$2 \cdot 2KM$	$2 \cdot 2KM$
	real	$2KM$	$2KM$	$2KM$	$2KM$
standard Goertzel	compl.	$M(2K+4)$	$M(4K+4)$	$M(2K+4)$	$M(4K+4)$
	real	$M(K+2)$	$M(2K+1)$	$M(K+2)$	$M(2K+1)$
sliding DFT	compl.	$4KM$	$2K+4KM$	$4Mg$	$(2+4M)g$
	real	$4KM$	$K+3KM$	$4Mg$	$(1+3M)g$
sliding Goertzel	compl.	$M(4K+4)$	$2K+M(6K+4)$	$8Mg$	$(2+10M)g$
	real	$M(K+2)$	$K+2KM+M$	$3Mg$	$(1+3M)g$

calculated. Solving this problem at less complexity is provided by the sliding discrete Fourier transform (DFT) or the sliding Goertzel, for example, described in [57–59]. However, the same method can be used for our approach by implementing a moving average summation over the output samples. Therefore, also those methods do not possess any advantage compared with our method, as long as the calculation of one output sample per final filter stage is less complex than the FFT-based approach.

Table 1 provides a complexity comparison of the DFT, the Goertzel algorithm, the sliding DFT and the sliding Goertzel. K denotes the length of the underlying data block, which is equal to the length of the DFT, M denotes the number of spectral estimates to be calculated, $S_n[k]$, $S_n[k+g]$ are the n th frequency component at time instances k , $k+g$. g defines the gap between the first sample to be investigated and the next one. Owing to the structure of the sliding algorithms, the complexity for one individual sample increases, if the gap g increases. The reason is that all intermediate samples have to be calculated, even if those are not used.

A general discussion analysing the pros and cons of other energy detection-based spectrum sensing approaches used in today's communication systems has already been given in [60] and is therefore skipped here.

3 PSD estimate calculation

To finally achieve a power spectral density (PSD) estimate, the power of the output signals at each final filter stage has to be calculated. According to the Parseval Theorem [61], given by

$$\sum_{n=0}^{N-1} |x[n]|^2 = \frac{1}{N} \sum_{k=0}^{N-1} |X[k]|^2 \quad (1)$$

for a discrete signal, the power can either be calculated in the time or in the frequency domain. In (1) $X[k]$ is the DFT of $x[n]$, both with an interval length of N samples.

3.1 Low-complex PSD estimation method

Each of the output signals contains spectral parts from a certain subband of the original signal. Calculating the power of each of the output signals therefore allows to derive estimates for the PSD in each part of the spectrum of the original signal. We perform this task in the time domain. The power P_j of the j th subband is given by

$$P_j = \sum_{n=0}^{N-1} |x_j[n]|^2, \quad \forall j \quad (2)$$

whereas the normalisation by $1/N$ can be neglected for the investigated application, as the number of samples for all subbands is the

same. As extensively discussed in [62] it can be shown that there exists a less complex method for the given architecture to fulfil the same task. The main idea is to calculate the power P_0 for the first subband using (2) only, and to use a different approach for all the other subbands using

$$Q_j = \left(\sum_{n=0}^{N-1} |x_j[n]| \right)^2 \quad (3)$$

instead. The advantage of calculating Q_j is that this method is by far less complex compared with the one used in (2), as only one instead of N multiplications in each frequency range has to be performed. Remember, that we assume real output signals from the filter stages. Certainly, in general $Q_j \neq P_j$ and Q_j itself does not provide a valid value for a power estimator. However, in [62] it has been shown that using our approach and assuming a flat spectrum in each individual subband we have

$$\frac{Q_j}{Q_0} = \frac{P_j}{P_0} \quad (4)$$

The simulation results given in Section 5 confirm that the assumption of a flat spectrum makes sense. Therefore if the relation Q_j/Q_0 and the power estimate of the first subband P_0 are known, the power estimate of the j th subband P_j can be calculated according to

$$P_j = P_0 \frac{Q_j}{Q_0} \quad (5)$$

If the absolute power estimate of each subband is of interest, N multiplications are now only needed for the first subband to calculate P_0 . Additionally one multiplication is needed to calculate Q_0 , whereas for all other subbands two multiplications and one division have to be performed to calculate P_j . If only the relative power compared with the first subband, which could represent the wanted signal, is of interest, then P_0 is not required. Furthermore, only one multiplication instead of two is needed to calculate the relevant values for the j th subband. Although the simulation results given in Section 5 provide a numeric proof of the validity of the concept, a detailed mathematical derivation has been carried out in [62], yielding the same conclusion.

In the following section simulations are shown, which demonstrate, that the calculation according to (5) is valid for the proposed architecture for a wide range.

3.2 Simulation results for the low-complex power estimator

In Fig. 5 PSD estimates using the methods from (2) and (3) are illustrated, where

$$P_{j,\text{norm}} = \frac{P_j}{P_0} \quad (6)$$

and

$$Q_{j,\text{norm}} = \frac{Q_j}{Q_0} \quad (7)$$

The underlying data are a typical worst-case scenario for the 20 MHz test case described in the standard [13, 63] and in a more compact form in [6]. Fig. 5a shows the performance of both approaches. In Fig. 5b the difference between the two proposed approaches is shown, which can be considered as being the detection error for the approach used according to (3). It can be seen that both methods deliver the same result (w.r.t. measurement

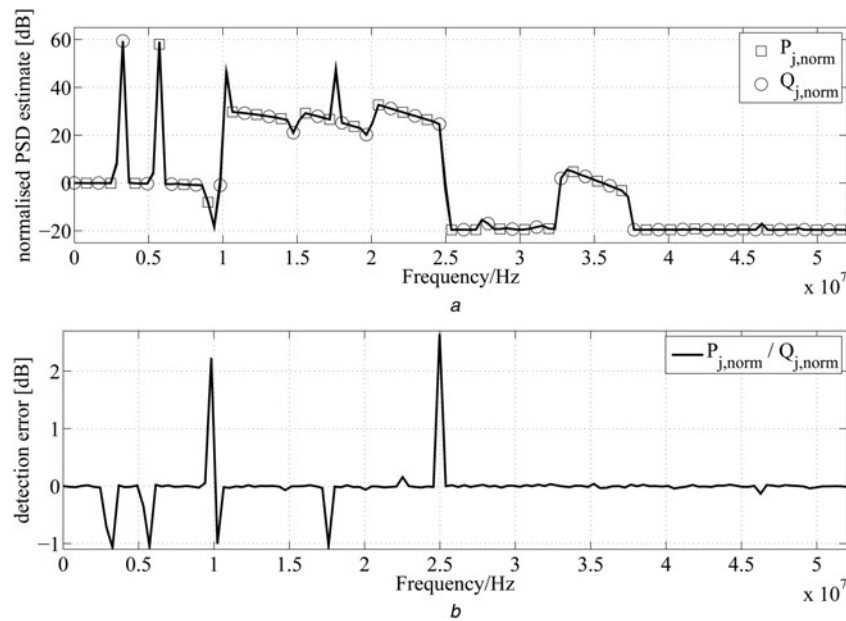


Fig. 5 Example of the detection accuracy for a given spectrum
a Comparison of both proposed approaches
b Difference of proposed approaches in dB

accuracy) for a very wide spectrum range. Only in subbands, where huge jumps in amplitude of certain frequency components are located, detection errors using the method according to (3) instead of (2) can be observed. Typical values for the detection error are at around 2 dB. For the investigated application this can be neglected, as can be seen in the simulation results given in Section 5.

4 Chip area demand and power consumption estimation

In this section, estimates of the presumed chip area demand and power consumption of the proposed systems are given. The derivations are based on the 65 nm CMOS technology description given in [64], where the values of the area requirements and power consumption of each elementary logical and combinatorial unit, for example, ‘1 bit full adder’, ‘1 bit multiplier’, ‘D-FlipFlop’, ‘AND-Gate’ and ‘Buffer’, are given. Based on this information, the overall filter structures, and the knowledge about the clock frequency of each block, chip area and power consumption estimates have been derived.

An interesting issue at this point is, how the complexity (area and power consumption) of the proposed approaches has to be rated in the context of a real Rx transceiver chip implementation. This comparison allows to conclude whether the design should be implemented or not. As a reference Intel’s SMARTi4G chip is used. The information needed for the comparison can be found in [65, 66]. Table 2 gives an overview on the percentile share of the chip area and power consumption of different approaches (‘specific against generic’ and ‘completely developed against adjacent channel and continuous wave (CW) blocker detection only’) and different bit widths. The ‘specific’ approach has been described in [11], whereas the basics of the ‘generic’ approach have been given in [14] and further developed and specified in the previous sections of this paper. In [2–4] it has been stated that in many situations the detection of the closest blockers, namely the adjacent channel and the most critical CW blocker, are of interest only. Therefore simplified versions of the filter chain being capable to detect those blockers only have been analysed for comparative reasons. The investigated area and power estimates are also given in Table 2. Depending on the desired accuracy and actual usage of the BDU, bit widths of around 12–14 bit are resonable. The

values for 32 bit have been given as a comparison, as those provide detection accuracies comparable with the aforementioned floating point implementation. For the SMARTi4G figures of merit both for the whole chip and the Rx path solely are given. The values for the Rx path only are again conservative values, as a standard receiving scenario is chosen, that is, no antenna diversity approach or similar are activated. If more sophisticated methods are used, then the power consumption rises by up to 150%.

According to empiric investigations for the SMARTiUE chip given in [4], about 50% of the overall power consumption in the Rx path can be saved, if the detection algorithm given for the UMTS case is used [2–4]. As UMTS support is also part of the SMARTi4G, and LTE functionality defines an additional feature, it can be assumed that also for the LTE-based approach 20–50% of the power consumption in the Rx path can be saved. The actual value heavily depends on the actual receiving scenario. Therefore according to the estimates given in Table 2 it can be

Table 2 Fraction of the filter banks’ power consumption and chip area requirements w.r.t. Intel’s SMARTi4G chip in % – 20 MHz test case is assumed

		S4G, %	Bits	Specific appro.		Generic appro.	
				Full, %	simpl., %	Full, %	simpl., %
power	Rx only	100	12	4.81	4.63	7.99	3.61
			16	6.17	5.95	10.40	3.61
			32	11.62	11.24	20.07	9.08
	full chip	100	12	0.46	0.44	0.76	0.34
			16	0.58	0.56	0.98	0.44
			32	1.10	1.06	1.90	1.06
area	Rx only	100	12	2.50	1.20	4.67	1.14
			16	3.20	1.54	6.06	1.48
			32	5.97	2.87	11.65	2.87
	full chip	100	12	0.82	0.39	1.52	0.37
			16	1.04	0.50	1.58	0.48
			32	1.95	0.94	3.80	0.94

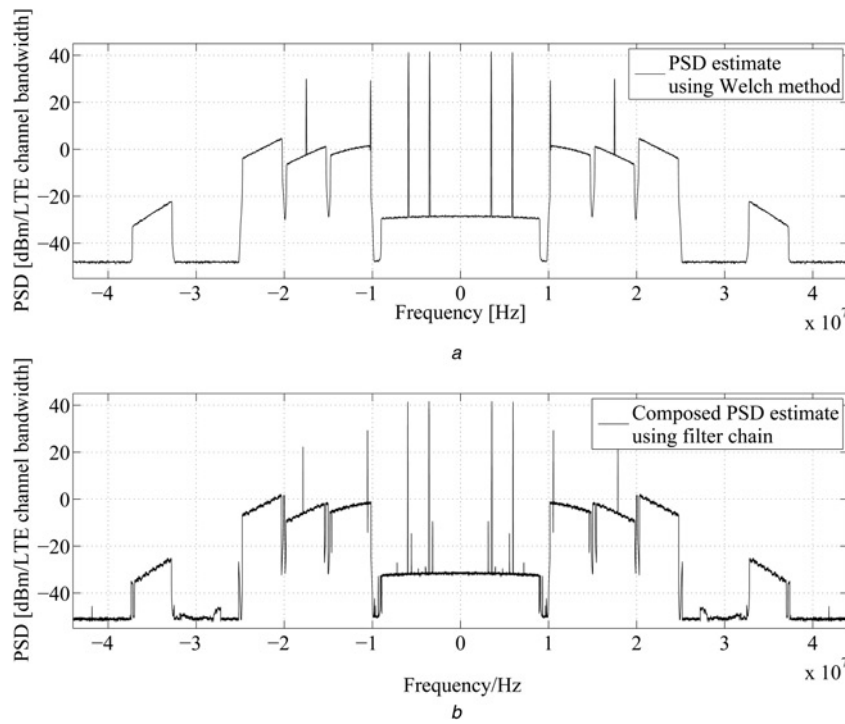


Fig. 6 Comparison of different PSD estimation approaches
a PSD estimate achieved by using the Welch method for the whole input signal
b Composed PSD estimate using the designed filter chain

concluded that the approach is worth being included in future RF transceiver chip solutions.

5 Simulation results

In this section, simulation results of the complete architecture are presented. Again, as a reference scenario the worst-case scenario for the 20 MHz test case given in the standard [13, 63] is chosen. The presentation includes results for the comparison of both methods for power calculation, as discussed in Section 3, which are summarised in Section 5.1. Here a floating point implementation of the filters is assumed. Furthermore, simulation results for different bit widths referencing the bit true implementation are given in Section 5.2.

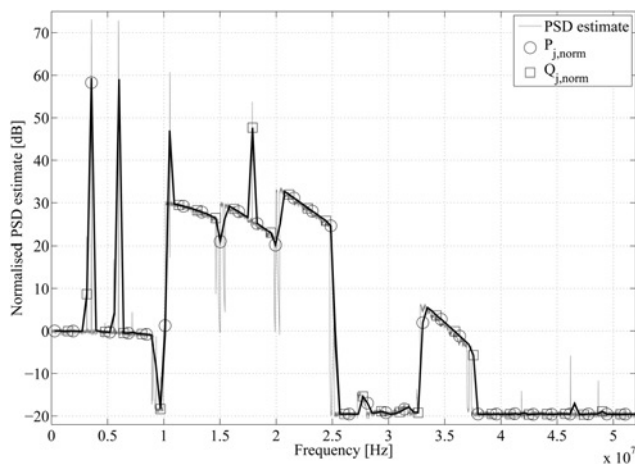


Fig. 7 PSD estimates using the proposed architecture

5.1 Floating point results comparing the different PCU methods

In Fig. 6, a comparison of different PSD estimation approaches for a certain input signal is given to validate the detection performance of the overall system later on. Fig. 6*a* shows a PSD estimate of an input signal, where the Welch method is performed over the whole signal. This curve will be taken as a reference. Fig. 6*b* illustrates a PSD estimate, where the filter chain approach is used. However, neither the approach according to (2) nor the one given in (3) is used here. This result, which delivers a reference curve for Fig. 7, is composed of 128 Welch PSD estimates, which have been performed on each of the filter output signals and put together to a complete spectrum. It can be seen that both results fit well and the main characteristic of both PSD estimates can be considered to be practically the same.

Fig. 7 shows a comparison of the PSD estimate from Fig. 6*b* with PSD estimates achieved by using the method according to (2) for $P_{j, \text{norm}}$ and (3) for $Q_{j, \text{norm}}$. It can be seen that both approaches approximate the actual spectral distribution very well. Only in regions with huge jumps in amplitude, mainly at positions, where Gaussian minimum shift keying (GMSK) blockers are present in the signal, markable differences occur. However, these are because of the averaging of power over a certain subband in the original signal, which is proposed in the given architecture, and can be improved by choosing finer resolution, meaning adding more filter and downsampling stages if needed.

In the following it will be shown that the resolution of the filter chain approach and the approximation of the spectrum of the given input signal satisfy the needs of the aspired application. Fig. 9 shows the simulation results using a reference scenario for an LTE bandwidth of 20 MHz as described in [6]. The legend in Fig. 8 lists all defined blockers. Note that the blockers given as CW blockers also only represent blockers of very small bandwidth in a real system. It can be seen that different blockers defined in the standard with different properties have to be considered. Fig. 9*a* and *b* present the detection accuracy of all blockers using the methods

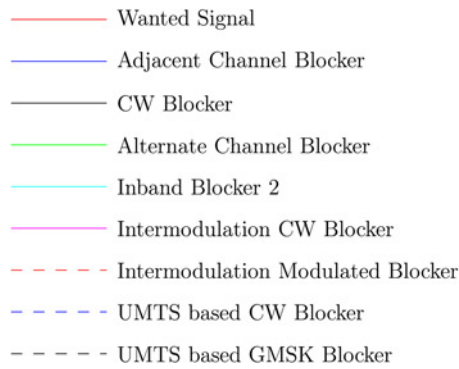


Fig. 8 Legend for the simulation curves

given in (2) and (3), respectively. In this test case, the power of the adjacent channel blocker is modified while all the other blockers' powers are constant. The absolute powers of all blockers are given in Fig. 9d. A value of 10 dB on the axis of abscissae means the adjacent channel blocker contains 10 dB more power than defined in the standard, whereas the offset of 0 dB refers to the reference test case. It can be seen that for a very wide range the blockers are detected accurately. In regions, where the detection error of certain blockers shows increased values, the detection can still be considered as successful. As can be seen from

Fig. 9d for those cases the misdetected blockers are no longer dominant and can therefore be neglected for further AFE and DFE configurations.

Fig. 9c shows a comparison of the two used methods for evaluating the detection accuracies. For deriving the curve, the difference from the curves in Fig. 9a and b is plotted. It can be seen that the less complex PSD estimation approach introduced in Section 3 and using $Q_{j,\text{norm}}$ has the same performance in a wide blocker power range. For different scenarios considering different LTE bandwidths and different blockers to be varied, similar results can be observed. This legitimates the given approach to be used in a real system.

The shown results are taken from an arbitrary scenario, in this case a typical LTE blocker detection scenario, and can be further generalised and adopted to any detection scenario.

5.2 Simulation results for the bit true simulation

In this section, the gained simulation results for the bit true implementation are presented. In each comparison, different bit widths (8–32 bit) are chosen. The wanted signal and the adjacent channel are exemplarily chosen and a bandwidth of 20 MHz is assumed. Similar results can be observed for different bandwidths and blockers to be detected.

The results for the 20 MHz test case at different bit widths are shown in Figs. 10a–d for the adjacent channel detection. The MATLAB floating point results are included as a reference. As

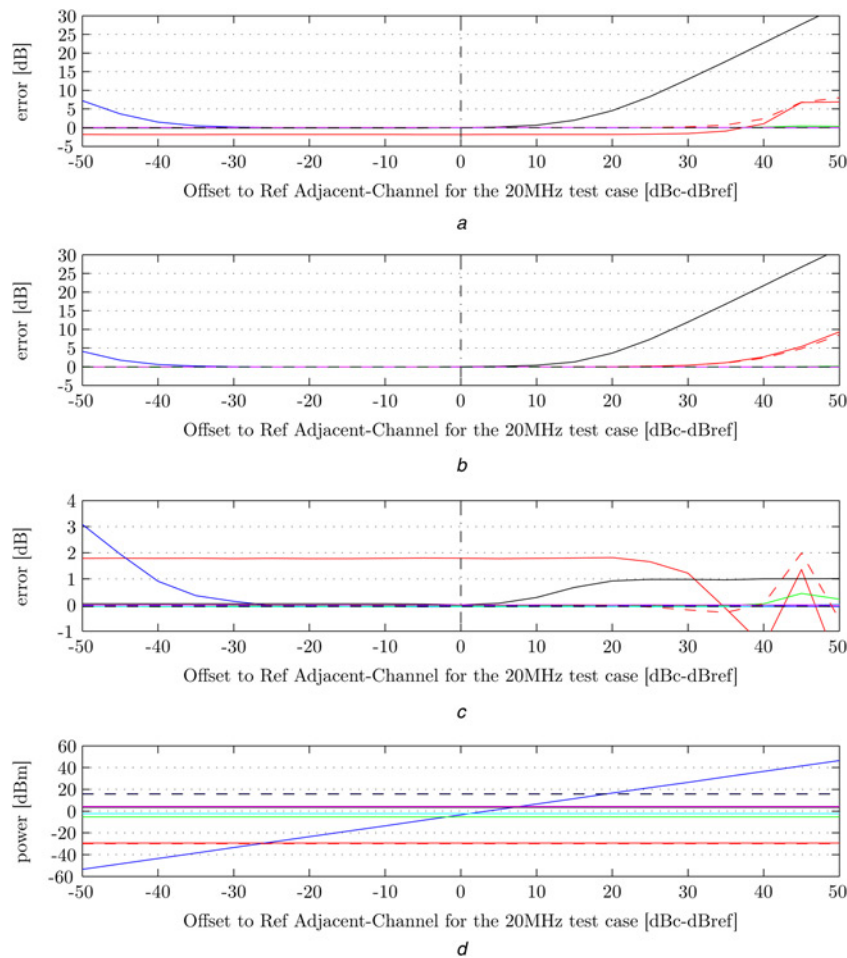


Fig. 9 Simulation results for the detection process

a Detection error in dB for the adjacent channel blocker power to be modified for the 20 MHz using P_{norm}

b Detection error in dB for the adjacent channel blocker to be modified in power for 20 MHz using Q_{norm}

c Comparison of the above blocker detection error curves

d Absolute blocker powers based on the LTE channel bandwidth in dBm/channel bandwidth

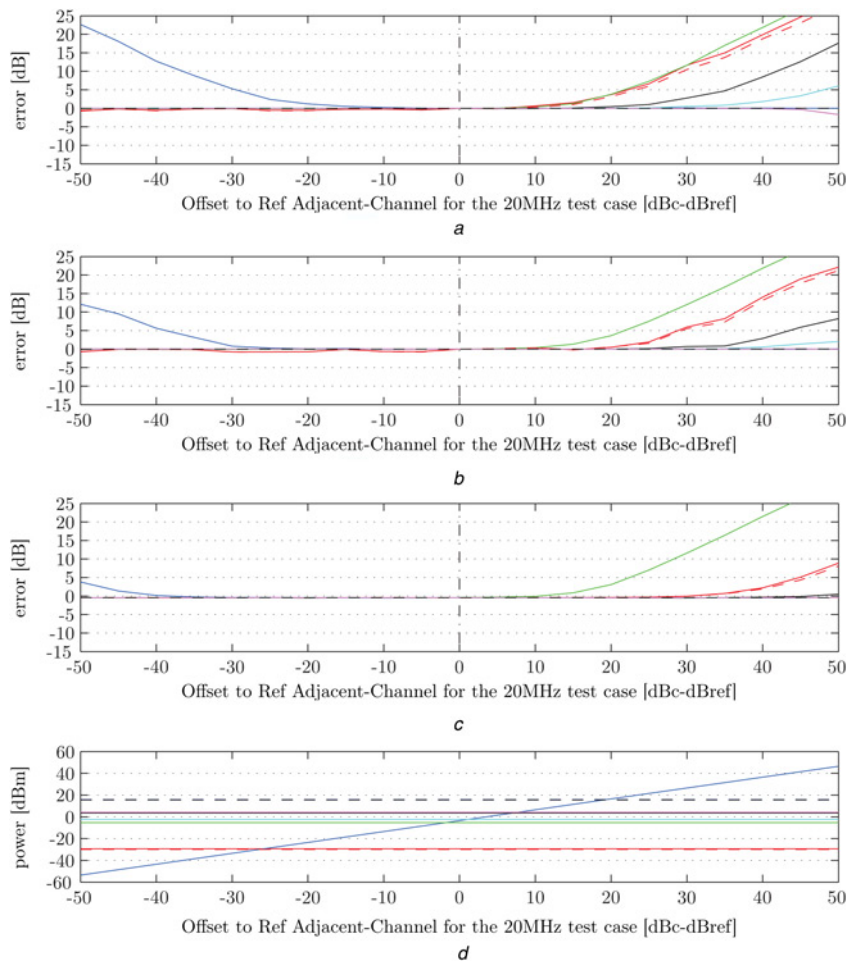


Fig. 10 Simulation results for the detection process

a 14 bit resolution

b 16 bit resolution

c Floating point simulation

d Absolute blocker powers based on the LTE channel bandwidth in dBm/20 MHz

can be seen, good performance for the wanted signal detection can be achieved for bit widths of 14.

6 Conclusion

A low-complexity concept for efficient spectrum sensing providing sufficient accuracy for blocker detection in LTE systems has been presented. The approach uses highly efficient low-cost multi rate dyadic filter banks. Furthermore, it was shown that the power calculation at each filter output can be decreased dramatically in complexity compared with the straight forward approach. Based on this approach intelligent AFEs and DFEs can be implemented, whereas the general spectrum sensing approach allows CR related applications as well.

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