Device and circuit performance analysis of double gate junctionless transistors at $L_g = 18$ nm

Chitrakant Sahu, Jawar Singh

Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology, Design and Manufacturing Jabalpur, Madhya Pradesh, India
E-mail: chitrakant@iiitdmj.ac.in

Published in *The Journal of Engineering*; Received on 6th January 2014; Accepted on 17th February 2014

Abstract: The design and characteristics of double-gate (DG) junctionless (JL) devices are compared with the DG inversion-mode (IM) field effect transistors (FETs) at 45 nm technology node with effective channel length of 18 nm. The comparison are performed at iso-V_{th} for both n- and p-type of devices. The JL device shows lower drain-induced barrier lowering, steep subthreshold slope and lower OFF state current. For the first time, the authors demonstrate a pass gate (PG) logic, inverter circuit and static random access memory (SRAM) stability analysis using JL devices, rather than a complementary metal-oxide semiconductor (CMOS) configuration. They observed that transient response of JL PG configuration is similar to that of conventional CMOS PGs. JL inverter also shows similar transient characteristics with 25% reduction in delay and 12% improvement in 6 T SRAM cell stability compared with IMFETs, which shows large potential in digital circuit applications. The simulations were performed using coupled device-circuit methodology in ATLAS technology aided computer design (TCAD) mixed-mode simulator.

1 Introduction

The aggressive scaling of metal-oxide semiconductor field effect transistor (MOSFET) has led to short-channel effects (SCEs) because of reduced gate controllability over the channel. In the nanoscale devices, the influence of SCE on the characteristics of conventional MOSFETs cannot be ignored. To reduce this influence, multi-gate structures such as double-gate (DG), surrounding-gate and FinFETs, which can suppress the SCEs and improve the capacity of control of the current, have been proposed [1–3]. However, aggressive scaling of semiconductor devices, the industry faces severe challenges while formation of steep source and drain junctions in short-channel devices. Therefore ultrafast annealing methods and the development of novel doping techniques are investigated which are complex and expensive. To address these issues, junctionless transistor (JLT) which contains a single doping species at the same level in its source, drain and channel has been proposed and investigated [4–6]. The JL devices are promising candidate for next generation high-speed and low-power integrated circuits owing to their excellent control of SCEs, ideal subthreshold swing (SS), low leakage current and good carrier transport efficiency [4–12]. Many reports on JLTs are available in the literature based on Lilienfeld's first transistor architecture [13] also Colinge *et al.* [4], Park *et al.* [5] and Jeon *et al.* [6] have successfully fabricated the multigate junctionless (JL) nanowire transistors. Different JLT architectures include double-gate architecture [7–9], bulk planar architecture [10], tri-gate nanowire architectures with silicon on insulator (SOI) as well as bulk substrate [11, 12, 14] and gate all-around architecture [15, 16].

The JL FET is very different from conventional MOSFET in terms of operating principle. The current in JLFET is because of majority carrier instead of minority and it flows in the volume instead of semiconductor-dielectric interface. In JLFET, most of the studies focused on the device performance estimation of JL transistors, but few addressed the circuit applications of such devices. Recently, Han *et al.* [14] has reported inverter based on tri-gate JL bulk FinFET and shown improved static noise margin (SNM) and reduced delay compared with inversion-mode (IM) bulk FinFET. As the double-gate/multigate devices are also promising candidates for the replacement of conventional MOSFETs because of their better electrostatic integrity, therefore one would be interested to know its circuit performance. A popular and widely used alternative to the conventional complementary metal-oxide semiconductor (CMOS) logic configuration is the pass gate (PG) configuration, which can significantly reduce the number of transistors required to implement a logic circuit. Also pass transistors are generally used as switches to pass logic levels between the nodes of a circuit, rather than as switches connected directly to the power supply. To transform the device level advantages of JLT into circuit level, we have investigated the circuit behaviour of JL devices. Mixed-mode simulation is typically used to simulate circuits that contain semiconductor devices for which accurate compact models do not exist, since JLT is an emerging device and from best of our knowledge there are no compact SPICE models available for circuit level simulation.

In this paper, we first optimised the JLFET for high-performance (HP) 45 nm technology node as defined by the Semiconductor Industry Association International Technology Roadmap for Semiconductors (ITRSs) [17], with effective channel length $L_g = 18$ nm, and compared the device and circuit performances with DG MOSFETs provided in [18]. The working and operation of n- and p-type DG JLT on PG configuration is described and its transient behaviour are observed using ATLAS mixed-mode simulation [19, 20]. Additionally, an inverter is designed with JL devices, where n and p channels were simply connected similar to existing CMOS inverter. We study how the increased gate capacitance and reduced drive capability affect the overall circuit performance and power dissipation. We also explored 6T static random access memory (SRAM) cell design making insightful comparisons with the DG MOSFET.

This paper is structured as follows. In Section 2, the simulation method and optimised parameters for studying the characteristics of devices and circuits are introduced. Section 3 consists of working and transient response of PG configuration JLT. In Section 4, the inverter and SRAM performances of IM and JL are compared. Finally, Section 5 summarises the conclusion.

2 Device and circuit simulation methodology

Fig. 1 show schematic views of (a) n-type and (b) p-type JL DGFETs. The JL device have silicon thickness ($T_{si} = 12$ nm), channel length ($L_g = 18$ nm) width ($W = 1$ μm) and source/drain (S/D) extensions are ($L_{ext} = 18$ nm), analogues to device design proposed in [18] for DG MOSFET. Gate oxide thickness (T_{ox}) of 1.2

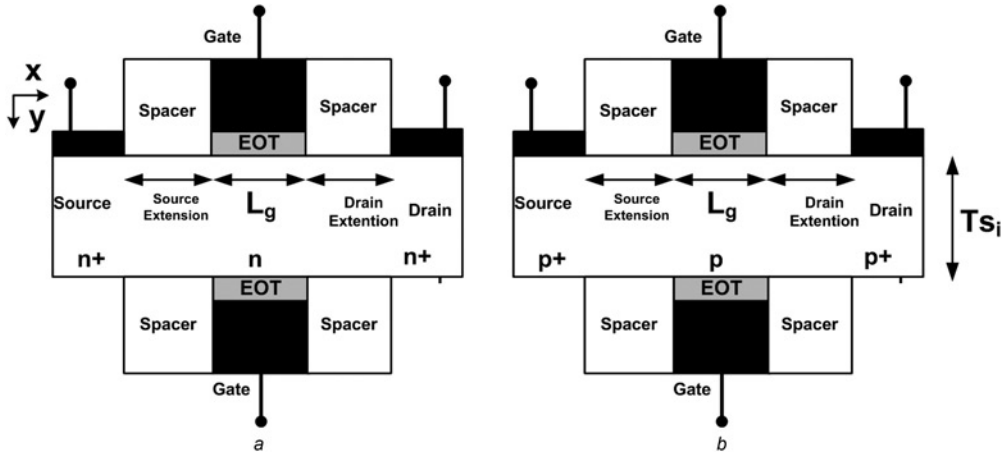

Fig. 1 *Cross-sectional view of*
a n-Type
b p-Type DG JLFET

nm have been used which is thick enough to avoid excessive gate tunnelling current in the HP device, as specified in the ITRS [17]. For a fair comparison between JL and IMFETs, linear threshold voltages V_{th} are adjusted to about ±0.3 V by tuning gate work-function and detailed parameters are provided in Table 1. The parasitic S/D series resistance R_S/R_D has two main components: the extension resistance R_{ext} and the contact resistance R_{con}. We estimated R_{ext} by numerically solving the following expression

$$R_{ext} = \int_0^{L_{ext}} \frac{1}{qN_{SD}(x)\mu(N_{SD})t_{si}}\,dx \tag{1}$$

where the carrier mobility depends on N_{SD} and R_{ext} is estimated as 46 and 77 Ωμm for n- and p-type DG MOSFET, respectively. Continued scaling of channel length decreases the channel resistance and increases the impact of parasitic S/D resistance on saturation current. The significant part of S/D resistance also lies on contact resistance since it is not scalable. Based on the transmission-line model, the contact resistance can be expressed as

$$R_{co} = \sqrt{\frac{\rho_{sd}\rho_c}{W}}\coth\left(l_c\sqrt{\frac{\rho_{sd}}{\rho_c}}\right) \tag{2}$$

where l_c is the width of the contact window, W is the transistor width, ρ_{sd} is the sheet resistivity of the source–drain diffusion and ρ_c is the interfacial contact resistivity of the ohmic contact between the metal and the silicon. R_{co} includes the resistance of the current crowding region in silicon underneath the contact. Equation (2) has two limiting cases: short contact and long contact. For the short contact limit $l_c \ll \sqrt{\rho_{sd}/\rho_c}$, we have

$$R_{co} = \frac{\rho_c}{Wl_c} \tag{3}$$

Equation (3) indicates that under short contact condition (which is the case for deep sub-micron devices) the contact resistance is dominated by the interfacial contact resistance and is determined by the contact window width. With the continued scaling of feature dimensions, l_c reduces and R_{co} increases. The channel resistance, however, decreases with the scaling of channel length. Therefore for deep sub-micron devices, without careful contact engineering, contact resistance can become dominant and the device current can be limited by S/D resistance instead of being controlled by gate, which results the transistors may cease to function properly. Thus, in order to capture the fundamental properties of double-gate fully depleted devices, in this study, we selected contact and S/D external resistance as specified in the ITRS [17]. The R_{ext} is estimated as 77 Ωμm, since the ITRS at 45 nm targets R_S/R_D = 125 Ωμm [17], then we assume a reasonable R_{con} = 48 Ωμm. Similarly, for p-type devices (1) yields R_{ext} = 46 Ωμm. Then, again assuming R_{con} = 110 Ωμm, we let R_S/R_D = 156 Ωμm. The JL and IM devices are simulated with same R_S/R_D and to match identical parasitic resistances, and to meet ITRS requirement for 45 nm technology node (with effective channel length 18 nm).

The simulation involves CVT model along with Shockley–Read–Hall (SRH) and Auger recombination models for minority carrier recombination. We have also included concentration dependent mobility (CONMOB) model for low field mobility related to doping density and field dependent mobility (FLDMOB) model for high field velocity saturation depending on parallel electric field in the direction of current flow. The inclusion of quantum effects in MOSFET circuit simulators is essential to accurately describe the electrical behaviours of today's nanoscale devices and to assess their performance limits. The necessary self-consistent solution of the two-dimensional (2D) Poisson and Schrodinger equation in a cross-section of the JL DGFET structure was incorporated by Silvaco ATLAS TCAD [19] with energy valley degeneration and bandgap narrowing taken into account in all the simulations. The keyword 2DXY.SCHRO is used to involve the 2D Poisson–Schrodinger solver. The keywords NUM.DIRECT and SP.DIR of models statement are used to select the valleys with appropriate effective mass. To refine small and noisy carrier concentration because of rapidly diminishing wave functions from the confining

Table 1 Device parameters of JL and IMFET

Parameters	JL FET	IMFET
channel doping concentration	N:1 × 10^{19} cm^{-3} P:1 × 10^{19} cm^{-3}	N:1 × 10^{15} cm^{-3} P:1 × 10^{15} cm^{-3}
source/drain doping concentration	N:1 × 10^{20} cm^{-3} P:1 × 10^{20} cm^{-3}	N:1 × 10^{20} cm^{-3} P:1 × 10^{20} cm^{-3}
gate work-function	N: 5.25 eV P: 4.17 eV	N: 4.8 eV P: 4.6 eV
S/D contact resistance	N: 48 Ωμm P: 110 Ωμm	N: 79 Ωμm P: 79 Ωμm
S/D extension resistance	N: 77 Ωμm P: 46 Ωμm	N: 46 Ωμm P: 77 Ωμm
S/D total resistance	N: 125 Ωμm P: 156 Ωμm	N: 125 Ωμm P: 156 Ωμm

doi: 10.1049/joe.2013.0269

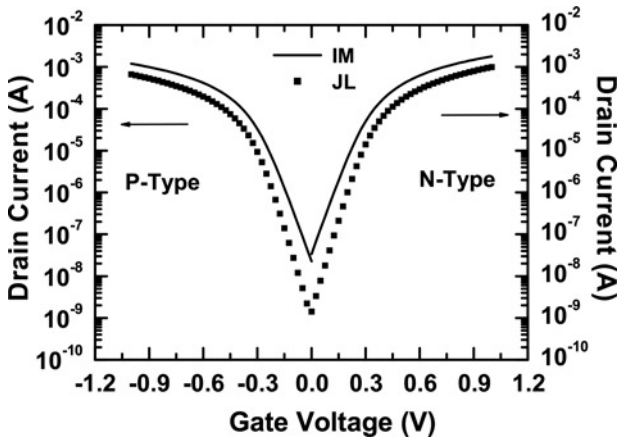

Fig. 2 *Transfer characteristics in logarithmic scales for the DG JLT and DG MOSFET at $V_{ds} = \pm 1$ V*

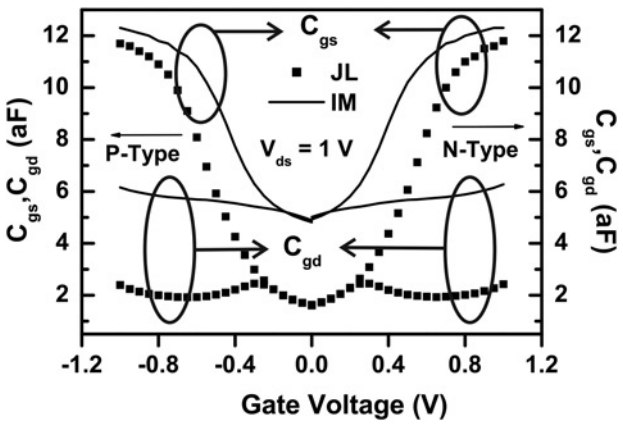

Fig. 3 *Gate to source (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate voltage for the n-type JL and IM DGFET at $V_{ds} = 1$ V*

Table 2 Extracted parameters of DG JL and IMFET

Devices	I_{on}/I_{off}	DIBL, mV/V	SS, mv/dec
nJLT	7.0×10^5	44.7	68.13
nFET	0.5×10^5	101.3	79
pJLT	9.0×10^5	43.2	67.4
pFET	1.0×10^5	100.2	78.2

potential barriers, quantum minimum carrier concentration (QMINCONC) is used. For the calculation of μ_{eff} in this simulation, a relationship between the effective channel mobility is used as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{phon}} + \frac{1}{\mu_{rough}} + \frac{1}{\mu_{bulk}} \tag{4}$$

The mobility consists of three parts: surface acoustic phonon scattering μ_{phon}, surface roughness scattering μ_{rough} and bulk mobility with doping-dependent modification μ_{bulk}; the details are given in [12]. The effective mobility value extracted from the simulations is 100 cm^2/V for devices with an impurity concentration of 10^{19} cm^{-3} and *Qss* is assumed to be 3×10^{12} cm^{-2}.

One of the major challenge in downscaling of nanoscale MOSFETs for low power consumption and high-speed nanoscale digital applications is the control of drain current in subthreshold regime with the reduction in the channel length. The subthreshold current is the leakage current that affects dynamics of the circuits and determines the CMOS standby power. A steep SS is also an important parameter that is a measure of conversion speed of transistor from ON to OFF that is given by $SS = d\ \mathrm{Log}(I_d)/dV_g$. In nanoscale MOSFET it is also seen that the influence of higher drain voltage leads to decreases in threshold voltage, which is also known as drain-induced barrier lowering (DIBL) effect. This effect is because of slope of surface potential in the drain side implying the effectiveness in reduction of electric field near the drain and presenting immunity to SCE because of increased drain voltages.

Fig. 2 shows $I_d - V_{gs}$ characteristics of *p*-channel (left) and *n*-channel (right) for both JL and IMFET, respectively. For a fair comparison, linear threshold voltages V_{th} are adjusted to about ±0.3 V by tuning gate work-function. The IM devices shows higher driving current but at the cost of higher subthreshold leakage current. JL device structure shows improved ON to OFF current ratio that can be observed from data provided in Table 2 because of reduced SCEs. JL devices also show lower SS and DIBL to those of the IM devices at gate lengths L_g of 18 nm. The

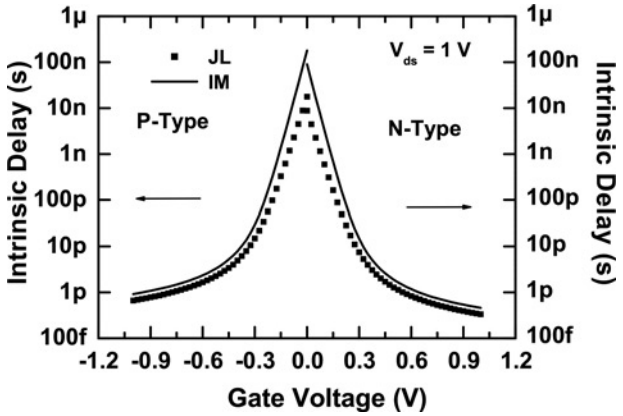

Fig. 4 *Intrinsic delay for both JL and IM devices as a function of gate voltage at $V_{ds} = \pm 1$ V*

reason for these differences is that, in conventional IM devices, some of the depletion charge is balanced by the source and drain at end of the channel. The severity of this phenomenon, which is known as the SCE, increases when the channel length is short. In contrast, JL devices do not have a concentration gradient between the source/channel and channel/drain to produce a junction. Therefore the charge is controlled by the gate alone, which substantially reduces SCEs. The steep SS and small DIBL values are key factors for future HP nanoscaled devices at low operating voltages.

Fig. 3 shows plot of C_{gs} and C_{gd} for JL and IM DGFET as a function of gate voltages. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz and drain voltage, $V_{ds} = 1$ V. The intrinsic capacitances depend on the operating region of the device, hence C_{gs} changes from subthreshold region to saturation region for both devices. However, C_{gd} is constant throughout because of effective voltage at drain end V_{gd} is not enough to make this end fully conducting. The larger values of C_{gs} and C_{gd} in the case of the IM devices result from lower channel doping as compared with JL devices. The gate capacitance $C_{gg} = C_{gs} + C_{gd}$ of JL and IM devices are observed 14aF and18aF, respectively, at $V_{gs} = V_{gs} = 1$ V. Fig. 4 shows intrinsic gate delay for JL and IM DGFET as a function of gate voltages. The intrinsic gate delay is important as it represents the frequency limit of the transistor operation. It is given by $C_{gg}V_{dd}/I_d$ where C_{gg} is the gate capacitance, V_{dd} is supply voltage and I_d is drain current. We observed that intrinsic gate delay is less in JL devices compared with the simulated IM devices. This is because of the lower gate capacitance of JL devices.

doi: 10.1049/joe.2013.0269

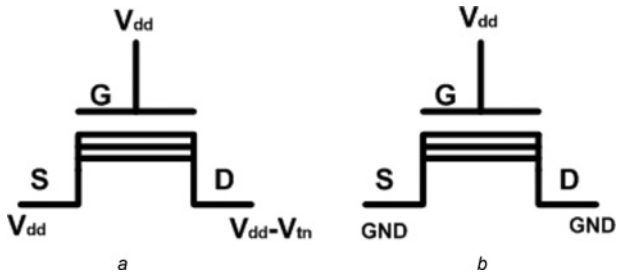

Fig. 5 *Pass gate configuration of p-type JLT*
a Passing '1'
b Passing '0'

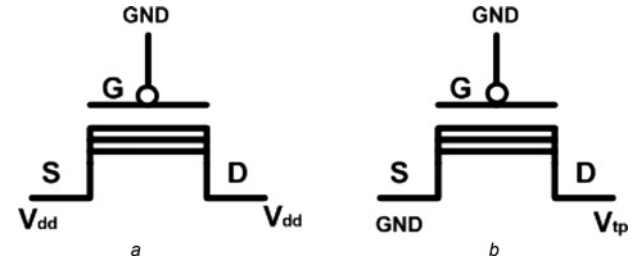

Fig. 7 *PG configuration of p-type JLT*
a Passing '1'
b Passing '0'

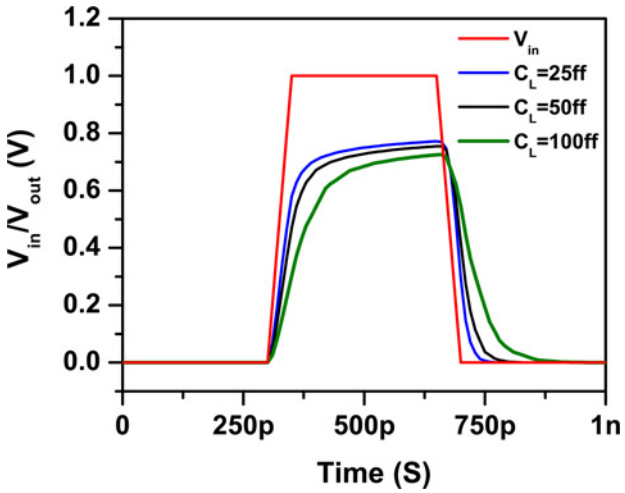

Fig. 6 *Transient behaviour of PG configuration n-type JLT at different capacitive loads*

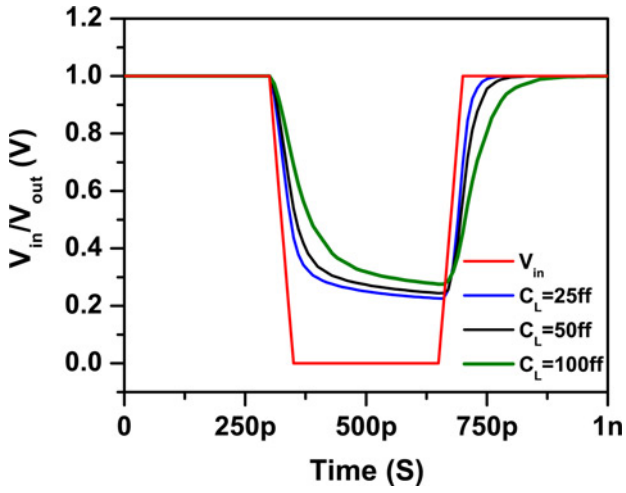

Fig. 8 *Transient behaviour of PG configuration p-type JLT at different capacitive loads*

3 JLT pass transistor configuration

A popular and widely used alternative to the conventional CMOS logic configuration is the PG configuration, which can significantly reduce the number of transistors required to implement a logic circuit. Also pass transistors are generally used as switches to pass logic levels between the nodes of a circuit, rather than as switches connected directly to the power supply. In conventional MOSFET, an n-type PG produces a 'strong zero' or ground and a 'weak one' by lowering the output below $V_{dd} - V_{tn}$, where V_{tn} is the threshold voltage of the nFET. In contrast, a p-type pass transistor produces a 'strong one', but a 'weak zero' by raising the output above V_{tp} when the input is zero, where V_{tp} is the threshold voltage of the pFET. The operating principle and simulation results for the PG configuration using both p-type and n-type JLT are described below.

3.1 DG nJLT PG

The configurations shown in Figs. 5*a* and *b* are n-type JL PG transistors. In new symbol of JLT parallel lines represent bulk conduction from source to drain. It passes the logic level on its source (input) to its drain (output), when its gate is driven to V_{dd} (when the PG is enabled). When the PG is disabled (its control gate is driven to ground), the resistance between the source (input) and drain (output) of the device, R_{ds}, is on the order of 100 kΩ. The PG can be useful when sharing a bus or a logic circuit and its inputs and outputs can be swapped that is, logic flow through the PG can be bi-directional. Fig. 6 shows how the output of a PG at various capacitive load conditions. The operation is similar to that of MOSFET PG and to keep the nJLT on, minimum voltage required is V_{tn}. It can be said that an nJLT device is not good at passing a '1' similar to MOSFET PG.

3.2 DG pJLT PG

Figs. 7*a* and *b* show PG configuration and Fig. 8 shows transient characteristics of pJLT at various capacitive load conditions. As expected the operation of the pJLT device is complementary to the nJLT's operation. The pJLT device turns on when its gate is driven to ground. If its gate is pulled to V_{dd}, the device is off (and the output is in the high resistance state). In Fig. 7*a*, the PG is passing a '1' to the output and (b) '0' is passed to the output. However, noting that the output only gets pulled down to V_{tp}. It can be said that a pJLT PG is good at passing a '1' and bad at passing a '0' similar to MOSFET PG.

4 Methodology of circuit simulation

Fig. 9*a* shows the JL inverter used as test circuits to estimate circuit characteristics. Fig. 9*b* shows the flowchart for coupled device-circuit approach for mixed-mode simulation. In mixed-mode simulation, operation is mainly divided in two parts. The first part includes the device description and simulation model parameters. The device descriptions provide information about device geometry, doping distribution and meshes. Simulation model parameters includes setting up models like mobility, recombination, impact ionisation etc. for simulation. The second part describes the circuit netlist and analysis. The circuit description includes the circuit topology (called 'netlist') and the electrical models and parameters of the circuit components. After that, bias condition and type of analysis like dc, ac and transient are described. First simulation

doi: 10.1049/joe.2013.0269

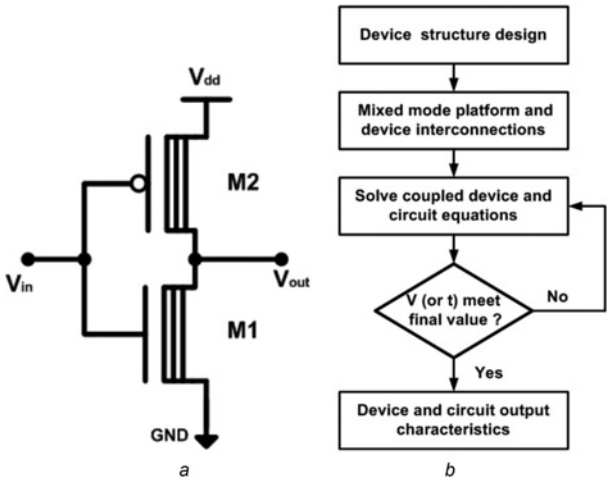

Fig. 9 *Test circuit and simulation methodology*
a JL FET inverter circuit
b Flowchart for the coupled device-circuit approach

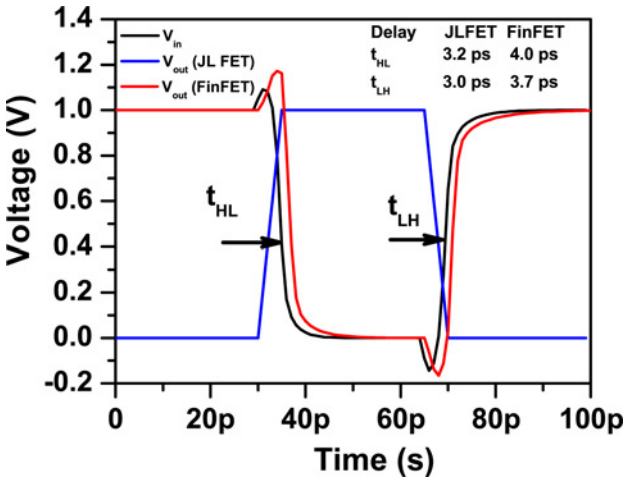

Fig. 10 *Transient characteristics of JL and IMFET inverter circuits, in which the definitions of high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) are indicated*

runs on the initial guess for the coupled device-circuit and then for nodal equations of the tested circuits. The nodal equation is formulated according to the Kirchhoff current law. Coupling the formulated circuit equations to the device transport equations obtains a large matrix containing both circuit and device equations. Solving the large matrix obtains the device and circuit characteristics simultaneously. The coupled simulation solves iteratively until it reaches its specified final voltage or time. When a simulation has finished it gives information about I-V data that is, voltages in all circuit nodes and currents in all circuit branches.

5 JL CMOS inverter performance

The CMOS inverter is a basic building block for digital circuit design and performs the logic operation of A to $\bar{A}$. The JL inverter, shown in Fig. 9*a* is a series combination of a *p*-channel and an *n*-channel JL DGFET. The gates of the two JL FETs connected together to form the input and the two drains are connected together to form the output similar to conventional CMOS inverter. When the input to the inverter is connected to ground, the output is pulled to V_{dd} through the pJLT device M_2 (M_1 shuts off). When the input terminal is connected to V_{dd}, the output is pulled to ground through the nJLT device M_1 (M_2 shuts off) similar to CMOS Inverter. As shown in Fig. 2 drain current of pJLT is approximately half of nJLT because of difference between mobility of electrons and holes. In inverter circuit both the devices are connected in series, in order to maintain same current, width of pJLT is taken twice of nJLT similar to conventional CMOS technology. The flowchart of coupled device-circuit approach using mixed-mode simulation of DG JL and MOSFET inverter circuits are shown in Fig. 9*b*. Results of transient and static characteristics are described below.

5.1 Propagation delay

Fig. 10 shows the transient characteristics of an inverter circuit based on JL and IMFETs and the high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) between and input output signals are also shown. When input signal switches from low to high voltage, the nJLT starts to turn on and pJLT is turned off. Similarly, when input signal switches from high to low voltage pJLT will turn on and nJLT will turn off. However, using the parameter setting in this paper, the simulated JL CMOS inverter circuit shows strikingly similar transient characteristics. The t_{HL} and t_{LH} values in the JL CMOS inverter are smaller than those observed in the IM CMOS inverter. Propagation delay t_p is defined as average of t_{HL} and t_{LH}. Reducing delay in digital circuit allows them to process data at a faster rate and improve overall performance. From transient response extracted values of t_{HL} and t_{LH} are 3.2 and 3.0 ps (JL inverter) and 4.0 and 3.7 ps (IM inverter), respectively. One can observe that the propagation delay of JL inverter is decreased by ~25%. Also the voltage overshoot in the transient response of inverter circuit is mainly attributed to the C_{gd} of the inverter transistors, which directly couples the steep voltage step at the input node to the output even before the response of transistor. Since in case of JL devices C_{gd} is low so the voltage overshoot is low as compared with IM inverter.

5.2 Static noise margin

The DC and transient behaviour exhibited by the proposed DG JL devices and inverter are very promising; therefore, we are extending this approach one more level higher for SRAM cell stability analysis. As SRAM is considered to be another benchmark circuit for evaluation of any emerging technology and its success absolutely depends of the proper realisation of SRAM cell. The stability of an inverter cell is often related to the SNM, which is defined as the highest dc noise voltage for which the cell state does not flip during its access. Generally, an SRAM cell operates in three different states: (i) standby; (ii) write; and (iii) read. As SRAM cell being most vulnerable to noise during read operations [21–23], therefore we estimated the read SNM. Fig. 11 shows the

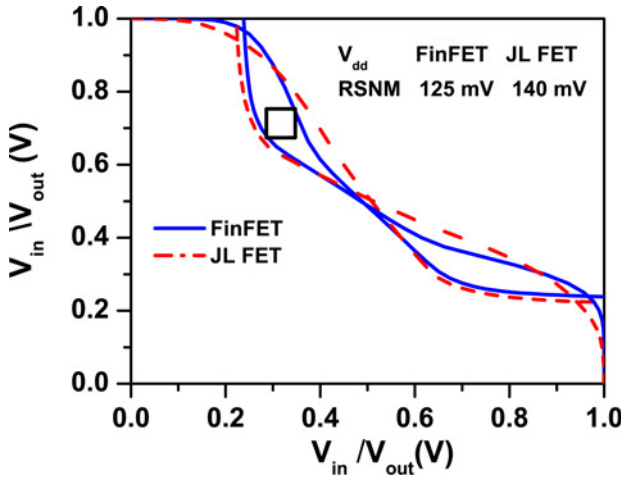

Fig. 11 *Static transfer characteristic curves of JL and IMFET inverter, in which the definition of read static noise margin (RSNM) is indicated*

plot for read SNM of standard 6 T SRAM cell. The JL FET-based SRAM's static transfer characteristics are very similar to those of the IMFET-based SRAM cell. The read SNM from both transfer characteristics are extracted by square fitting method that is the largest square to be fitted in between overlapped plot of inverter transfer characteristics and its inverse characteristics. The extracted values of read SNMs for JL- and IM DGFET-based SRAM cells are 140 and 125 mV, respectively. Hence, in terms of stability of SRAM cell, we can say that JL-based SRAM cell offers 12% improved stability as compared with DG MOSFET-based SRAM cell.

6 Conclusion

Simulations results show that the DG JLFET had a lower OFF current and better short-channel characteristics compared with its counterpart DG IMFET. Transient characteristics of PG configuration JL devices are similar to those of conventional MOSFET. The circuit performance comparisons show that the inverter and SRAM designed by JLT had similar transient and static transfer characteristics, comparable with those of DG MOSFETs. Also lowers gate capacitance in JL inverter devices leads to smaller miller capacitance, which speed up performance by 25% and 6 T SRAM cell stability is improved by 12%.

7 References

[1] Lee C.W., Afzalian A., Akhavan N.D., Yan R., Ferain I., Colinge J.P.: 'Junctionless multigate field-effect transistor', *Appl. Phys. Lett.*, 2009, **94**, pp. 053511-1–053511-2

[2] Colinge J.P., Gao M.H., Romano A., Maes H., Claeys C.: 'Silicon-on-insulator gate-all-around device'. IEDM Technical Digest, 1990, pp. 595–598

[3] Balestra F., Cristoloveanu S., Benachir M., Brini J., Elewa T.: 'Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly performance', *IEEE Electron Device Lett.*, 1987, **EDL-8**, (9), pp. 410–412

[4] Colinge J.P., Lee C.W., Afzalian A., *ET AL.*: 'Nanowire transistors without junctions', *Nat. Nanotechnol.*, 2010, **5**, (3), pp. 225–229

[5] Park C.-H., Ko M.-D., Kim K.-H., *ET AL.*: 'Electrical characteristics of 20-nm junctionless Si nanowire transistors', *Solid State Electron.*, 2012, **73**, (7), p. 710

[6] Jeon D.-Y., Park S.J., Mouis M., Barraud S., Kim G.-T., Ghibaudo G.: 'A new method for the extraction of flat-band voltage and doping concentration in tri-gate Junctionless transistors', *J. Solid-State Electron.*, **81**, (2013), pp. 113–118

[7] Chen Z., Xiao Y., Tang M., *ET AL.*: 'Surface-potential-based drain current model for long-channel junctionless double-gate mosfets', *IEEE Trans. Electron Devices*, 2012, **59**, (12), 3292–3298

[8] Duarte J.P., Choi S.J., Moon D.I., Choi Y.K.: 'Simple analytical bulk current model for long-channel double-gate junctionless transistors', *Trans. Electron Devices*, 2011, **32**, pp. 704–706

[9] Duarte J.P., Choi S.-J., Choi Y.-K.: 'A full-range drain current model for double-gate junctionless transistors', *IEEE Trans. Electron Devices*, 2011, **32**, (6), 704–706

[10] Bulk Planar Junctionless Transistor (BPJLT): 'An attractive device alternative for scaling', *IEEE Electron Device Lett.*, 2011, **32**, (3), 261–263

[11] Lee C.W., Afzalian A., Akhavan N.D., Yan R., Ferain I., Colinge J. P.: 'Junctionless multigate field-effect transistor', *Appl. Phys. Lett.*, 2009, **94**, pp. 1053511–1053511-2

[12] Trevisoli R., Doria R., de Souza M., Das S., Ferain I., Pavanello M.: 'Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors', *IEEE Trans. Electron Devices*, 2012, **59**, (12), pp. 3510–3518

[13] Lilienfeld J.E.: 'Method and apparatus for controlling electric cur-rent'. U.S. Patent 1 745 175, 1925

[14] Han M.-H., Chang C.-Y., Chen H.-B., Cheng Y.-C., Wu Y.-C.: 'Device and circuit performance estimation of junctionless bulk finFETs', *IEEE Trans. Electron Devices*, 2013, **60**, (6), 1807–1813

[15] Han M.-H., Chang C.-Y., Jhan Y.-R., *ET AL.*: 'Characteristic of *p*-type junctionless gate-all-around nanowire transistor and sensitivity analysis', *IEEE Electron Device Lett.*, 2013, **34**, (2), pp. 157–159

[16] Su C.J., Tsai T.I., Liou Y.L., Lin Z.M., Lin H.C., Chao T.S.: 'Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels', *Electron Device Lett.*, 2011, **32**, pp. 521–523

[17] International Technology Roadmaps for Semiconductor, ITRS, London, UK, 2008 ed., 2008

[18] Agrawal S., Fossum J.G.: 'On the suitability of a high-k gate dielectric in nanoscale finFET CMOS technology', *IEEE Trans. Electron Devices*, 2008, **55**, (7), pp. 1714–1719

[19] A.U. Manual. Device simulation software. In Silvaco Int., Santa Clara, CA, 2008

[20] Grasser T., Selberherr S.: 'Mixed-mode device simulation', *Microelectron. J.*, 2000, **31**, (11-12), pp. 873–881

[21] Seevinck E., List F.J., Lohstroh J.: 'Static-noise margin analysis of MOS SRAM cells', *IEEE J. Solid-State Circuits*, 1987, **22**, (5), pp. 748–754

[22] Bhavnagarwala A.J., Tang X., Meindl J.D.: 'The impact of intrinsic device fluctuations on CMOS SRAM cell stability', *IEEE J. Solid-State Circuits*, 2001, **36**, (4), pp. 658–665

[23] Li Y., Cheng H.-W., Han M.-H.: 'Statistical simulation of static noise margin variability in static random access memory', *IEEE Trans. Semicond. Manuf.*, 2010, **23**, (4), pp. 509–516

[24] Razavi P., Ferain I., Das S., Yu R., Akhavan N.D., Colinge J.: 'Intrinsic gate delay and energy-delay product in junctionless nanowire transistors'. 2012 13th Int. Conf. Ultimate Integration on Silicon (ULIS), 6–7 March 2012, pp. 125–128