Equivalent realisation circuit for a class of non-ideal voltage-controlled memristors

Saihu Pan, Pan Jiang, Bocheng Bao

School of Information Science and Engineering, Changzhou University, Changzhou 213164, Jiangsu, People's Republic of China
E-mail: mervinbao@126.com

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Abstract: In this study, an equivalent realisation circuit with off-the-shelf components and devices is proposed, which can be used to equivalently implement a class of non-ideal voltage-controlled memristors. The mathematical models of the equivalent realisation circuit with three function arithmetic circuits are built and their fingerprints are analysed by the pinched hysteresis loops with bipolar periodic voltage stimuli. The numerical simulations are easily verified by experimental measurements, which indicate that when three function arithmetic circuits are linked, the equivalent realisation circuit can realise three non-ideal voltage-controlled memristors with different non-linearities.

1 Introduction

Memristive equivalent realisation circuits, also known as memristor emulators with off-the-shelf components and devices behaving like memristors [1–7], are used to build physically implementable memristor application circuits, which are very useful for various memristor-based breadboard experiments due to no yet commercially available memristors. In these emulators, the equivalent realisation circuits of some ideal flux-controlled memristors with clear and articulate mathematical models [3–5] have received much attention in the designs and the investigations of various memristive chaotic circuits [5, 8–10]. However, the DC voltage integral drift of the integrator exists in the equivalent realisation circuit, which leads to that the experimental measurements of the memristive chaotic circuits are very difficult or completely incorrect. How can this problem be solved effectively?

In this paper, by connecting a parallel resistor to the integral capacitor and inserting into several different function arithmetic circuits in the equivalent realisation circuit of an ideal flux-controlled memristor, a new equivalent realisation circuit for some typical non-ideal voltage-controlled memristors with different non-linearities is presented, on which the corresponding mathematical modelling, fingerprint analyses, and circuit experimental verifications are performed. Fortunately, the DC voltage integral drift of the integrator in the equivalent realisation circuit can be avoided indeed, which is very useful to experimental observations of various memristor-based application circuits.

2 Proposed equivalent realisation circuit for memristors

The proposed equivalent realisation circuit for a class of non-ideal voltage-controlled memristors is shown in Fig. 1, which is composed of a buffer U_1, an integrator U_2 connected two resistors R_1, R_2, and a capacitor C_1, a function arithmetic circuit H, a multiplier M, and a current inverter U_3 connected three resistors R_3, R_4, and R_5. Different from the equivalent realisation circuits of the ideal flux-controlled memristors in [3–5], a parallel resistor R_2 is newly added to the integral capacitor C_1 in this proposed equivalent realisation circuit, which can effectively avoid DC voltage integral drift of the integrator [11].

Assume that in the proposed equivalent realisation circuit, v and i represent the voltage across and the current flowing through the input terminal, v_1 is the voltage across the integral capacitor C_1, and $v_o = H(v_1)$ stands for the output voltage of the function arithmetic circuit H. Observed from Fig. 1, the mathematical model is formulated as [4, 5]

$$i = W(v_1)v = [-a + bH(v_1)]v \tag{1}$$

$$\frac{\mathrm{d}v_1}{\mathrm{d}t} = f(v_1;\ v) = -\frac{v}{R_1C_1} - \frac{v_1}{R_2C_1} \tag{2}$$

where $W(v_1)$ is a continuous function of v_1, $f(v_1;v)$ is a continuous function of v_1 and v, $a = 1/R_3$, $b = g/R_3$, and g represents a variable scale factor in the multiplier M.

Three simple function arithmetic circuits depicted in Fig. 2 are taken as three examples. Correspondingly, their output voltages are [3–5]

$$v_o = H_a(v_1) = v_1 \tag{3}$$

$$v_o = H_b(v_1) = \frac{g_bR_{b2}E_{sat}}{R_{b1}}|v_1| \tag{4}$$

$$v_o = H_c(v_1) = g_cv_1^2 \tag{5}$$

where E_{sat} stands for the saturated output voltage of operational amplifier U_{b1} and g_b and g_c are two variable scale factors in the multipliers M_b and M_c, respectively.

Thus, the mathematical model described by (1) and (2) accords with the defining equations for the class of non-ideal voltage-controlled memristors [12]. Moreover, these memristors are active and controlled by the capacitor voltage v_1 and their memductances can be unified by

$$W(v_1) = -a + bH(v_1) \tag{6}$$

When three circuits in Fig. 2 are linked into the equivalent realisation circuit in Fig. 1, the equivalent realisation circuit can indeed implement three first-order non-ideal active voltage-controlled memristors.

3 Fingerprints of pinched hysteresis loops by simulations and experiments

To exhibit the fingerprints of the proposed equivalent realisation circuit in Fig. 1, the circuit parameters are fixed as $R_1 = 2$ kΩ, $C_1 = 33$ nF, $g = 0.1$, $R_3 = 0.5$ kΩ, and $R_4 = R_5 = 2$ kΩ, with AD633JN as analogue multiplier, AD711kN as operational amplifier, and operation voltages of ±15 V. When the sinusoidal voltage applied at the input terminal is $v = 2\sin(2\pi ft)$ V and the stimulus frequency f is set to 1 and 3 kHz, respectively, the loci in the v–i planes are hysteresis loops pinched at the origin, as shown in Fig. 3, where in Fig. 3*a*, the element parameter $R_2 = 10$ kΩ; in Fig. 3*b*, $R_2 = 3$ kΩ,

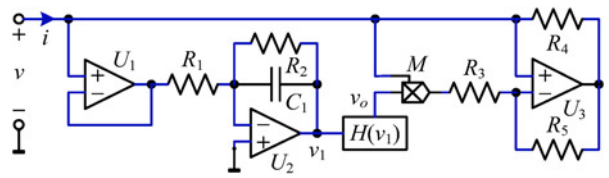

Fig. 1 *Proposed equivalent realisation circuit for a class of non-ideal voltage-controlled memristor*

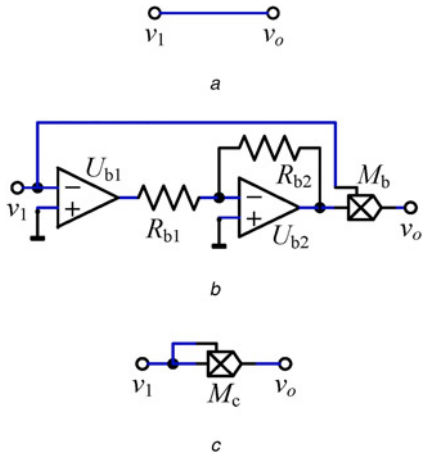

Fig. 2 *Three examples of function arithmetic circuits*
a Equal arithmetic circuit
b Absolute value arithmetic circuit
c Square arithmetic circuit

$R_{b1} = 13.5$ kΩ, $R_{b2} = 10$ kΩ, and $g_b = 0.2$; and in Fig. 3*c*, $R_2 = 3$ kΩ and $g_c = 1$.

The results of numerical simulations and circuit experiments in Fig. 3 verify that the equivalent realisation circuit in Fig. 1 can exhibit three characteristic fingerprints of the memristors [13], *i.e.* the equivalent realisation circuit with bipolar periodic voltage stimuli displays pinched hysteresis loops in the *v*–*i*-plane, the hysteresis lobe area starting from some critical frequency decreases monotonically as the voltage stimulus frequency increases, and

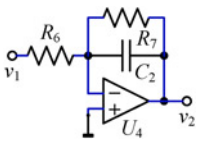

Fig. 4 *Integral circuit for second-order voltage-controlled memristor*

the pinched hysteresis loop shrinks to a single-valued function when the frequency tends to infinity. Therefore, the proposed equivalent realisation circuit has three fingerprints for identifying memristors [13], which can be used to implement a class of non-ideal voltage-controlled memristors.

It is remarkable that when another integral circuit shown in Fig. 4 is inserted between the integrator and the function arithmetic circuit in Fig. 1, the equivalent realisation circuit can be extended to implement three second-order non-ideal voltage-controlled memristors. The mathematical model for these memristors is uniformly expressed as

$$i = W(v_1,\ v_2)v = [-a + bH(v_1,\ v_2)]v \tag{7}$$

$$\frac{\mathrm{d}v_1}{\mathrm{d}t} = f_1(v_1,\ v_2;\ v) = -\frac{v}{R_1C_1} - \frac{v_1}{R_2C_1} \tag{8}$$

$$\frac{\mathrm{d}v_2}{\mathrm{d}t} = f_2(v_1,\ v_2;\ v) = -\frac{v_1}{R_6C_2} - \frac{v_2}{R_7C_2} \tag{9}$$

where $W(v_1, v_2)$ is a continuous function of v_1 and v_2, $f_1(v_1, v_2; v)$ and $f_2(v_1, v_2; v)$ are two continuous functions related to v_1, v_2, and v, a and b are the same as those of (1). Similar numerical simulations and experimental measurements can be performed to verify the model by (7)–(9). According to this extension method, an equivalent realisation circuit for high-order voltage-controlled memristors can be easily designed, on which many memristor-based breadboard experiments can be carried out.

4 Conclusions

In this paper, an equivalent realisation circuit for a class of non-ideal voltage-controlled memristors is presented. The equivalent realisation circuit is simple and consists only of already-existing components and devices. The mathematical modelling, numerical

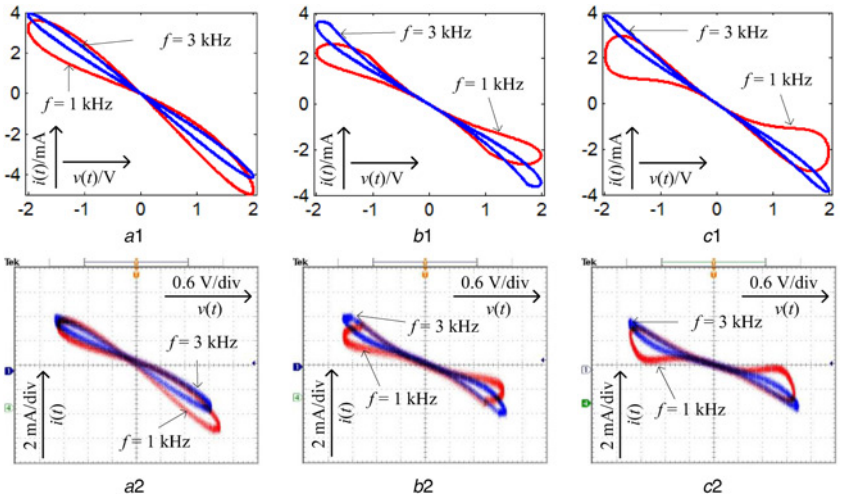

Fig. 3 *Pinched hysteresis loops of the equivalent realisation circuit driven by periodic voltages, where (a1), (b1), and (c1) are numerical simulations and (a2), (b2), and (c2) are experimental results*
a Equivalent realisation circuit linked with equal arithmetic circuit
b Equivalent realisation circuit linked with absolute value arithmetic circuit
c Equivalent realisation circuit linked with square arithmetic circuit

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simulations, and experimental measurements are performed, which demonstrate that the equivalent realisation circuit with some extendibility can exhibit wonderful memristive dynamics. Comparing with the equivalent realisation circuits of the ideal flux-controlled memristors in [3–5], the proposed equivalent realisation circuits can effectively avoid DC voltage integral drift of the integrator. Especially, when some memristive chaotic circuits are constructed by these voltage-controlled memristors, the corresponding system models become conventional models with several determined equilibrium points and circuit experiments is easy to fabricate with inexpensive already-existing components, which can be used as a teaching aid and for future applications with memristors.

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6 References

[1] Kim H., Sah M.P., Yang C., *ET AL.*: 'Memristor emulator for memristor circuit applications', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2012, **59**, (10), pp. 2422–2431, doi: 10.1109/ TCSI.2012.2188957

[2] Wang X.Y., Fitch A.L., Iu H.H.C., *ET AL.*: 'Implementation of an analogue model of a memristor based on a light-dependent resistor', *Chin. Phys. B*, 2012, **21**, (10), p. 108501, doi: 10.1088/1674-1056/21/10/108501

[3] Muthuswamy B.: 'Implementing memristor based chaotic circuits', *Int. J. Bifurcation Chaos*, 2010, **20**, (5), pp. 1335–1350, doi: 10.1142/ S0218127410026514

[4] Bao B.C., Xu J.P., Zhou G.H., *ET AL.*: 'Chaotic memristive circuit: equivalent circuit realization and dynamical analysis', *Chin. Phys. B*, 2011, **20**, (12), p. 120502, doi: 10.1088/ 1674-1056/20/12/120502

[5] Bao B.C., Hu F.W., Liu Z., *ET AL.*: 'Mapping equivalent approach to analysis and realization of memristor based dynamical circuit', *Chin. Phys. B*, 2014, **23**, (7), p. 070503, doi: 10.1088/ 1674-1056/23/7/070503

[6] Corinto F., Ascoli A.: 'Memristive diode bridge with LCR filter', *Electron. Lett.*, 2012, **48**, (14), pp. 824–825, doi: 10.1049/ el.2012.1480

[7] Bao B.C., Yu J.J., Hu F.W., *ET AL.*: 'Generalized memristor consisting of diode bridge with first order parallel RC filter', *Int. J. Bifurcation Chaos*, 2014, **24**, (11), p. 1450143, doi: 10.1142/ S0218127414501430

[8] Chen M., Yu J.J., Yu Q., *ET AL.*: 'A memristive diode bridge-based canonical Chua's circuit', *Entropy*, 2014, **16**, (12), pp. 6464–6476, doi: 10.3390/e16126464

[9] Bao B.C., Zou X., Liu Z., *ET AL.*: 'Generalized memory element and chaotic memory system', *Int. J. Bifurcation Chaos*, 2013, **23**, (8), p. 1350135, doi: 10.1142/S0218127413501356

[10] Iu H.H.C., Yu D.S., Fitch A.L., *ET AL.*: 'Controlling chaos in a memristor based circuit using a twin-T notch filter', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2011, **58**, (6), pp. 1337–1344, doi: 10.1109/ TCSI.2010.2097771

[11] Chen M., Yu J.J., Bao B.C.: 'Finding hidden attractors in improved memristor-based Chua's circuit', *Electron. Lett.*, 2015, **51**, (6), pp. 462–464, doi: 10.1049/el.2014.4341

[12] Chua L.O.: 'The fourth element', *Proc. IEEE*, 2012, **100**, (6), pp. 1920–1927, doi: 10.1109/JPROC.2012.2190814

[13] Adhikari S.P., Sah M.P., Kim H., *ET AL.*: 'Three fingerprints of memristor', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2013, **60**, (11), pp. 3008–3021, doi: 10.1109/TCSI.2013.2256171