# Time-division-multiplex control scheme for voltage multiplier rectifiers

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**Abstract:** A voltage multiplier rectifier with a novel time-division-multiplexing (TDM) control scheme for high step-up converters is proposed in this study. In the proposed TDM control scheme, two full-wave voltage doubler rectifiers can be combined to realise a voltage quadrupler rectifier. The proposed voltage quadrupler rectifier can reduce transformer turn ratio and transformer size for high step-up converters and also reduce voltage stress for the output capacitors and rectifier diodes. An *N*-times voltage rectifier can be straightforwardly produced by extending the concepts from the proposed TDM control scheme. A phase-shift full-bridge (PSFB) converter is adopted in the primary side of the proposed voltage quadrupler rectifier to construct a PSFB quadrupler converter. Experimental results for the PSFB quadrupler converter demonstrate the performance of the proposed TDM control scheme for voltage quadrupler rectifiers. An 8-times voltage rectifier is simulated to determine the validity of extending the proposed TDM control scheme to realise an *N*-times voltage rectifier. Experimental and simulation results show that the proposed TDM control scheme has great potential to be used in high step-up converters.

## 1 Introduction

Urgent demands on carbon dioxide reduction have allowed Renewable Energy Generation Systems (REGSs) to build up its share of the global electricity market. Photovoltaic Generation Systems (PVGSs) have enabled new projects, bringing the costs of PV generation per kilowatt hour much closer to fossil-fuel-based generation costs. The cumulative capacity of installed PVGSs worldwide was estimated to be around 184 GW at the end of 2014 and is expected that at a 4–5% increase in PVGS market growth can be reached in the next few years [1, 2]. New power converters designed for the special output characteristics of photovoltaic (PV) panels can increase the practicability of PVGSs and makes the PV industry more competitive. One of the special characteristics of PV panels is that the output voltage is usually <48 V; while 200/380 V DC-bus voltages are necessary in a single-phase full-bridge inverter used in a PVGS to interconnect to the 110/220 V AC grid. In particular, a DC-bus voltage of 760 V is usually required in the half-bridge inverter, neutral point clamp inverter and so on. Although the PV panels are usually connected in series to generate sufficient voltage to prevent high step-up voltage conversion, the independent converter applied to each PV panel can maximise the output power during partial shading and reduce the panel hot-spot risk [3, 4].

For the converter used in an individual PV panel, a high step-up voltage conversion ratio is required. Generally, a higher voltage conversion ratio can be realised by using transformers. Conventionally employed voltage-fed and current-fed converters with high transformer turn ratios are not well suited for high step-up applications. A higher transformer turn ratio often results in larger transformer size, larger leakage inductance, a more complicated transformer design and so on, which may cause high voltage stress on diodes and output capacitors and lower switching frequency [5–9]. Voltage doubler rectifiers, such as half-wave and full-wave voltage doubler rectifiers are better choices for high step-up applications because its output voltage is twice of the voltage in secondary winding of the transformer. Accordingly, the transformer turn ratio can be halved. However, the voltage stresses on the capacitors and/or the diodes are increased correspondingly. Cockcroft–Walton voltage multipliers proposed in [10, 11] can be used to reduce the voltage stresses on diodes. Dickson-type voltage multiplier and M-type voltage multiplier proposed in [12] can reduce the capacitor current stress. A symmetrical voltage quadrupler rectifier (SVQR) derived from two half-wave voltage doublers, which helps to decrease capacitor and diode stresses, was proposed in [13].

A voltage multiplier rectifier with a novel time-division-multiplexing (TDM) control scheme for high step-up converters is proposed in this paper. The TDM control scheme is used to control the energy transferred to the output capacitors at different time intervals. With the proposed TDM control scheme, two full-wave voltage doubler rectifiers can be combined to realise the proposed voltage quadrupler rectifier. The voltage quadrupler rectifier and TDM control scheme can reduce transformer turn ratio and transformer size for high step-up converters and also reduce voltage stresses for the output capacitors and rectifier diodes. Diodes and capacitors with a lower rated voltage can be adopted in the proposed rectifier meaning that better switching characteristics can be achieved. A phase-shift full-bridge (PSFB) converter is adopted in the primary side of the proposed voltage quadrupler rectifier to construct a PSFB quadrupler converter. The proposed PSFB quadrupler converter with specifications of an input voltage of 24 V DC, an output voltage of 200 V DC, and a rated power of 100 W, is designed and implemented in this paper. Experimental results for the implemented PSFB quadrupler converter demonstrate the performance of the proposed TDM control scheme for a voltage quadrupler rectifier. An *N*-times voltage rectifier can be straightforwardly produced from extending the concepts from the proposed TDM control scheme. An 8-times voltage rectifier is simulated to determine the validity of extending the proposed TDM control scheme to realise an *N*-times voltage rectifier. Experimental and simulation results show that the proposed novel TDM control scheme has great potential to be used in high step-up converters in PVGSs.

## 2 Basic concepts of voltage multiplier rectifiers

Fig. 1 illustrates the circuit configurations of half-wave and full-wave voltage doubler rectifiers, assuming the output values of secondary winding voltage, $v_{sec}$, can be either $+V_{sec}$, $-V_{sec}$, or zero in one switching cycle. Fig. 1*a* illustrates the operational modes for the half-wave voltage doubler rectifier. From the left-hand circuit of Fig. 1*a*, it can be observed that the energy is transferred to the capacitor $C_m$ where the voltage of $C_m$ reaches $V_{sec}$ during the negative half-cycle voltage of the secondary-side transformer. In the positive half-cycle voltage of secondary-side transformer as illustrated in the right-hand circuit of Fig. 1*a*, energy from the secondary-side transformer and capacitor $C_m$ are

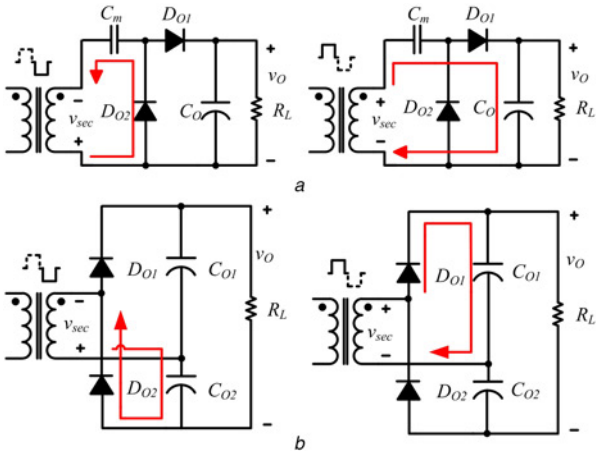



**Fig. 1** *Conventional circuit configurations of voltage doubler rectifiers*
*a* Half-wave voltage doubler rectifier
*b* Full-wave voltage doubler rectifier

transferred to the output capacitor $C_O$ where the voltage of $C_O$ reaches $2V_{sec}$. Fig. 1*b* shows the operational modes for the full-wave voltage doubler rectifier. The left-hand and right-hand circuits of Fig. 1*b* show that energy is transferred to the output capacitors $C_{O2}$ and $C_{O1}$ during the negative and positive half-cycles of the secondary-side transformer, respectively. The voltages of $C_{O2}$ and $C_{O1}$ both reach $V_{sec}$ giving an output voltage of $2V_{sec}$ by superposition.

Although higher step-up voltage ratios can be realised by adopting voltage doubler rectifiers, voltage stresses on diodes in the rectifiers are equal to the output voltage and still high. Therefore, some state-of-the-art voltage multiplier circuits such as the M-type voltage multiplier, the Dickson-type voltage multiplier and the Cockcroft–Walton voltage multiplier, have been proposed to reduce either the diode voltage stresses or the capacitor current stresses [10–13]. For example, a SVQR as shown in Fig. 2, derived from the half-wave voltage doubler, was proposed in [13]. The output voltage of a SVQR is four times of a conventional full-bridge voltage rectifier, which helps reduce the turns of the secondary winding and decreases the parasitic parameters of the transformer.

## 3 Proposed voltage multiplier rectifier

### 3.1 TDM control scheme

A voltage quadrupler rectifier derived from a full-wave voltage doubler rectifier is proposed in this paper. Fig. 3 illustrates the basic concepts of the proposed voltage quadrupler rectifier. From Fig. 3, it can be observed that two full-wave voltage doubler rectifiers are combined to construct the basic circuit configuration. The novel TDM control scheme is designed to transfer and store energy to the output capacitors from rectifier diodes at different time intervals. The output capacitors shown in Fig. 3 can achieve

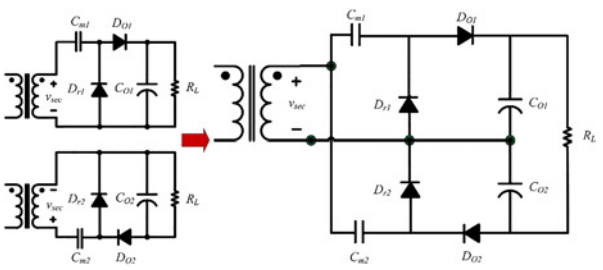


**Fig. 2** *Circuit configuration of the SVQR [13]*

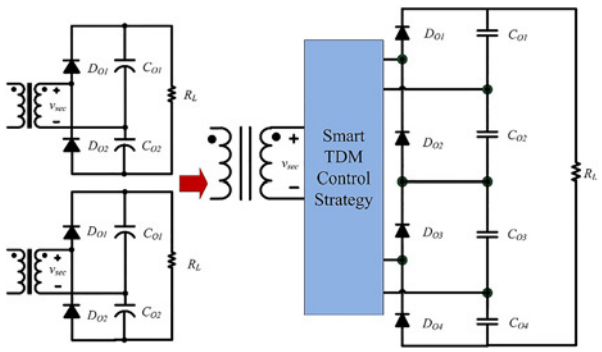



**Fig. 3** *Basic concepts of proposed voltage quadrupler rectifier*

close to equalising voltage where 4-times output voltage can be realised due to superposition of the output capacitor voltages.

Fig. 4*a* shows the novel TDM driving signals and the circuit configuration of proposed voltage quadrupler rectifier, respectively. Four auxiliary switches ($Q_5$–$Q_8$), constructing the TDM control circuit, are used to coordinate with the TDM control signals. Fig. 4*b* illustrates the operational modes when the auxiliary switches $Q_5$ and $Q_6$ are in the ON state. From Fig. 4*b*, it can be seen that energy is transferred to the output capacitors $C_{O1}$ and $C_{O2}$ during the positive and negative half-cycles of the secondary-side transformer, respectively. The voltages of $C_{O1}$ and $C_{O2}$ can both reach $V_{sec}$. Similarly, the voltages of $C_{O3}$ and $C_{O4}$ can also both reach $V_{sec}$ when the auxiliary switches $Q_7$ and $Q_8$ are in the ON state. Accordingly, each voltage of output capacitor can reach $V_{sec}$ and 4-times voltage can be realised.

SIMetrix/SIMPLIS [14] is used to simulate the circuit as shown in Fig. 4 to demonstrate the validity of the proposed voltage quadrupler rectifier with a novel TDM control scheme. The voltage magnitude of $v_{sec}$ is set at 50 V. Fig. 5 shows simulation results for output capacitor voltages and output voltage. From Fig. 5*a*, it can be seen that each of the output capacitors can almost achieve equalising voltage. Fig. 5*b* shows that 4-times voltage, i.e. 200 V, can be obtained. Therefore, the validity of the

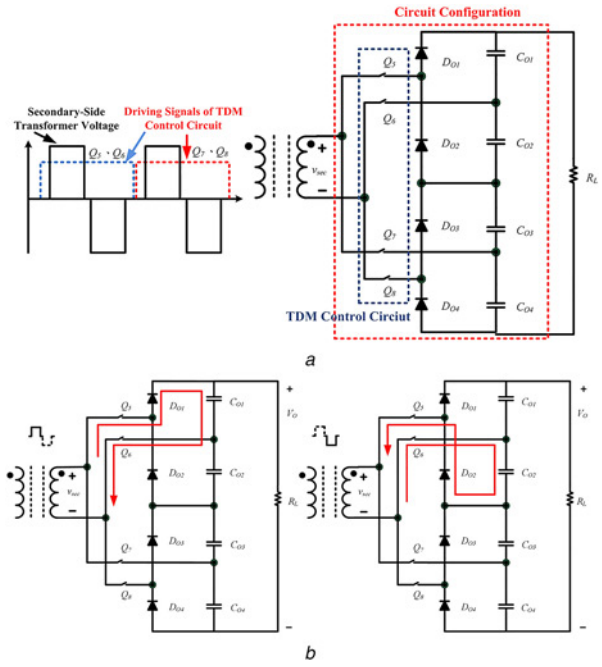



**Fig. 4** *TDM driving signal, circuit configuration and operation modes*
*a* Novel TDM driving signal and circuit configuration
*b* Operational modes

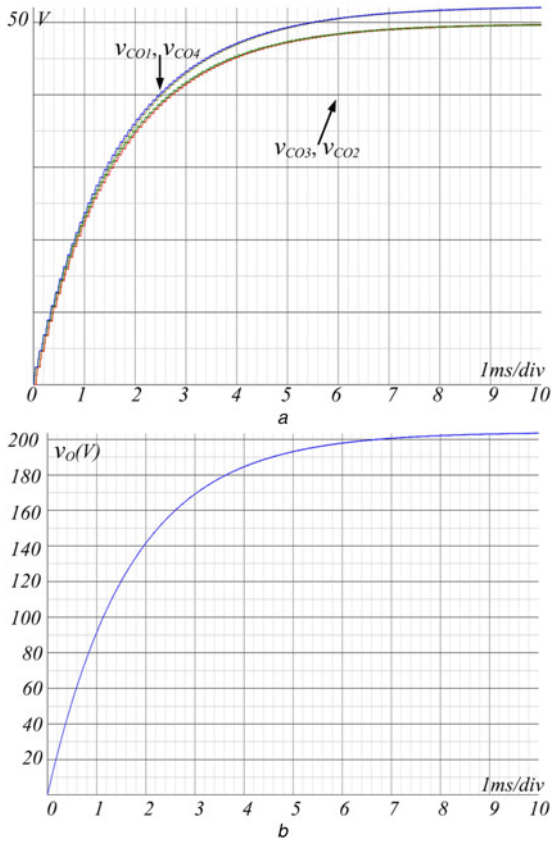



**Fig. 5** *Simulated results for the TDM control scheme*
*a* Voltages of output capacitors
*b* Output voltage

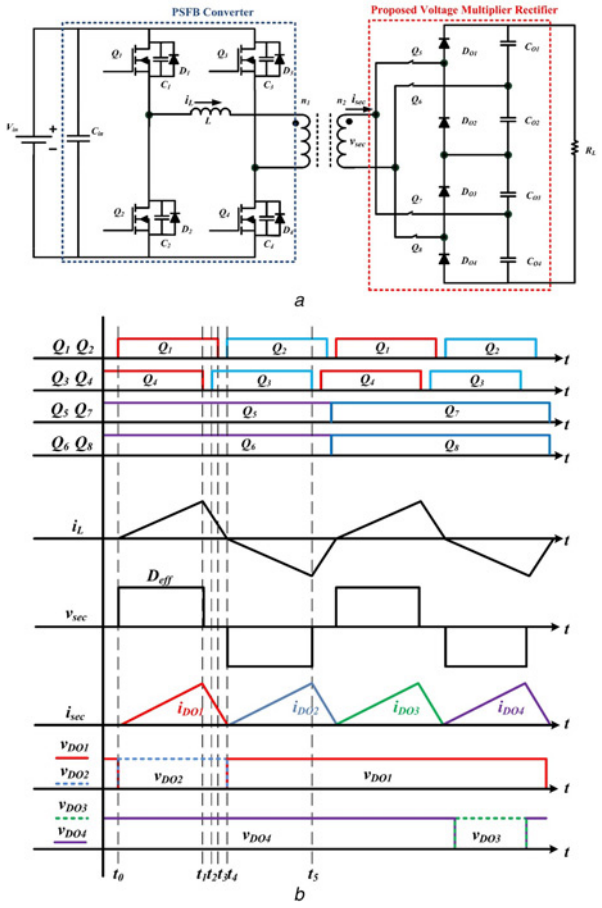



**Fig. 6** *Circuit configuration and key waveforms for proposed PSFB quadrupler converter*
*a* Circuit configuration
*b* Key waveforms

proposed voltage quadrupler rectifier with a novel control scheme can be demonstrated. The output voltage of proposed rectifier is double the half-wave and full-wave voltage doubler rectifiers, meaning the turn ratio of the transformer can be further reduced.

### 3.2 PSFB quadrupler with novel TDM control scheme

A PSFB converter is adopted in the primary side of the proposed voltage quadrupler rectifier to construct a PSFB quadrupler converter. Fig. 6*a* illustrates the circuit configuration of the proposed PSFB quadrupler converter. In Fig. 6*a*, the main switches ($Q_1$–$Q_4$) and the auxiliary switches ($Q_5$–$Q_8$) are used to control the PSFB converter and the TDM control circuit, respectively. Fig. 6*b* shows the theoretical key waveforms for the proposed PSFB quadrupler converter, where $i_L$ is the current of leakage inductor, $v_{sec}$ is the secondary-side voltage of transformer, $i_{sec}$ is the secondary-side current of transformer, and $v_{DOi}$ and $i_{DOi}$ are the voltage and current of diode $i$, respectively. The charging currents of output capacitors are designed and operated in discontinuous conduction mode to achieve zero-current switching for the auxiliary switches ($Q_5$–$Q_8$) and diodes ($D_{O1}$–$D_{O4}$). The switching losses can therefore be effectively reduced. The larger capacitance is needed for the output capacitors ($C_{O1}$–$C_{O4}$) to suppress the output voltage ripple. There are ten modes in one switching cycle of TDM control circuit; only five modes are analysed in detail due to the symmetrical structure of the proposed converter. The equivalent circuit for each operational mode is shown in Fig. 7.

*Mode 1 ($t_0 \le t < t_1$):* As shown in Fig. 7*a*, before $t_0$, main switch $Q_4$ and auxiliary switches $Q_5$ and $Q_6$ are in the ON state. At $t_0$, main switch $Q_1$ turns ON and then energy is transferred from $V_{in}$ to output capacitor $C_{O1}$ through the transformer, auxiliary switches $Q_5$ and $Q_6$, and output diode $D_{O1}$. The voltage of output capacitor $C_{O1}$ can be expressed as

$$V_{C_{O1}} = \left(\frac{n_2}{n_1}\right) \cdot D_{eff} \cdot V_{in} \quad (1)$$

where $V_{C_{Oi}}$ is the average voltage of output capacitors $C_{Oi}$, $V_{in}$ is the input voltage, $n_1$ and $n_2$ are the winding turns for primary side and secondary side of the transformer, respectively, and $D_{eff}$ is the effective duty cycle of the PSFB converter as illustrated in Fig. 6*a*.
*Mode 2 ($t_1 \le t < t_2$):* At $t_1$, main switch $Q_4$ turns OFF and then the leakage inductor current $i_L$ charges and discharges parasitic capacitors $C_3$ and $C_4$, respectively, due to current continuity as shown in Fig. 7*b*. Meanwhile, $i_L$ decreases almost linearly. It goes to next mode when the voltage of $C_4$ reaches $V_{in}$.
*Mode 3 ($t_2 \le t < t_3$):* At $t_2$, main switch $Q_3$ turns ON. Zero voltage switching (ZVS) can be achieved due to the voltage across $Q_3$ (the voltage of $C_3$) having been decreased to zero. As shown in Fig. 7*c*, the leakage inductor current $i_L$ starts free-wheeling through $Q_1$ and $Q_3$.
*Mode 4 ($t_3 \le t < t_4$):* At $t_3$, the main switch $Q_1$ turns OFF and then the leakage inductor current $i_L$ charges and discharges parasitic capacitors $C_1$ and $C_2$, respectively, due to current continuity as shown in Fig. 7*d*. It goes to next mode when the voltage of $C_1$ reaches $V_{in}$.
*Mode 5 ($t_4 \le t < t_5$):* At $t_4$, $Q_2$ turns ON. ZVS can be achieved due to the voltage across $Q_2$ (the voltage of $C_2$) having been decreased to zero. As shown in Fig. 7*e*, the current of the leakage inductor $i_L$ falls to zero at $t_4$, and after that, energy is transferred from $V_{in}$ to output capacitor $C_{O2}$ through the transformer, auxiliary switches

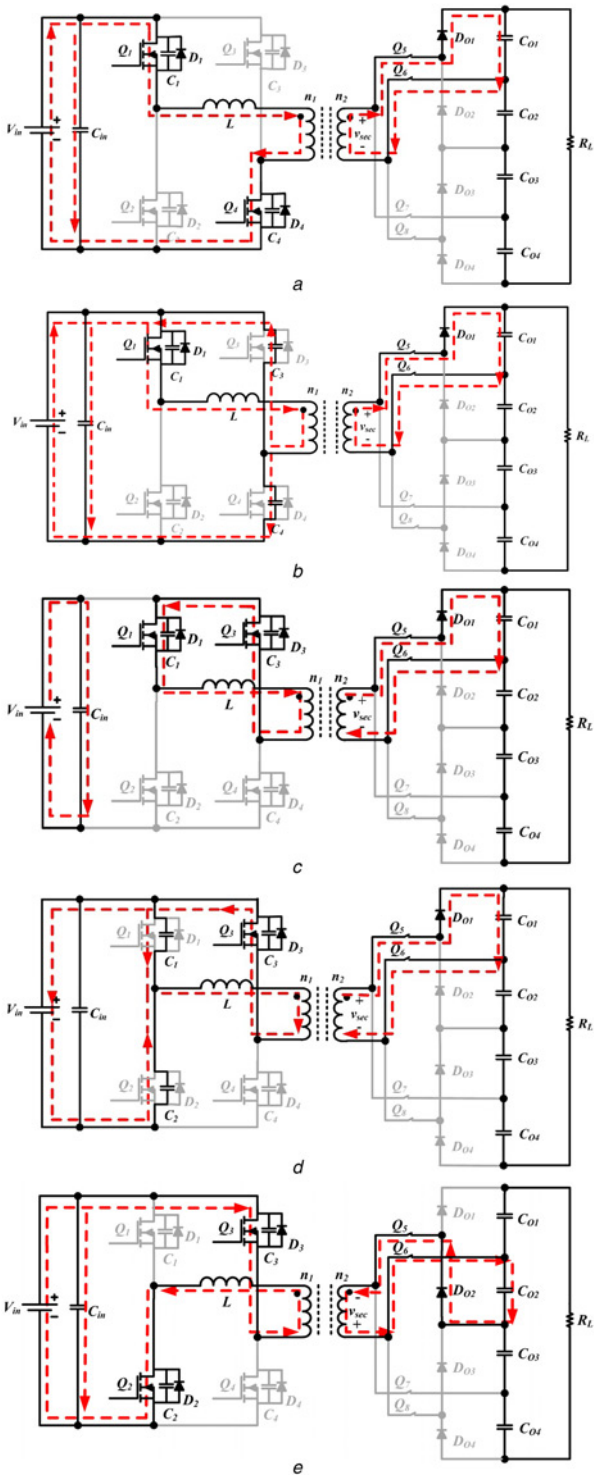


**Fig. 7** *Operational modes of proposed PSFB quadrupler converter*
*a* Mode1 ($t_0 \le t < t_1$)
*b* Mode 2 ($t_1 \le t < t_2$)
*c* Mode 3 ($t_2 \le t < t_3$)
*d* Mode 4 ($t_3 \le t < t_4$)
*e* Mode 4 ($t_4 \le t < t_5$)

$Q_5$ and $Q_6$, and output diode $D_{O2}$. The voltage of output capacitor $C_{O2}$ can be expressed as

$$V_{C_{O2}} = \left(\frac{n_2}{n_1}\right) \cdot D_{\text{eff}} \cdot V_{\text{in}} \tag{2}$$

The remaining modes of proposed converter can be analysed using similar procedures as the aforementioned five modes. From Fig. 7, it can be easily observed that the voltages of output capacitors can be expressed as

$$V_{C_{O1}} = V_{C_{O2}} = V_{C_{O3}} = V_{C_{O4}} = \left(\frac{n_2}{n_1}\right) \cdot D_{\text{eff}} \cdot V_{\text{in}} \tag{3}$$

The output voltage can be calculated by superposition and be written as

$$V_{\text{O}} = V_{C_{O1}} + V_{C_{O2}} + V_{C_{O3}} + V_{C_{O4}} \tag{4}$$

where $V_{\text{O}}$ is the average output voltage of the PSFB quadrupler converter.

The voltage gain of the proposed converter is

$$\frac{V_{\text{O}}}{V_{\text{in}}} = \frac{V_{C_{O1}} + V_{C_{O2}} + V_{C_{O3}} + V_{C_{O4}}}{V_{\text{in}}} = 4 \cdot \left(\frac{n_2}{n_1}\right) \cdot D_{\text{eff}} \tag{5}$$

The voltage stresses of the output diodes are halved compared with half-wave and full-wave voltage doubler rectifiers due to the proposed TDM control scheme making two full-wave rectifiers work at different time intervals. The voltage stresses of output diodes can be expressed as

$$V_{D_{O1}} = V_{D_{O2}} = V_{D_{O3}} = V_{D_{O4}} = \frac{V_{\text{O}}}{2} \tag{6}$$

where $V_{D_{Oi}}$ is the average voltage of output diode $D_{Oi}$.

Meanwhile, the current stresses of the output diodes are equal to the current of the secondary side of transformer, i.e.

$$I_{D_{O1}} = I_{D_{O2}} = I_{D_{O3}} = I_{D_{O4}} = I_{\text{sec}} \tag{7}$$

where $I_{D_{Oi}}$ is the average current of output diode $D_{Oi}$ and $I_{\text{sec}}$ is the average current in the secondary side of transformer.

Table 1 compares the performances of the proposed voltage quadrupler rectifier with a SVQR as proposed in [13]. From Table 1, it can be observed that the proposed rectifier and the SVQR have similar performances on diode number, capacitor number, diode voltage stress and diode current stress. The maximum voltage stress of auxiliary switches ($Q_5$–$Q_8$) is $V_{\text{O}} - V_{\text{CO}}$. However, lower voltage stress on output capacitors can be realised using the proposed rectifier. Diodes and capacitors with lower rated voltages usually mean better switching characteristics. The disadvantage of the proposed rectifier is the four additional auxiliary switches ($Q_5$–$Q_8$) have to be used to construct the TDM control circuit and therefore increases the overall cost of the proposed PSFB quadrupler converter. Since the low-voltage-rated metal–oxide–semiconductor field-effect transistor (MOSFET) is relatively inexpensive, the proposed TDM control circuit with more elastic voltage multiplier can be realised without significant increase in the overall cost. Besides, in order to reduce switching losses induced by the four additional auxiliary switches ($Q_5$–$Q_8$),

**Table 1** Performance comparisons of proposed rectifier and SVQR

| Multiplier rectifier | Proposed rectifier | SVQR [13] |
|---|---|---|
| Diode number | 4 | 4 |
| Capacitor number | 4 | 4 |
| Diode voltage stress | $V_{\text{O}}/2$ | $V_{\text{O}}/2$ |
| Diode current stress | $I_{\text{O}}$ | $I_{\text{O}}$ |
| Output capacitor voltage stress | $V_{\text{O}}/4$ | $V_{\text{O}}/2$ |
| Potential for $N$-times voltage | yes | no |

where $V_{\text{O}}$ and $I_{\text{O}}$ are output voltage and output current, respectively.

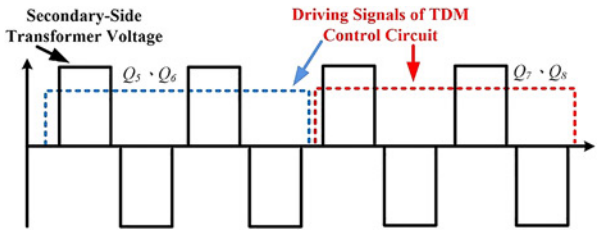



**Fig. 8** *Another novel TDM driving signals*

different TDM driving signals can be applied to the TDM control circuit. For example, another novel TDM driving signal is shown in Fig. 8. From Fig. 8, it can be seen that the switching frequency for the auxiliary switches ($Q_5$–$Q_8$) in the TDM control circuit can be decreased. If the voltage frequency in the secondary side of transformer is 50 kHz, then the switching frequencies for the auxiliary switches ($Q_5$–$Q_8$) in Figs. 4*a* and 8 are 25 and 12.5 kHz, respectively. Due to lower switching frequency, lower-cost switches can be utilised and lower switching loss can also be achieved in the TDM control circuit. The charging currents of output capacitors are designed and operated in discontinuous conduction mode to achieve zero-current switching for the auxiliary switches ($Q_5$–$Q_8$) and diodes ($D_{O1}$–$D_{O4}$). The switching losses can therefore be effectively reduced. The larger capacitance is needed for the output capacitors ($C_{O1}$–$C_{O4}$) to suppress the output voltage ripple. From Fig. 5*a*, it can be seen that the voltage ripples on the output capacitors ($C_{O1}$–$C_{O4}$) are small. The special characteristic of the proposed novel TDM control scheme is that an *N*-times voltage rectifier can be extended straightforwardly. Fig. 9 shows the circuit configuration of the proposed *N*-times voltage rectifier. The TDM driving signals can be easily modified from Figs. 4*a* and 8 and are not shown here. Consequently, the proposed rectifier and TDM control circuit can be extended to construct an *N*-times voltage rectifier without extra burden.

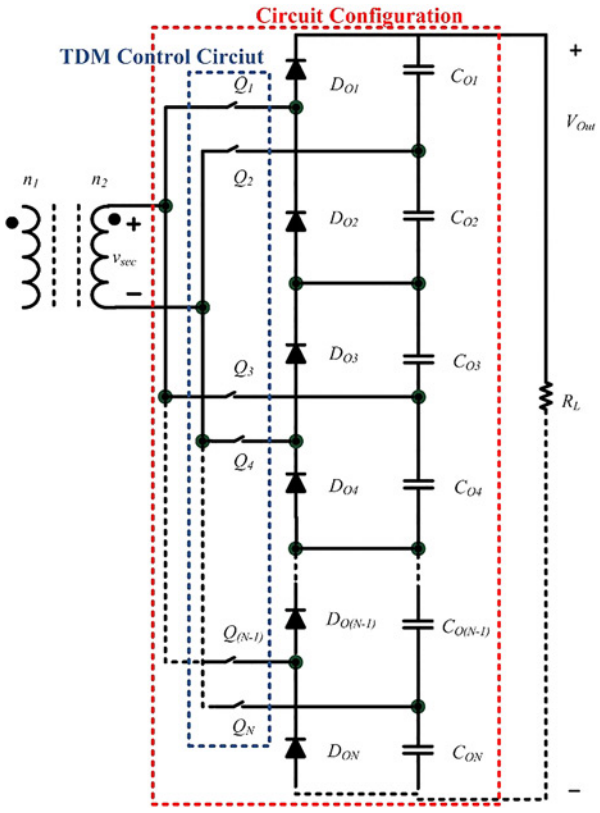



**Fig. 9** *Proposed N-times voltage rectifier*

**Table 2** Parameters of proposed PSFB quadrupler converter

| | |
|---|---|
| Input voltage | 24 V |
| Output voltage | 200 V |
| Rated power | 150 W |
| Switching frequency of PSFB converter | 50 kHz |
| Switching frequency of TDM control circuit | 25 kHz |
| $Q_1$, $Q_2$, $Q_3$, $Q_4$ | IRFP4227PbF |
| $Q_5$, $Q_6$, $Q_7$, $Q_8$ | IRFP4227PbF |
| $D_{O1}$, $D_{O2}$, $D_{O3}$, $D_{O4}$ | DHG30I600HA |
| $C_{O1}$, $C_{O2}$, $C_{O3}$, $C_{O4}$ | 330 µF × 4 |
| Transformer turn ratio ($n_2/n_1$) | 2.5 |

## 4 Experimental and simulation results

A PSFB quadrupler converter is implemented to demonstrate the performance of the proposed TDM control scheme for voltage multiplier rectifiers. An 8-times voltage rectifier is simulated to determine the validity of extending the proposed TDM control scheme to realise an *N*-times voltage rectifier.

### 4.1 Experimental results

The proposed PSFB quadrupler converter with specifications of an input voltage of 24 V DC, an output voltage of 200 V DC, and a rated power of 100 W, is designed and implemented in this paper. To prevent the possible reverse currents in the proposed TDM control circuit, the reverse blocking MOSFETs (RB-MOFETs), realised by adding minor changes to the structure of a standard MOSFET to make it capable of withstanding reverse current and voltage, are utilised for auxiliary switches ($Q_5$–$Q_8$). Table 2 lists the parameters of the proposed PSFB quadrupler converter. Microchip dsPIC33FJ16GS504 [15] is used to realise a fully-digitalised controller for the proposed converter. Fig. 10 illustrates the driving signals for $Q_1$, $Q_2$, $Q_5$, and $Q_7$. From Fig. 10*a*, it can be seen that the switching frequencies for main switches ($Q_1$–$Q_4$) and auxiliary switches ($Q_5$–$Q_8$) are about 50 and 25 kHz, respectively. Another TDM driving signals used to reduce the switching frequency for auxiliary switches ($Q_5$–$Q_8$) in the TDM control circuit are shown in Fig. 10*b*. Fig. 10*b* shows that the switching

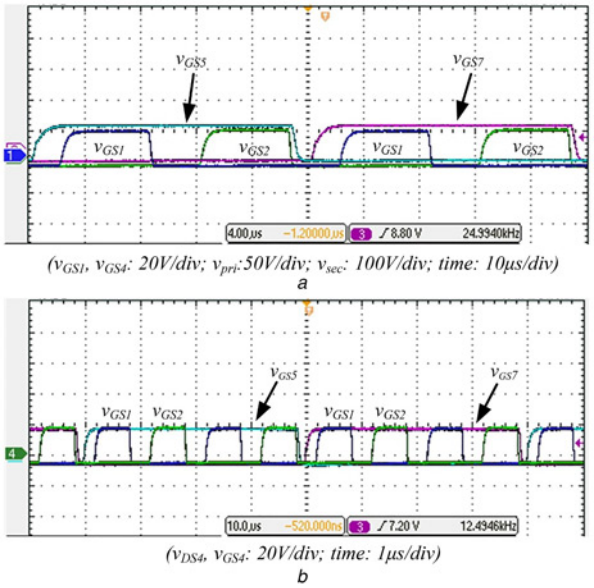
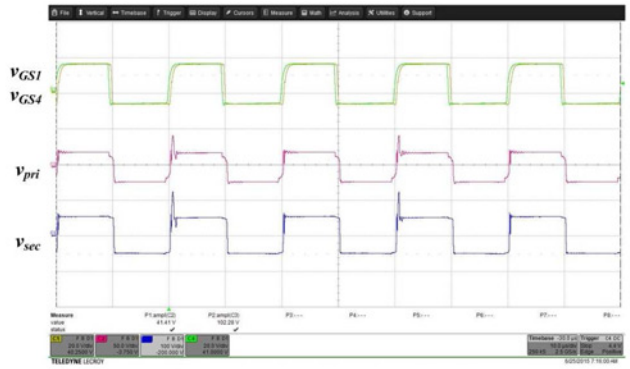



**Fig. 10** *Driving signals for $Q_1$, $Q_2$, $Q_5$, and $Q_7$*
*a* Switching frequencies of 25 kHz for $Q_5$ and $Q_7$
*b* Switching frequencies of 12.5 kHz for $Q_5$ and $Q_7$

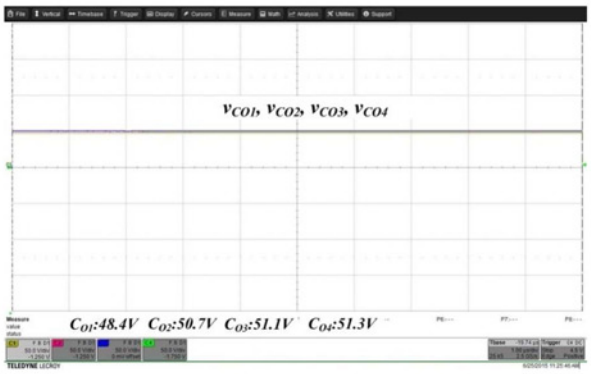



($v_{GS1}$, $v_{GS4}$: 20V/div; $v_{pri}$:50V/div; $v_{sec}$: 100V/div; time: 10μs/div)

*a*


($v_{DS4}$, $v_{GS4}$: 20V/div; time: 1μs/div)

*b*




($v_{CO1}$, $v_{CO2}$, $v_{CO3}$, $v_{CO4}$: 50V/div; time: 1μs/div)

*c*


($V_{dc1}$ is input voltage. $I_{dc1}$ is input current. $P_1$ is input Power. $V_{dc2}$ is output voltage. $I_{dc2}$ is output current. $P_2$ is output Power. $\eta_1$ is the conversion efficiency of proposed converter.)

*d*

**Fig. 11** *Experimental results of the proposed converter under an output power of 100 W*
*a* Voltage waveforms of transformer
*b* Voltage waveforms for $Q_4$
*c* Voltage waveforms for output capacitors
*d* Conversion efficiency

frequencies for main switches ($Q_1$–$Q_4$) and auxiliary switches ($Q_5$–$Q_8$) are about 50 and 12.5 kHz, respectively. From Fig. 10, the proposed novel TDM driving signals can be confirmed.

Fig. 11*a* shows the driving signals of main switches $Q_1$ and $Q_4$ and the voltage waveforms of the transformer under an output power of 100 W. From Fig. 11*a*, the phase shift in the driving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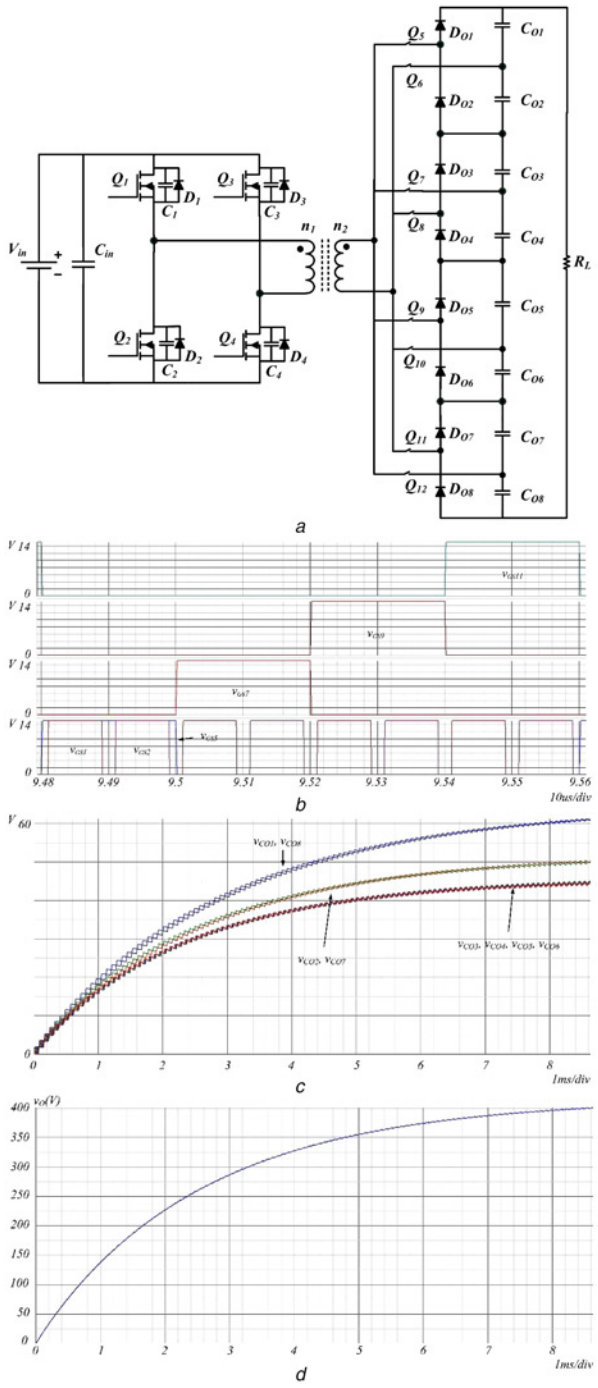


**Fig. 12** *Simulation results of the proposed 8-times PSFB converter*
*a* Circuit configuration
*b* Driving signals of switches $Q_1$, $Q_2$, $Q_5$, $Q_9$, and $Q_{11}$
*c* Voltage waveforms of output capacitors
*d* Output voltage

signals of main switches $Q_1$ and $Q_4$ is realised. Besides, it can also be observed that the voltage surges in $v_{pri}$ and $v_{sec}$ of the transformer occur each two times due the half-switching frequency, i.e. 25 kHz, in the proposed TDM control circuit. Fig. 11*b* illustrates the driving signal $v_{GS}$ and the voltage $v_{DS}$ for main switch $Q_4$. Since the $V_{DS}$ for main switch $Q_4$ decreases to zero and then $Q_4$ turn ON, ZVS in main switch $Q_4$ is achieved. Fig. 11*c* illustrates the voltage waveforms of the output capacitors. Fig. 11*c* indicates that the voltage ripples on the output capacitors ($C_{O1}$–$C_{O4}$) are well suppressed. The voltages of output capacitors are 48.4, 50.7, 51.1, and 51.3 V. It can be observed from Fig. 11*c* that almost same voltage for each capacitor voltage can be obtained. Therefore, 4-times voltage gain, the output voltage of 200 V as shown in Fig. 11*d*, can be realised by the proposed PSFB quadrupler converter. Fig. 11*d* also indicates that the conversion efficiency is 87.41% under an output power of 100 W. The overall efficiency of the proposed PSFB quadrupler converter is around 87–89% and might be lower than SVQR circuit [13] due to the four additional auxiliary switches ($Q_5$–$Q_8$) used in the proposed TDM control circuit. However, different primary-side circuits and rated voltages are adopted, the efficiency difference of these two circuits cannot be compared straightforwardly. Besides, voltage imbalance in the output capacitors would occur due to several capacitors in series. Fig. 11*c* shows that the maximum imbalance ratio for the output capacitors is 3.3%. If more accurate voltage for each output capacitor is required, an inner voltage control loop for each output capacitor can be designed and integrated into the PSFB quadrupler converter without modifying the proposed TDM control scheme. Since the rated output voltage as shown in Fig. 11*d* can be realised, the inner voltage control loop is not implemented here.

### 4.2 Simulation results

The proposed novel TDM control scheme can be extended to realise an *N*-times voltage rectifier and the simulation results for an 8-times voltage rectifier are shown here. Fig. 12*a* shows the circuit configuration of the proposed 8-times PSFB converter. Fig. 12*b* illustrates the driving signals of switches $Q_1$, $Q_2$, $Q_5$, $Q_7$, $Q_9$, and $Q_{11}$ for proposed novel TDM driving signals. Figs. 12*c* and *d* show the simulated voltages of the output capacitors and output voltage, respectively. From Figs. 12*c* and *d*, it can be observed that 8-times voltage gain, i.e. output voltage of 400 V, can be obtained. Consequently, the proposed rectifier and novel TDM control circuit can be extended effectively to construct an *N*-times voltage rectifier.

## 5 Conclusions

A voltage quadrupler rectifier with a novel TDM control scheme for high step-up converters was proposed in this paper. Based on the proposed TDM control scheme, two full-wave voltage doubler rectifiers can be combined to realise the proposed voltage quadrupler rectifier. The output voltage of the proposed rectifier is twice of half-wave and full-wave voltage doubler rectifiers; therefore, the turn ratio of transformer winding and the voltage stresses on the output capacitors and rectifier diodes of the proposed rectifier can be reduced. Diodes and capacitors with lower rated voltage can be adopted in the proposed rectifier. A PSFB converter was adopted in the primary side of the proposed voltage quadrupler rectifier to construct a PSFB quadrupler converter. Experimental results verified the validity of the proposed TDM control scheme for voltage quadrupler rectifiers. The extension of the proposed TDM control scheme for an 8-times voltage rectifier was also simulated in this paper. Simulation results revealed that the proposed TDM control scheme has great potential to be used in high step-up converters. Other issues such as integrating a dual boost converter into the proposed *N*-times voltage rectifier to realise a non-isolated high step-up converter and extension of the proposed TDM control scheme to design a bi-directional high step-up/step-down converter will be discussed and implemented in the future.

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