Accurate geometry scalable complementary metal oxide semiconductor modelling of low-power 90 nm amplifier circuits

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Abstract: This paper proposes a technique to accurately estimate radio frequency behaviour of low-power 90 nm amplifier circuits with geometry scalable discrete complementary metal oxide semiconductor (CMOS) modelling. Rather than characterising individual elements, the scheme is able to predict gain, noise and reflection loss of low-noise amplifier (LNA) architectures made with bias, active and passive components. It reduces number of model parameters by formulating dependent functions in symmetric distributed modelling and shows that simple fitting factors can account for extraneous (interconnect) effects in LNA structure. Equivalent-circuit model equations based on physical structure and describing layout parasites are developed for major amplifier elements like metal–insulator–metal (MIM) capacitor, spiral symmetric inductor, polysilicon (PS) resistor and bulk RF transistor. The models are geometry scalable with respect to feature dimensions, i.e. MIM/PS width and length, outer-dimension/turns of planar inductor and channel-width/fingers of active device. Results obtained with the CMOS models are compared against measured literature data for two 1.2 V amplifier circuits where prediction accuracy for RF parameters (S_{21}, noise figure, S_{11}, S_{22}) lies within the range of 92–99%.

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1 Introduction

During the evolution of integrated circuits, the noise content of complementary metal oxide semiconductor (CMOS) process was initially considered too high [1, 2] which made compound semiconductors (group III–V materials) preferable for achieving superior radio frequency (RF) characteristics [3–5]. However, rapid advancement and scaling down of CMOS technology, having started with an original intention of improving digital circuits, have allowed the development of low-power monolithic integrated circuits (MIC) for RF applications (low-power amplifiers, bandpass filters, on-chip antennas and correlators/mixers) [6–10]. RF features of active CMOS devices have been continually improving with >40 GHz unity gain frequencies being achieved by 180–90 nm transistors [11–13]. CMOS technologies also facilitate benefits like large manufacturing output, lower cost and compatibility with existing digital foundry [14]. An efficient way to further reduce fabrication overhead of CMOS circuits is to develop accurate RF models of its member elements [15–17]. It can significantly reduce the number of attempts (and hence masking cost) required to achieve desirable performance from a prototype transceiver. These models should be able to estimate frequency characteristics and RF behaviour of individual elements and complete circuits comprising power rail, bias supplies, active devices and passive RLC components.

Recent literatures have presented a number of modelling examples of RF CMOS elements [18–23]. In most cases, they have concentrated on characterising an individual component over a necessary frequency range. When these models are based on device physics, inclusion of detailed material properties can make them burdensome from a computational point of view. Models of 180 nm MOS varactor and capacitor have been proposed in [18] which can predict *Y*-parameters for up to 6 GHz. A distributed capacitor model which is able to estimate impedance matrix parameters has been verified in [19]. Modelling of CMOS power devices is discussed in [20] in relation to development of matching networks and trade-offs associated with power efficiency. Transistor modelling for RF design is also addressed in [21] in order to analyse frequency-dependent and thermal noise behaviour. The concept of design space exploration for on-chip inductors is introduced in [22] with the help of closed-form mechanisms. Development of expressions for various shapes of CMOS planar inductors has been the focus of [23].

This paper proposes a CMOS modelling technique for metal–insulator–metal (MIM) capacitors, spiral symmetric (SS) inductors, polysilicon (PS) resistors and bulk RF transistors (RFT) in order to estimate RF behaviour of low-power 90 nm amplifier circuits. The scheme exploits interdependency of layout parasites to simplify device expressions and reduces number of independent parameters through symmetric modelling. Effects extraneous to amplifier components (e.g. loss because of interconnects) are considered with the help of selected fitting factors. Equivalent-circuit model equations for associated parasites are derived on the basis of physical device structures. They are scalable with relevant geometric features and able to produce range of values needed in CMOS amplifier circuits. RF performance estimated by the models is compared with measured 90 nm data collected from the literature [24]. They are utilised to predict behaviour of two high-gain/overvoltage-protected C-band amplifiers which can manage 12.4–13.4 dB peak gain with low power (∼9 mW) and noise figure (NF) readings (2.7–2.9 dB). The results suggest that the modelling technique, which is based on parasitic models simplified by dependent functions, can accurately characterise RF performance of integrated amplifier architectures.

This paper is organised in the following way. Section 2 proposes CMOS MIM, SS, PS and RFT models and documents their behaviour in detail. Two high-gain and pulse-protected 1.2 V amplifier architectures are presented for testing of models in Section 3. RF parameters of complete low-noise amplifier (LNA) circuits are estimated with the modelling technique in Section 4 and verified against measured results. Finally, conclusions of the work are summarised in Section 5.

2 Modelling of CMOS elements

In this section, RF modelling is performed for active and passive CMOS components which are needed in nanoscale transceiver circuits. The models include appended RLC elements representing junction (depletion) capacitance, thermal resistive loss, substrate

loss, coil parasites, high-frequency effects and parasitic capacitance between active layer and substrate. Equivalent-circuit analyses are completed for MIM capacitor, PS resistor and octagonal SS inductor among passive devices.

Scalable model (SM) for active RFT is developed with the inclusion of extrinsic RC elements with defined device parameters. The models are employed to estimate measured behaviour of CMOS 90 nm amplifier circuits to verify the accuracy of RF modelling.

2.1 MIM capacitor

An MIM capacitor is often preferred for microwave front-end circuits over other forms of CMOS capacitors because of its quasi-linear behaviour against frequency and relatively high-quality factor [25]. It uses a strip of dielectric film (insulator) packed between two electrodes made with metal layers and has a range of up to 20 pF. It is widely used as a passive component for input–output matching circuits, signal coupling, power supply protection, resonance tanks and feedback connections in MICs [7, 8]. In a submicron amplifier architecture, it typically serves as a part of load and impedance matching network at RF input port. Study of the literature on CMOS amplifiers shows their on-chip capacitors having values in the 0.08–8 pF range [24, 26–30], indicating a possibility of coverage with an appropriate model of MIM capacitor.

The proposed two-port RC model of an MIM capacitor is presented in Fig. 1. In this circuit, C_{mim} is the primary capacitive element created by placing two conductors on both sides of an insulating layer. Dielectric resistive loss is accounted for with a series component R_{ins} and parasites associated with top and bottom electrodes are represented by R_{m1} and R_{m2}. Four shunt elements are included as a part of distributed modelling to simulate substrate effect. They are indicative of parasites existing between top (C_{pr11}, C_{pr12}) and bottom (C_{pr21}, C_{pr22}) metal layers and body. No resistive element is included in the shunt path as thermal substrate loss is not considered for the MIM model. SM equations are developed in terms of length (L_{mim}) and width (W_{mim}) of metal plates in the MIM structure. Empirical expressions which are able to describe model behaviour against variation of structure geometry take the form of

$$R_{m1} = \frac{20.35}{L_{\text{mim}} W_{\text{mim}}} - \frac{1.67}{(\ln L_{\text{mim}})^2 (\ln W_{\text{mim}})^2}\ \Omega \tag{1}$$

$$R_{m2} = 0.67 a_1 \left[\frac{125.9}{(L_{\text{mim}})^{0.5} W_{\text{mim}}} - \frac{230.3}{L_{\text{mim}} W_{\text{mim}}}\right] \Omega \tag{2}$$

$$R_{\text{ins}} = 0.5 R_{m2} \tag{3}$$

$$C_{\text{mim}} = 3.71\text{e}^{-3} + 0.5(W_{\text{mim}} + L_{\text{mim}}) + 2.05(L_{\text{mim}} W_{\text{mim}}) fF \tag{4}$$

$$C_{\text{pr11}} = C_{\text{pr12}} = \frac{1}{3}\left[0.972 + 0.267(W_{\text{mim}} + L_{\text{mim}})\right] \left[+0.024(L_{\text{mim}} W_{\text{mim}})\right] fF \tag{5}$$

$$C_{\text{pr21}} = C_{\text{pr22}} = 0.5 C_{\text{pr11}} \tag{6}$$

Here L_{mim} and W_{mim} are expressed in μm and a_1 is fitting parameter. When the model is included in a complete circuit, assigning an optimised value to this factor can account for interconnect loss and improve consistency of RF results. R_{ins}, C_{pr21} and C_{pr22} are defined as dependent parameters (with respect to R_{m2} and C_{pr1}) to simplify device expressions and reduce model complexity without compromising on estimation accuracy. In this model, L_{mim} resides in the range of 5 ∼ 60 μm and W_{mim} has a wider dimension coverage of 5 ∼ 100 μm. If $L_{\text{mim}} = 5$ μm for the model, variation of W_{mim} within 5 ∼ 100 μm achieves MIM capacitance values of 0.05–1.1 pF. As C_{mim} scales directly with L_{mim}, changing the latter to 12 μm modifies this range to 0.43–8.3 pF. Overall coverage of the model can produce 0.05–12 pF passive elements which are consistent with size of LNA capacitors and reported data on insulator capacitance [31]. The shunt parasites used in the model $\left(C_{\text{pr11}} \sim C_{\text{pr22}}\right)$, which are coupled with the substrate, have values of 5–180 fF.

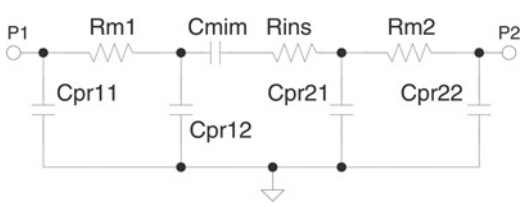

Fig. 1 *Distributed RC model of an MIM capacitor*

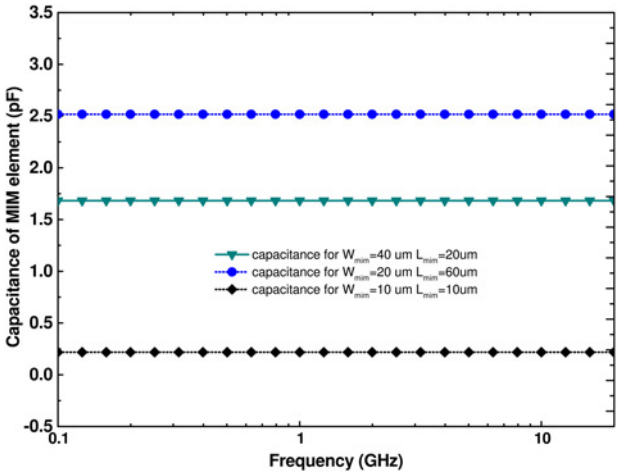

Fig. 2 *Input capacitance of proposed MIM model samples*

Fig. 2 illustrates capacitance produced by different sizes of the model over the observed frequency range of 0.1–20 GHz. To obtain an assessment of models's power efficiency, its quality factor (Q_{mim}) can be approximated with the following equation

$$Q_{\text{mim}} = \frac{1}{\omega(R_{\text{ins}} + R_m)(C_{\text{total}})} \tag{7}$$

when plotted as a function of device geometry and frequency in Fig. 3, Q_{mim} achieves values of 10–390 between 1 and 10 GHz.

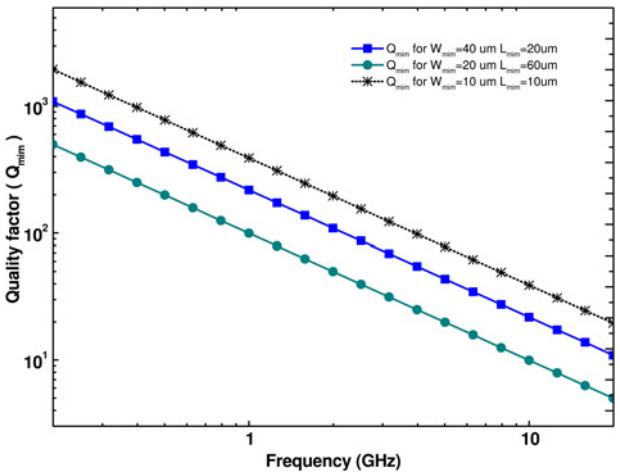

Fig. 3 *Quality factor of MIM capacitors plotted against frequency*

2.2 PS resistor

PS resistors are considered suitable for nanoscale RF circuits as they have smaller parasitic components as compared with other on-chip resistors. They are compatible with BiCMOS and CMOS processes and offer up to 500 Ω/square sheet resistance in shielded condition [32]. The resistivity of the structure is controlled by amount of doping in poly layers and grain boundaries present in deposits. Unlike diffused (MOS) resistors, its inherent substrate parasites are not dependent on bias voltages. PS layers occupy a relatively smaller area in most technologies and their temperature dependence is weaker than well and implanted resistors. Metal resistors are often dominated by thickness variation which is not the case for poly resistors and, as a result, amount of conductivity modulation remains minimal. In addition, they are not dominated by piezoresistive effect and can produce a wide range of small and large values [33–35].

Fig. 4 shows the PS resistor model employed in this Letter. It has been developed to cover the range of resistance (0.05–20 kΩ) used in reported LNA circuits [26, 27, 28–30]. It utilises a double-T RC network where resistive contribution of the poly layer is represented by R_{poly}. Peripheral resistance at the two ends of the deposit are accounted with R_{ct1} and R_{ct2}. R_{sub} is included in the model to represent resistive loss in oxide and substrate. Parasitic capacitors associated with a polysilicon layer and its oxide base are responsible for C_{pari} and C_{paro}. An RCR branch on both sides of R_{poly} creates the two T circuits of the model. Symmetry is maintained with the placement of R_{ct}, R_{sub} and C_{par} elements (with respect to R_{poly}) to reduce number of independent parameters. These components are scalable with width and length of the deposited PS layer (W_{poly} and L_{poly}). Analytical model equations for the equivalent circuit are expressed as

$$R_{poly} = \frac{0.9L_{poly}}{3.389(W_{poly}) - 0.125}\ \text{k}\Omega \tag{8}$$

$$R_{ct1} = R_{ct2} = 591.2\left[\exp\left(\frac{0.076}{W_{poly}}\right) - 1\right]\Omega \tag{9}$$

$$R_{sub_{1/2}} = \frac{16.48}{L_{poly}W_{poly}} - \frac{30.49}{(L_{poly})^2\exp(W_{poly})}\ \text{k}\Omega \tag{10}$$

$$C_{pari1} = C_{pari2} = 0.5045L_{poly} + 0.7162\left(\frac{W_{poly}}{\sqrt{L_{poly}}}\right)\text{fF} \tag{11}$$

$$C_{paro1} = C_{paro2} = 2C_{pari1} \tag{12}$$

In these equations, L_{poly} and W_{poly} are expressed in a unit of μm and C_{paro} is defined as a dependent parameter to simplify the model. The smaller parasite R_{ct} is scaled with W_{poly} in the design range. With a 1 μm poly width, if L_{poly} is increased from 1 to 100 μm the model can achieve an effective resistance of 0.3–28 kΩ. In comparison, if L/W ratio of the structure is reduced with increasing W_{poly} (1–60 μm, L_{poly} = 5 μm), overall poly resistance drops from 1.4 kΩ to ~25 Ω. Substrate resistive components of the model (R_{sub}) offer moderate values and capacitive parasites are smaller as compared with their counterparts in the MIM model. Table 1 presents calculated total resistance of the PS model as a function of device geometry and its frequency-dependent resistive profiles are illustrated in Fig. 5.

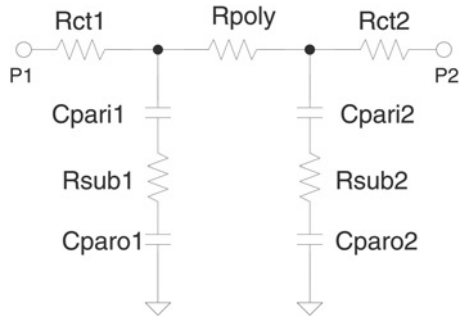

Fig. 4 *Proposed double-T model of PS resistor*

Table 1 Model resistance as a function of device geometry

W_{poly}, μm	L_{poly}, μm	R_{model}, Ω
0.5	5	3082.57
1	10	2860.75
5	20	1090.12
5	50	2695.11
10	90	2408.59
30	15	136.26
10	50	1342.56

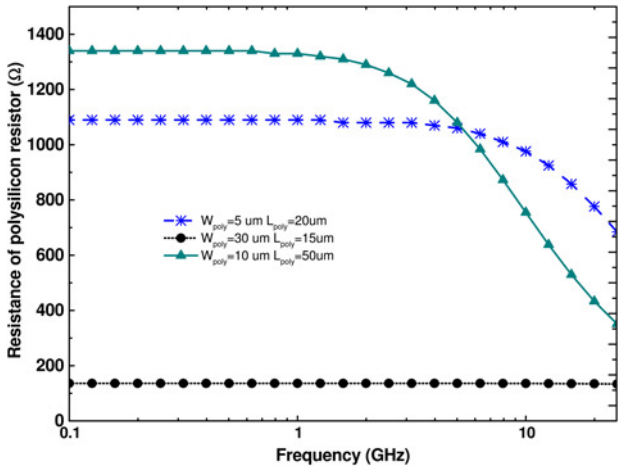

Fig. 5 *Frequency profiles of PS resistor models*

2.3 SS inductor

Spiral inductors play a critical role in determining RF performance of CMOS transceiver circuits [36]. They are primarily employed as part of load banks, oscillators, band-pass filter, feedback network and port matching circuits in CMOS applications [7, 26, 27]. The spiral has to produce necessary reactance and reasonable quality factor simultaneously for ensuring optimum RF circuit behaviour. An octagonal structure is often selected to reduce on-chip area requirement which is further facilitated with symmetric realisation of two halves of a spiral. As cost of tuned circuits is directly correlated with spiral inductors, their modelling also plays a role in limiting manufacturing overhead.

The equivalent-circuit model of a spiral inductor is illustrated in Fig. 6 which employs cascaded networks to represent different sections (halves) of a planar symmetric spiral. Each half is modelled with a pi-shaped RLC network including elements standing for spiral parasites. L_{shf} is generated by the spiral sections and mutual coupling between coil parts is modelled with the coefficient K_{hf12}. Thermal loss in the spiral is represented with R_{shf} and peripheral resistance of each section (generated by underpass, contacts) creates the R_{ph} components. These model parameters are expressed in terms of outer diameter of the spiral (D_{sind}) and number of turns in the planer coil (N_{sind}). Other characterising features like gap between spiral lines are assumed to have constant values.

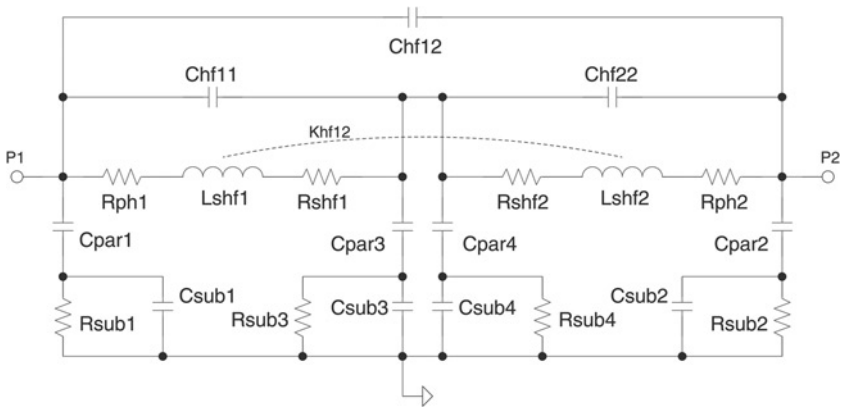

Fig. 6 *RF model of SS inductor*

Capacitance between lines of each spiral section is modelled with C_{hf11} and C_{hf22}. Similarly, parasites created between different spiral sections are responsible for C_{hf12}'s inclusion. Components which link each coil section to the substrate are modelled through *h*-circuits initiated with C_{par}. R_{sub} and C_{sub} stand for elements which are responsible for overall substrate loss. The model assumes that there is no centre-tap connection to the geometric centre point of a spiral. Its planar symmetric structure is adopted in order to avoid use of multiple single-ended coil parts to achieve symmetry. Model equations for the spiral inductor take the form of

$$R_{\text{ph1}} = R_{\text{ph2}} = 0.11(N_{\text{sind}} - 1)\,\Omega \tag{13}$$

$$C_{\text{hf11}} = C_{\text{hf22}} = 1.378 - 0.1D_{\text{sind}} + N_{\text{sind}}(0.658 + 0.067D_{\text{sind}})\,\text{fF} \tag{14}$$

$$C_{\text{hf12}} = 7.59 + 0.067D_{\text{sind}}\text{fF} \tag{15}$$

$$R_{\text{shf1}} = R_{\text{shf2}} = 397 + 0.152D_{\text{sind}} + (6.565D_{\text{sind}} - 408)N_{\text{sind}}\ \text{m}\Omega \tag{16}$$

$$L_{\text{shf1}} = L_{\text{shf2}} = x_1(D_{\text{sind}})^{x_2} + x_3\text{n}H \tag{17}$$

$$\begin{aligned}\{x_1,\ x_2,\ x_3\}_{(N_s=1)} &= \{0.375\ m,\ 1.087,\ -16.15\ m\}\\ \{x_1,\ x_2,\ x_3\}_{(N_s=2)} &= \{0.774\ m,\ 1.168,\ -70.4\ m\}\\ \{x_1,\ x_2,\ x_3\}_{(N_s=3)} &= \{2.45\ m,\ 1.075,\ -228.2\ m\}\end{aligned} \tag{18}$$

$$K_{\text{hf12}} = 0.952 + 2.38\ mN_{\text{sind}} + 0.0379\text{e}^{-3}D_{\text{sind}} \tag{19}$$

$$C_{\text{par1}} = C_{\text{par2}} = 0.164 + N_{\text{sind}}(0.274 - 0.795N_{\text{sind}} + 0.061D_{\text{sind}}) + 4.52\text{e}^{-3}D_{\text{sind}}\text{fF} \tag{20}$$

$$C_{\text{par3}} = C_{\text{par4}} = 0.208 + N_{\text{sind}}(0.71 - 1.86N_{\text{sind}} + 0.142D_{\text{sind}}) + 0.0123D_{\text{sind}}\text{fF} \tag{21}$$

$$C_{\text{sub1}} = C_{\text{sub2}} = 0.5C_{\text{par1}} \tag{22}$$

$$C_{\text{sub3}} = C_{\text{sub4}} = 0.5C_{\text{par3}} \tag{23}$$

$$R_{\text{sub1}} = R_{\text{sub2}} = x_4(D_{\text{sind}})^{x_5} + x_6\Omega \tag{24}$$

$$\begin{aligned}\{x_4,\ x_5,\ x_6\}_{(N_s=1)} &= \{83.08\ k,\ -1.087,\ 15.09\}\\ \{x_4,\ x_5,\ x_6\}_{(N_s=2)} &= \{168.5\ k,\ -1.368,\ 28.72\}\\ \{x_4,\ x_5,\ x_6\}_{(N_s=3)} &= \{92.26\ k,\ -1.23,\ 16.79\}\end{aligned} \tag{25}$$

$$R_{\text{sub3}} = R_{\text{sub4}} = x_7(D_{\text{sind}})^{x_8} + x_9\Omega \tag{26}$$

$$\begin{aligned}\{x_7,\ x_8,\ x_9\}_{(N_s=1)} &= \{35.61\ k,\ -1.087,\ 6.468\}\\ \{x_7,\ x_8,\ x_9\}_{(N_s=2)} &= \{72.21\ k,\ -1.368,\ 12.31\}\\ \{x_7,\ x_8,\ x_9\}_{(N_s=3)} &= \{39.54\ k,\ -1.23,\ 7.198\}.\end{aligned} \tag{27}$$

Symmetric circuit representation helps to reduce number of independent model parameters for the inductor and dependent functions are used for the C_{sub} elements to allow model simplification. As reported, low-power RF LNAs (<6 dB NF) employ very small inductors for matching and loading (~0.1–4 nH) [24, 26, 27, 29–30], the model adopts a range of 100–300 μm and 1–3 for D_{sind} and N_{sind}, respectively, which allows it to generate necessary effective reactance for low-noise circuits.

Fig. 7 presents inductor quality factors (Q_{sind}) obtained with the proposed symmetric spiral model. It shows that peak Q_{sind} values of 7–15 can be achieved with the model in the design domain, whereas its peak-Q frequency covers a range of 4–30 GHz. To estimate Q factors, the inductor model is included in a two-port circuit which can predict Q_{sind} and effective inductance L_{sind} with the help of imaginary and real parts of Y and Z parameters

$$Q_{\text{sind}} = -\frac{Y_{11}(I)}{Y_{11}(\Re)} \tag{28}$$

$$L_{\text{sind}} = \frac{Z_{11}(I)}{2\pi f} \tag{29}$$

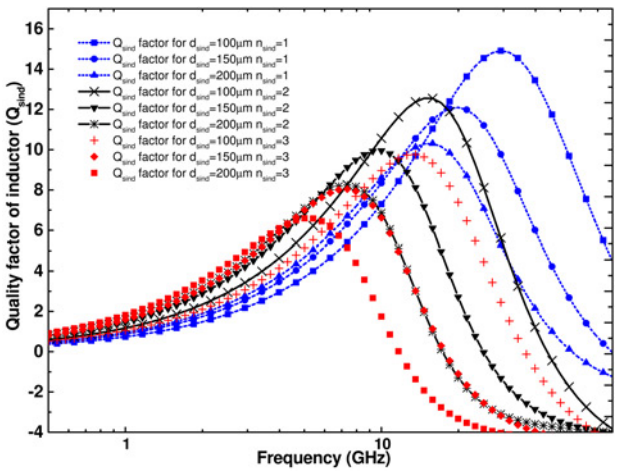

Fig. 7 *Quality factors of the SS inductor model*

Table 2 documents sample values of calculated effective model inductance (L_{sind}) as a function of coil geometry.

2.4 Scalable RFT model

This Letter uses a SM for 90 nm RFTs which have base threshold voltages around 300 mV. Limitation of active device modelling is a chief concern in maintaining accuracy of RF circuit simulation. A typical compact model of a MOS device is usually implemented with parameters extracted at low frequencies [20]. However, RF modelling suitable for high-frequency CMOS amplifier circuits needs to include the effect of various junction parasites. This Letter realises a SM for an RFT which is presented in Fig. 8 and defined for $W_{sm} = 25$–300 µm, covering typical device width employed in transceiver amplifier circuits [26–29]. It is built on a BSIM4 90 nm MOS model core where C_{gsi}, C_{gdi}, C_{sbi} and C_{dbi} represent inherent junction parasites [37]. The model core is obtained including the effects of asymmetric/bias-dependent modelling, charge partition, gate-induced drain leakage, gate dielectric tunneling current, high-speed considerations and asymmetric source/drain junctions. The overall SM is developed as a function of device width (W_{sm}) which can be obtained by multiplying number of fingers (NF) with unit finger dimension. It adopts small external resistive elements connected to transistor terminals (R_{ge}, R_{se}, R_{de} and R_{be}) to account for excess losses not predicted by the core (as the device is placed in an integrated architecture). C_{gse} is because of high-frequency fringe parasites associated with MOS gate and source terminals in an LNA circuit. C_{dbe} performs a similar function for drain and body of the device. Core and external sections of the SM are designated as SM(in.) and SM(ex.). The expressions of external model parameters are as follows

$$R_{se} = R_{se} = a_2 \times \frac{8.15}{7.88\,m + (0.242W_{sm}/5)}\ \Omega \tag{30}$$

$$R_{de} = a_2 \times \frac{9.85}{(0.252W_{sm}/5) - 0.0183}\ \Omega \tag{31}$$

$$R_{ge} = a_2 \times \frac{18.6}{(2.154W_{sm}/5) - 10.379}\ \Omega \tag{32}$$

$$C_{gse} = 5.33[0.2093W_{sm} - 0.0489]\left(\frac{W_{sm}}{10NF}\right)\ \text{fF} \tag{33}$$

$$C_{dbe} = 0.0176[0.118W_{sm} + 0.409)]\left(\frac{W_{sm}}{10NF}\right)\ \text{fF} \tag{34}$$

In these equations, W_{sm} has a unit of µm and a_2 is included as a fitting factor which can model the effect of interconnects associated with a transistor as it is placed in a CMOS circuit.

In the next section, the proposed models are utilised to estimate the behaviour of two 90 nm C-band low-power amplifiers and modelled results are compared against measured microwave parameters to verify prediction accuracy and consistency of the modelling technique.

Table 2 Effective inductance of the SS inductor model

D_{sind}, µm	N_{sind}	L_{sind}, nH
300	1	0.68
200	2	1.21
300	2	2.12
200	3	1.69
300	3	3.58

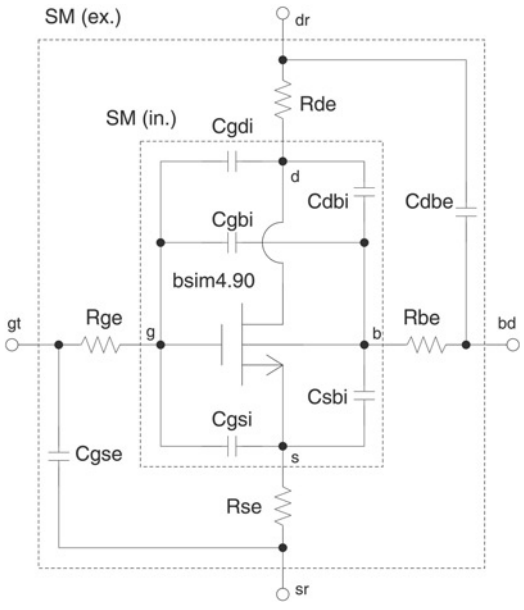

Fig. 8 *SM of a RF transistor*

3 Modelling of 90 nm amplifiers

The objective of the RF models developed in this paper is to accurately estimate microwave behaviour of transceiver amplifier circuits. With that view, the models are employed to analyse the performance of two 90 nm CMOS low-power amplifier (LNA) circuits with an RF simulator. The architectures consist of active and passive elements which fall within the models' dimension range. Their topologies are illustrated with the help of Figs. 9*a* and *b*. These structures are suitable for implementing low-dissipation low-NF front-ends with a scaled supply rail. The first LNA aims to provide high-power gain and port isolation, whereas the second architecture includes passive on-chip protection against electrostatic discharge (ESD, which becomes a design issue as gate oxides are scaled down). Fig. 9*a* shows back-to-back common source (CS) and common gate stages which realise a cascode structure with two transistors. These devices are of identical size ($W = 110$ µm) and powered by a main supply rail of 1.2 V. The input CS transistor (T_1) is biased with a smaller gate supply (V_{gate}). Overall dc current drawn from V_{dd} is 8.1 mA which results in a power dissipation of 9.7 mW for the amplifier. The LNA's input port is matched to a preceding component (of 50 Ω) with an input coupling element C_{ip1} and a gate inductor L_{m1} which cancel the capacitive part of input impedance. Additionally, adjustment of $Z_{in}(\Re)$ is managed with a small source inductor L_{dg1} which introduces degeneration of gain [38]. The cascode device T_2 is biased with the supply rail (V_{dd}) and a CC circuit at RF_{out} port (C_{op1} and C_{op2}) forms the load with L_{tank1} and manages output matching.

Fig. 9*b* presents a second 90 nm architecture which incorporates reactive and active protection circuits into the cascode amplifier. Its core transistors (T_3 and T_4) are identical in size and drain a similar amount of power from the supply rail (9.7 mW) as compared with the first amplifier. It also includes a large isolating resistor (R_{gate2}) to deliver V_{gate} to the input of T_3 and houses a supply capacitor (C_{sup2}) to protect the circuit from ripples that may occur on the voltage rail. The inductor of its input protection circuit (L_{pr1}) cancels parasites associated with RF_{in} port and its own resistive component makes a parallel circuit with matched input impedance. L_{pr1} protects the gate oxide of the input driving transistor by allowing large voltage drops across it in response to ESD pulses at port RF_{in}. This allows excess voltage at the gate of T_3 to be kept below the

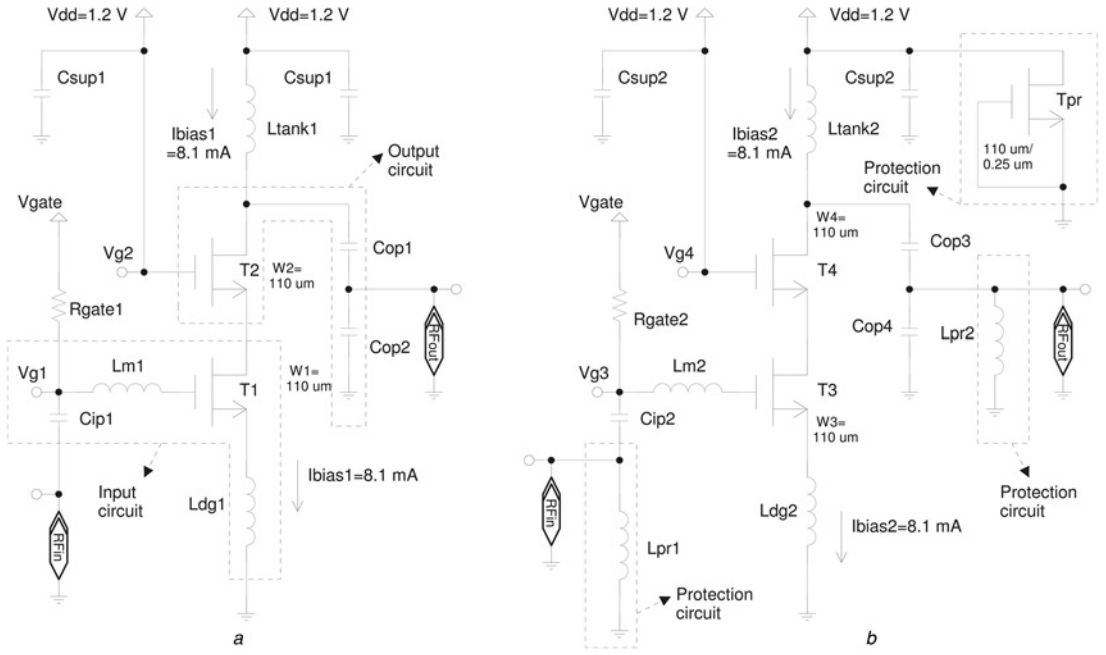

Fig. 9 *CMOS circuits analysed with RF models*
a Matched cascode low-power amplifier
b Overvoltage-protected cascode amplifier

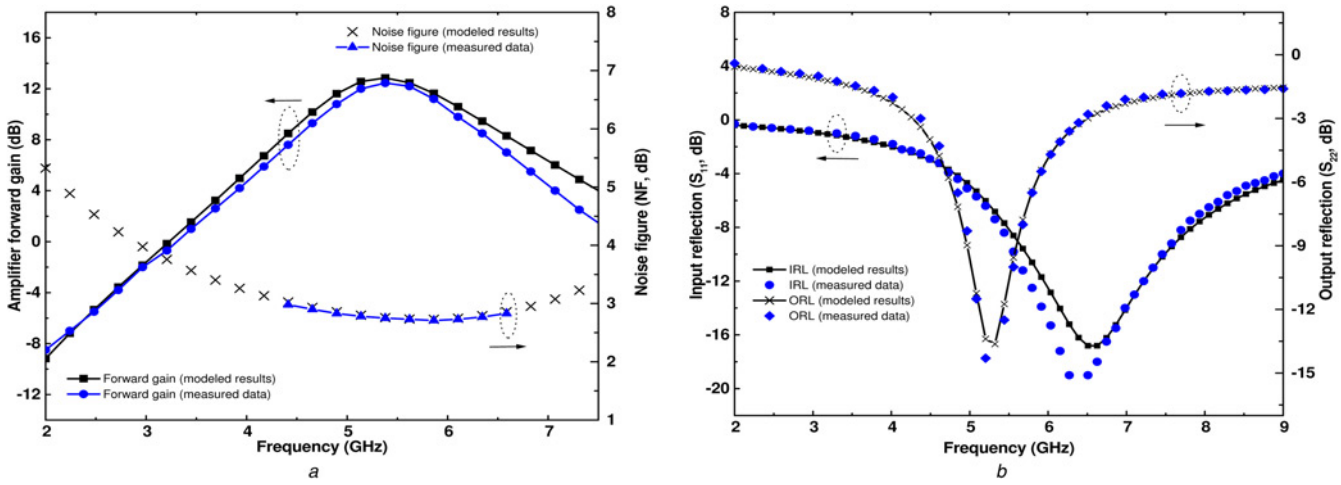

Fig. 10 *Comparison in terms of*
a Forward gain, NF
b Input/output reflection between modelled and measured results of the first amplifier

breakdown level. L_{pr2} introduces overvoltage protection in a similar fashion for the output matching port. A relatively long channel gate–source shorted device T_{pr} ($L = 0.25$ µm), which is not a part of the RF circuit, is connected to the V_{dd} rail to safeguard it from discharge pulses. Input and output matching circuits of the overvoltage-protected amplifier have similar component dimensions like the first cascode LNA. Measured data of the two 90 nm amplifiers (indicative of their RF performance) are collected from [24] to compare them with results obtained with the proposed SMs. The outcome of comparison between the two sets of data is presented in the next section.

4 Comparison of RF performance

Modelled and measured RF parameters of the first 90 nm low-power low-NF amplifier are illustrated with the help of Figs. 10*a* and *b*. Fig. 10*a* demonstrates noise and gain figures where the modelled S_{21} (forward power gain) curve has a peak of 12.8 dB at 5.4 GHz with a 3 dB bandwidth (BW) of 4.61–6.23 GHz. Noise figure (NF) of the amplifier remains below 3.6 dB within the C-band (4–8 GHz). BW limited NF has a centred minimum of 2.73 dB which is raised to 2.77 and 2.96 dB at the two edges of BW. Gain performance assessed from measured data is consistent with modelled results with a peak gain of 12.4 dB (a difference of 3.2%) and a BW of 4.7–6.1 GHz. In addition, measured NF has a reading of 2.70 dB at peak gain frequency and is indicative of greater model accuracy (matching: 98.9%). Reflection loss at the amplifier ports is demonstrated in Fig. 10*b* for S, C and X band frequencies. In case of input reflection (S_{11}), modelled and measured data are better than −3.4 and −3.7 dB over their message BWs, respectively. BW limited S_{22} (output reflection loss) is lower than −3.8 and

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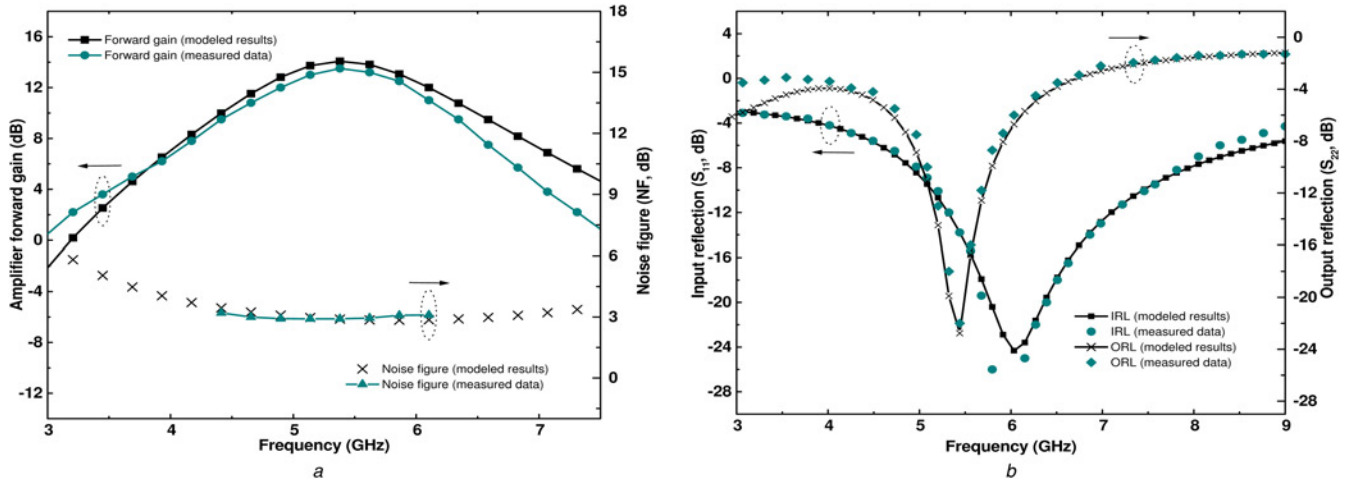

Fig. 11 *Comparison between modelled and measured results of the overvoltage-protected LNA with respect to*
a Forward gain, NF
b S_{11}, S_{22}

Table 3 Summary of estimation accuracy of the modelling technique

RF parameters	Model accuracy for LNA_1, %	Model accuracy for LNA_2, %
forward gain	96.8	96.3
NF	98.9	96.9
input reflection	91.9	98.5
output reflection	95.0	95.6

−4.0 dB for the two sets of data which show mutual correspondence around the centre frequency.

Figs. 11*a* and *b* document RF results for the second C-band 90 nm amplifier with reactive–active protection circuits. It achieves a better input matching performance than the first LNA which leads to a marginally higher forward gain. The modelled amplifier circuit has a S_{21} of 13.9 dB at 5.53 GHz, whereas the measured peak of 13.4 dB is located at 5.5 GHz (matching: 96.3%). Measured NF for the overvoltage-protected circuit is 2.95 dB at peak gain frequency, whereas centred NF for the modelled circuit has a value of 2.86 dB (error of 3.1%). Range of BW for the front-end amplifier is not significantly influenced with the inclusion of pulse-protection elements. For both measured and simulated data, NF remains better than 3.2 dB over circuit BW. In case of output reflection loss (S_{22}), the two curves follow each other over the 4–9 GHz frequency range. S_{22} approaches −19 dB near operating point and stays below −4.5 dB over both BWs. Correspondence between the two sets of results is also maintained for input return loss (S_{11}) with measured and modelled readings near 5.5 GHz being registered as −14.4 and −14.6 dB, respectively. Summary of estimation accuracy of the modelling technique at centre frequency (gain, NF) and over BW (reflection loss) is provided in Table 3 for RF parameters of the two amplifier architectures.

On the basis of these results, it can be said that the proposed CMOS modelling scheme, despite being based on simple parasitic models, is able to accurately estimate RF characteristics of integrated transceiver amplifier circuits.

5 Conclusions

An accurate modelling technique of low-noise CMOS amplifier circuits comprising active/passive components and bias/gate supplies is presented in this paper. The scheme minimises number of required parameters by symmetric modelling, simplifies model expressions by exploiting interdependency of parasites and includes simple fitting factors in selected models to replicate effect of extraneous losses. It can be scaled with feature sizes of RLC and transistor elements and incorporates parasites generated from layout considerations. The models have been tested with two 90 nm low-power amplifier topologies where modelled results (NF, gain) have errors lower than 3.5% for integrated circuits. Analytical scalable equations capable of device characterisation are derived for CMOS elements (SS planar inductors, RF devices, MIM capacitors and PS resistors) needed in a front-end amplifier architecture. Figures of merit of modelled circuits are compared against measured literature data which show good accuracy for the technique.

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7 References

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