Capacitive digital-to-analogue converters with least significant bit down in differential successive approximation register ADCs

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Abstract: This Letter proposes a least significant bit-down switching scheme in the capacitive digital-to-analogue converters (CDACs) of successive approximation register analog-to-digital converter (ADC). Under the same unit capacitor, the chip area and the switching energy are halved without increasing the complexity of logic circuits. Compared with conventional CDAC, when it is applied to one of the most efficient switching schemes, V_{cm}-based structure, it achieves 93% less switching energy and 75% less chip area with the same differential non linearity (DNL)/integral non linearity (INL) performance.

1 Introduction

The capacitive digital-to-analogue converter (CDAC) in the feedback of successive approximation register (SAR) ADC performs the binary searching of the closest digital representation to the sampled input signal during the conversion process. Conventionally, a binary weighted capacitor array (BWA) is used [1]. In differential implementations, symmetrical switching on the positive and negative capacitor arrays is widely adopted to guarantee a constant common-mode (CM) voltage at the inputs of the comparator. It is noted that the CM voltage variation caused by the least significant bit (LSB) switching is the least, an asymmetrical switching on the LSB is proposed for differential DACs in this manuscript. In this scheme, the LSB capacitors only switch down, never up, and thus called as 'LSB down' scheme. This manuscript explains the usages on the ideas of 'LSB down' so that it saves the switching energy and chip area. When it is applied to one of the highest energy efficient V_{cm}-based [2] structure, it achieves even higher efficiency. For the symmetrical switching, any variance on the V_{cm} does not affect the resolution for the differential architecture with good CM rejection. For the LSB transition, the variance and noise on V_{cm} does introduce variances, however, with the least magnitude.

2 Proposed CDACs with LSB down

First, let us look at the basic case with the modification on the LSB switching in the conventional differential BWA DAC as illustrated in Fig. 1 using 2 bit examples. There are two capacitor arrays (positive and negative) in these differential structures. In the proposed scheme, to determine the LSB, only one unit capacitor from either the positive or negative arrays, not from both arrays, switches. This leads to a reduction of the total capacitance by half compared with the conventional approach. As a result, the averaged switching energy is nearly halved.

When LSB-down scheme is applied to one of the best energy efficient CDACs, namely V_{cm}-based [2], the energy efficiency gets doubled. Fig. 2 describes the difference with 3 bits examples. Both switching energy and area are reduced by at least 50%. When it comes into implementation, the switching network, number of cycles and logic circuit remain almost the same as in the original approach, except the tiny modification on switching of the unit capacitor.

To find out the switching energies (E_{up} and E_{dn}) for the 'up' and 'down' transitions in each capacitor array for the differential configuration, the deduction for the second conversion step in Fig. 1 can be followed as [3–5]

$$E_{up}\left[\frac{V_{ref}}{2}\rightarrow\frac{3V_{ref}}{4}\right]=V_{ref}\left(\text{net charge from } V_{ref}\right)$$
$$=V_{ref}\left[\frac{3C_0V_{ref}}{4}-\frac{2C_0V_{ref}}{4}\right]=\frac{C_0V_{ref}^2}{4} \quad (1)$$

$$E_{dn}\left[\frac{V_{ref}}{2}\rightarrow\frac{V_{ref}}{4}\right]=V_{ref}\left[\frac{2C_0V_{ref}}{4}+\frac{3C_0V_{ref}}{4}\right]=\frac{5}{4}C_0V_{ref}^2 \quad (2)$$

So

$$E[2]=E_{up}\left[\frac{V_{ref}}{2}\rightarrow\frac{3V_{ref}}{4}\right]+E_{dn}\left[\frac{V_{ref}}{2}\rightarrow\frac{V_{ref}}{4}\right]$$
$$=\frac{3}{2}C_0V_{ref}^2 \quad (3)$$

where the index i represents the ith conversion step ($i=1, 2, \ldots, N$ for N bit example). It is noted that the 'down' transition here is assumed to switch the two capacitors simultaneously. Similarly, steps can be applied to find out the switching energies for all the transitions as indicated in Figs. 1 and 2. The waveform V_P and V_N at the output of differential CDAC is illustrated in Fig. 3.

3 Simulation results on switching energy

The averaging switching energies have been summarised in Table 1 and behaviour simulation plots are shown in Fig. 4. Additionally, a set-to-down [3] DAC is also included for comparison. Since the capacitors in set-to-down are not symmetrically switching during the conversion, it is not valid for applying LSB-down scheme. The digital numbers next to the dotted lines represent the normalised average switching energies for different DACs with the assumption that the input signals are distributed with identical probabilities. The energies are about halved when the LSB-down scheme is applied to the conventional BWA and the V_{cm}-based DACs. Note that when this scheme is applied to the V_{cm}-based, the V_{cm} is $V_{ref}/2$. If there is any fluctuation on V_{cm}, it only affects the resolution on the LSB. Although the input CM voltage for the comparator is varying during the comparison on the LSB, it is not problematic because the variation is the smallest at this moment. On the other hand, the V_{cm}-based structure with LSB down is 50% more efficient than the one without LSB down.

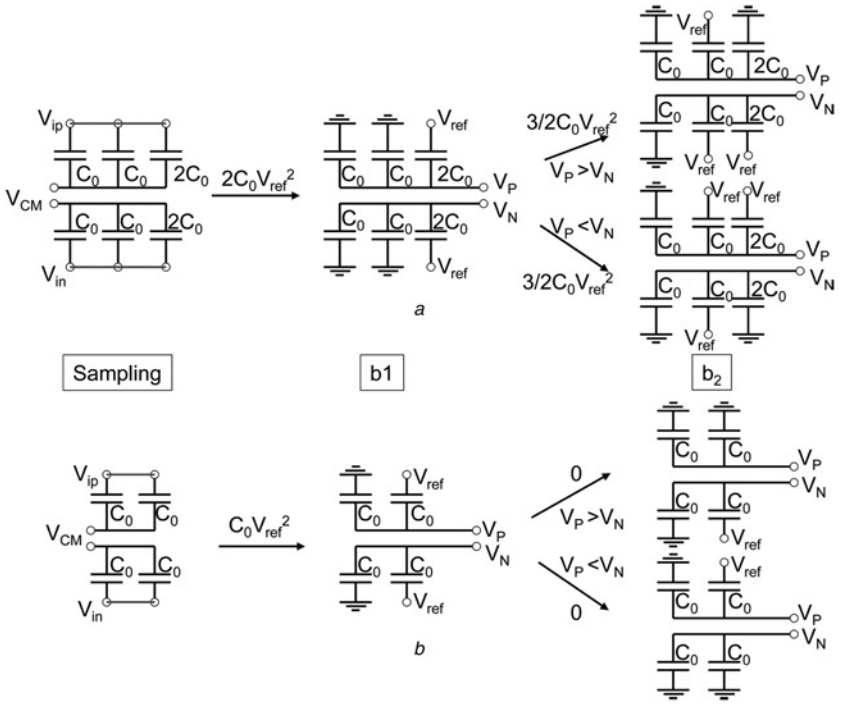

Fig. 1 *Comparison on BWA and BWA employing LSB down (2 bit example); V_P and V_N are outputs of the DAC to the comparator. The energy taken from V_{ref} in each switching step is marked near the corresponding arrow*
a BWA
b BWA with LSB down

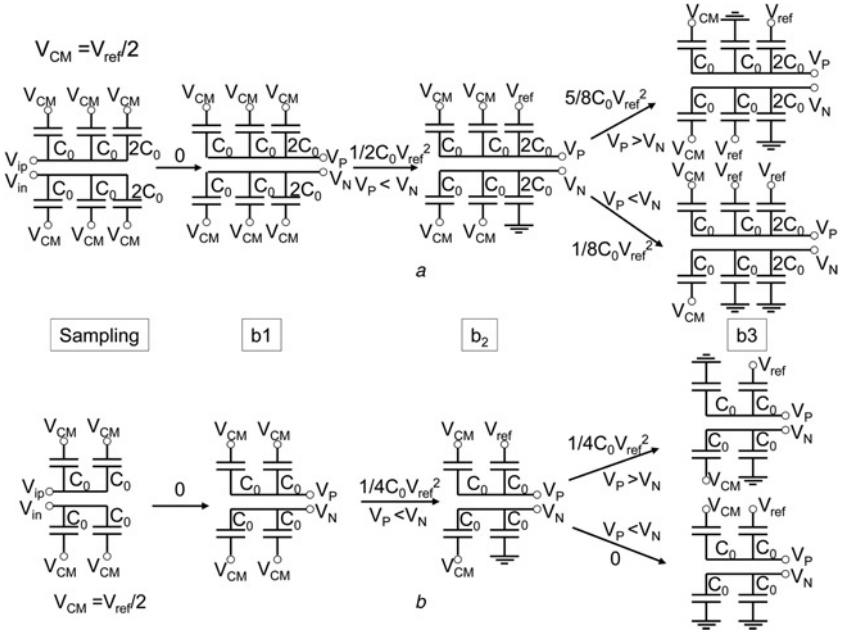

Fig. 2 *Comparison on*
a V_{cm}-based
b V_{cm}-based employing LSB down (3 bits example)

4 INL and DNL performance

Assume that the variation in unit capacitors of the DACs has a Gaussian distribution $[N(0, \sigma_0^2)]$, where σ_0 is the standard deviation of unit capacitor matching. The minimum unit capacitor is typically limited by the matching requirement rather than thermal noise requirement if we do not consider the mismatch calibration. Therefore the INL and DNL requirement for an 'N'-bit resolution SAR ADCs can be deduced from

$$V_{\mathrm{DAC}}(n) = \frac{\sum_{i=0}^{N-1}(C_i + \Delta C_i)b_i}{C_{\mathrm{T}}} V_{\mathrm{ref}} \tag{4}$$

$$\mathrm{DNL}(n) = V_{\mathrm{DAC}}(n-1) - V_{\mathrm{DAC}}(n) \tag{5}$$

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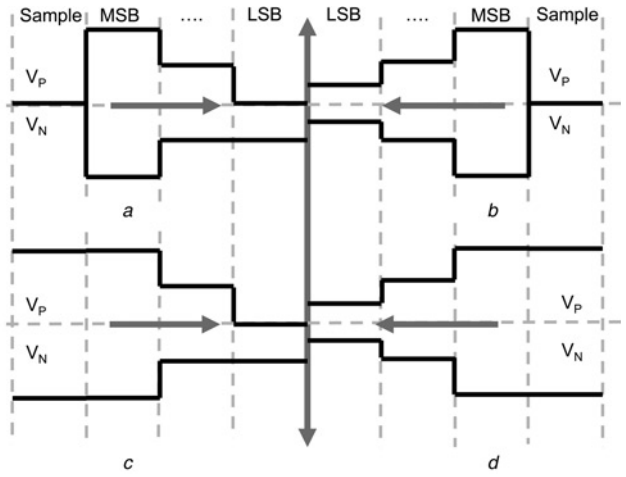

Fig. 3 *Waveform of V_P and V_N on*
a BWA with LSB down
b BWA
c V_{cm}-based with LSB down
d V_{cm}-based (3 bits example)

$$\mathrm{INL}(n) = V_{\mathrm{DAC}}(n) - V_{\mathrm{DAC\_ideal}}(n) \tag{6}$$

where C_T is the total capacitance, n is the corresponding digital codes for the output of DAC, C_i is the capacitance in the CDAC with the mismatch of ΔC_i and V_{ref} is the reference voltage. From the definition on DNL and INL in (5) and (6), the standard deviations of DNL and INL in terms of capacitor mismatch are easily calculated [4, 5]. Note that all the capacitor variations have been referred to the mismatch of the unit capacitor because of the rule of thumb that the mismatch is inversely proportional to the squared of the area [6]. The relationship between the standard deviation of INL and DNL and the mismatch (σ_0/C_0) of unit capacitor has been summarised in Table 1. Explicitly from Table 1, even though the INL/DNL performance becomes worst for the LSB-down schemes, the V_{cm}-based with LSB down can save the switching energy by around 93%, and the area by a quarter for the same INL/DNL performance as the conventional BWA approach. When capacitor mismatch calibration technique [7] is applied, the unit capacitor can be sized only considering the thermal noise requirement. With the same unit capacitance, the LSB-down scheme saved 50% of switching energy and area.

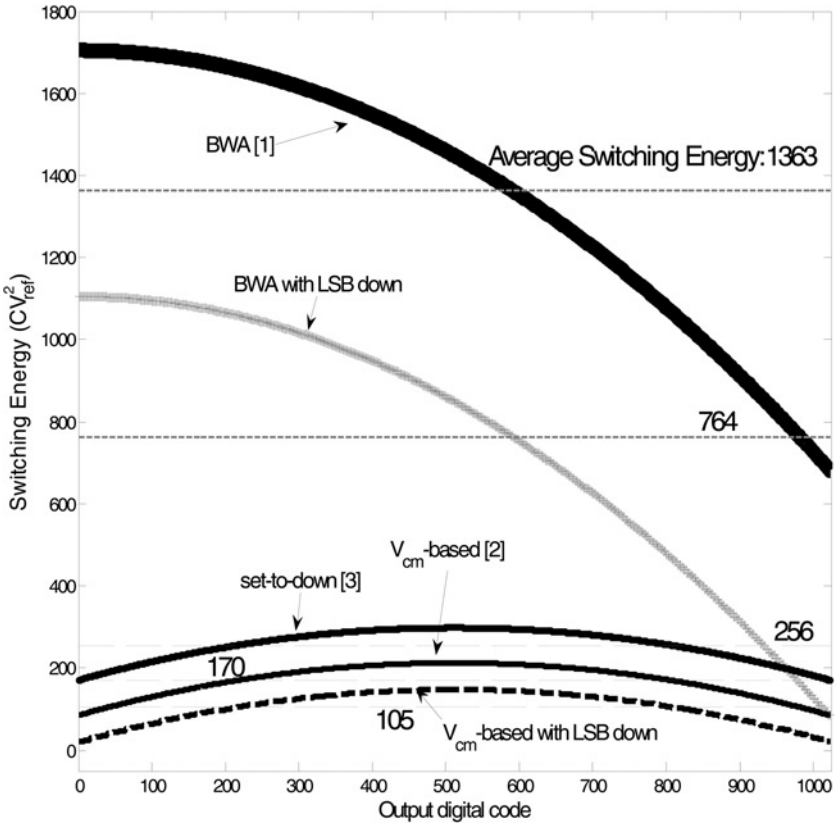

Fig. 4 *Normalised switching energy comparison for 10 bit SAR ADCs employing various CDACs*

Table 1 Comparison of CDACs with differential architectures

	Average power, J	σ_{INL}, LSB	σ_{DNL}, LSB	Total capacitance
BWA [1]	$1.33 \times 2^N C_0 V_{ref}^2$	$2^{(N/2)-1}(\sigma_0/C_0)$	$2^{(N/2)}(\sigma_0/C_0)$	$2^{N+1}C_0$
BWA with LSB down	$0.75 \times 2^N C_0 V_{ref}^2$	$\sqrt{2}2^{(N/2)-1}(\sigma_0/C_0)$	$\sqrt{2}2^{(N/2)}(\sigma_0/C_0)$	$2^N C_0$
V_{cm}-based [2]	$0.17 \times 2^N C_0 V_{ref}^2$	$(\sqrt{2}/2)2^{(N/2)-1}(\sigma_0/C_0)$	$(\sqrt{2}/2)2^{(N/2)}(\sigma_0/C_0)$	$2^N C_0$
V_{cm}-based with LSB down	$0.09 \times 2^N C_0 V_{ref}^2$	$2^{(N/2)-1}(\sigma_0/C_0)$	$2^{(N/2)}(\sigma_0/C_0)$	$2^{N-1}C_0$

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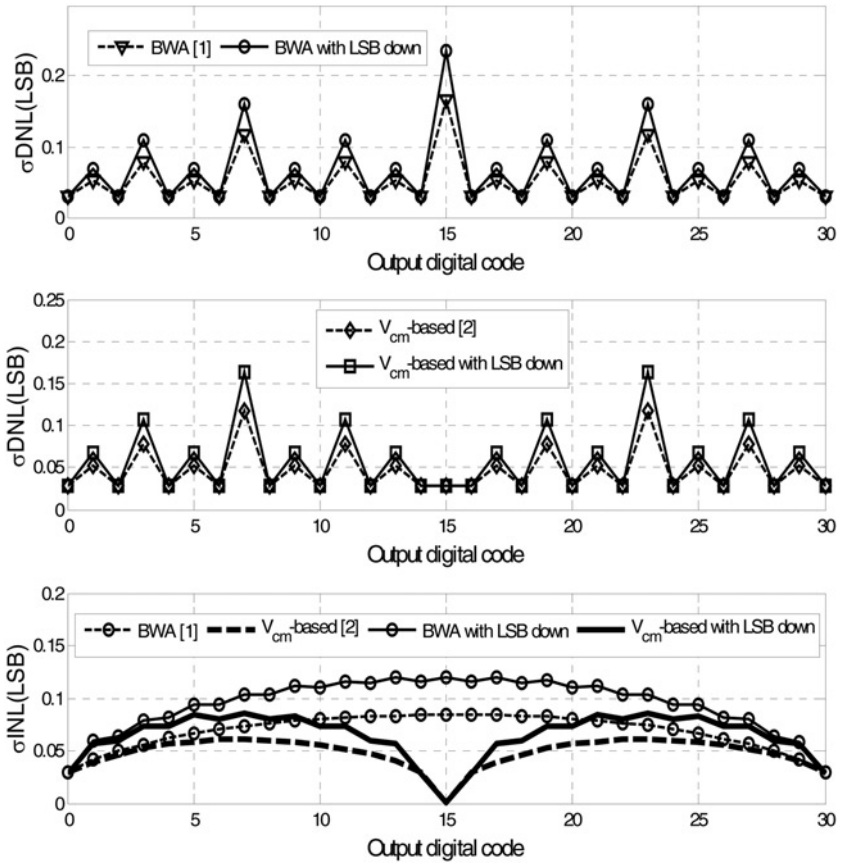

Fig. 5 *DNL and INL of 5 bit SAR ADC with BWA, BWA with LSB down, V_{cm}-based and V_{cm}-based with LSB down DACs5000 Monte Carlo runs were performed with independent identically distributed Gaussian errors in the unit capacitors ($\sigma_0/C_0 = 3\%$)*

Table 1 is a summary comparing the power, INL, DNL and total capacitance of different DAC approaches for an *N*-bit SAR ADC. The results have good achievement with simulations from 5000 Monte Carlo runs as shown in Fig. 5.

5 Conclusions

This manuscript has proposed to make use of asymmetrically switching in the LSB transition in some commonly used CDACs in differential SAR ADCs. When it is applied to V_{cm}-based structure, it achieves 93% energy efficiency with similar INL/DNL performance when compared with the conventional BWA approach. The total capacitance is reduced by a quarter of the BWA without introducing the complexity of logics and switches. It achieves 50% energy saving and area reduction with the same unit capacitor comparing the V_{cm}-based structure without LSB down.

6 Acknowledgment

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