Current sharing in parallel connected boost converters

M.R. Geetha[1], *R. Suja Mani Malar*[2], *T. Ahilan*[3]

[1]*Department of ECE, Ponjesly College of Engineering, Alamparai, Nagercoil, India*
[2]*Department of Electrical and Electronics Engineering, Narayanaguru Siddhartha College of Engineering, Nattalam, Kanyakumari District, India*
[3]*Department of Mechanical Engineering, Immanuel Arasar JJ College of Engineering, Marthandam, Kanyakumari District, India*
E-mail: geetha028@gmail.com

Published in *The Journal of Engineering*; Received on 26th August 2016; Accepted on 19th September 2016

Abstract: Parallel connection of converter modules results in generation of higher output current. Improper current sharing takes place if parameters of two converter modules are different. This study proposes a new current-sharing scheme for parallel connected boost converters. This current-sharing scheme control converter output by proper selection of transistor switch current. In this case, converter duty ratio is not adjusted directly. The adjustment of converter duty ratio depends on inductor current, capacitor voltage and power input voltage of converter. Stability of the proposed current-sharing scheme is increased by adding artificial ramp to transistor switch current. The effects of adding artificial ramp are analysed and discussed. The proposed current-sharing scheme is compared with existing current-sharing scheme whose converter output is regulated by direct choice of duty ratio. The proposed system is implemented in real time using PIC16F877A. Simulation and experimental results verify the effectiveness of the proposed current-sharing scheme.

1 Introduction

High power dc–dc converters have become a major requirement in many applications. It plays a vital role, especially in medical field, industries, satellite communication, telecommunication, military application etc. To generate higher output current from low power converter modules, two or more low power *dc–dc* converter modules can be connected in parallel at the output [1–4].This paper proposes parallel connected boost converters for generation of higher output current.

The main problem associated with parallel converters is parameter mismatch. It results in power in balance problems between converter modules. The power in balance problems degrades the performances of parallel connected converter modules. Hence, it is essential to ensure that each converter module of parallel connected boost converters share the load current equally in the presence of parameter mismatch. There exist many current-sharing techniques for parallel connected converters.

One of the commonly used methods for stabilisation of parallel *dc–dc* converters is the conventional droop method [5, 6]. Drawback of this method is load sharing depends on output-voltage regulation (OVR). Alternative current-sharing system is active current-sharing mechanisms [7–11]. Here, the difference between the reference current and the output current of each converter module is given as input to control loop. One common current-sharing approach is the dedicated master–slave control scheme. In this scheme, all of the slave modules follow the reference current of the master.

A control scheme for current sharing is proposed in [12]. Two loops were used, an output-voltage loop and an inner current loop. The control scheme was implemented using digital signal processor (DSP). The converter output is controlled by direct choice of duty ratio.

In [13], a three-loop control strategy, consisting of common OVR loop, individual circulating current suppression loop and individual inner current tracking loop were used for current sharing. In this method increase in number of loops increases circuit complexity.

A three-loop control scheme with fixed and common duty cycle was presented in [14]. Common duty ratio control scheme for an input-parallel–output-parallel (IPOP) connected converters was presented in [15, 16]. Automatic sharing of currents in two half-bridge converter modules by applying an interleaving connection in the rectifier diodes was presented in [17].

In [12, 13], current sharing takes place using direct choice of duty ratio, which increases circuit complexity. However, in [14–17] current sharing takes place without a dedicated current controller, but based on common duty ratio. The drawback is no perfect current sharing takes place if the parameter mismatch is more between converter modules.

This paper proposes a new current-sharing scheme in which converter output is controlled by correct selection of transistor switch current $i_s(t)$. The transistor switch current depends on control input signal $i_c(t)$ which is the difference between reference voltage and output voltage of converter module. The duty cycle of transistor is not directly controlled. Instead the regulation of converter output depends on input and output voltages and inductor currents. Such mode of regulating converter output is referred to as current programming mode.

Section 2 presents modelling of boost converter via algebraic approach. Section 3 presents stability analysis of the proposed system. Current programmed controller model of boost converter is given in Section 4. Block diagram description and current-sharing scheme of the proposed system is presented in Section 5. Design of voltage compensator is presented in Section 6. Section 7 gives the simulation and experimental results. The conclusion is discussed in Section 8.

2 Simple model of boost converter via algebraic approach

The circuit diagram of boost converter operating in continuous conduction mode is shown in Fig. 1. The small signal averaged equation for boost converter under duty cycle control is given as [18]

$$L\frac{\mathrm{d}\hat{i}_L(t)}{\mathrm{d}t} = \hat{v}_g(t) - D'\hat{v}_c(t) + \hat{d}\,(t)V(t) \tag{1}$$

$$C\frac{\mathrm{d}\hat{v}(t)}{\mathrm{d}t} = D'\hat{i}_L(t) - I_L\hat{d}(t) - \frac{\hat{v}(t)}{R} \tag{2}$$

$$\hat{i}_g(t) = D\hat{i}_L(t) + \hat{d}(t)\left(-\frac{\hat{v}(t)}{R}\right) + D'\left(\hat{i}_c(t) + \frac{\hat{v}(t)}{R}\right) \tag{3}$$

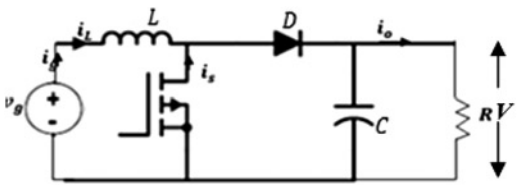

Fig. 1 *Circuit diagram of boost converter*

Applying Laplace for (1)–(3)

$$S L \hat{i}_L(s) = \hat{v}_g(s) - D' \hat{v}_c(s) + \hat{d}\,(s) V(s) \tag{4}$$

$$S C \hat{v}(s) = D' \hat{i}_L(s) - I_L \hat{d}(s) - \frac{\hat{v}(s)}{R} \tag{5}$$

$$\hat{i}_g(s) = D \hat{i}_L(s) + \hat{d}(s)\left(-\frac{\hat{v}(s)}{R}\right) + D'\left(\hat{i}_c(s) + \frac{\hat{v}(s)}{R}\right) \tag{6}$$

Assuming $\hat{i}_L(s)$ to be equal to the control input signal current $\hat{i}_C(s)$, (4) and (6) can be rewritten as

$$S L \hat{i}_C(s) = \hat{v}_g(s) - D' \hat{v}_c(s) + \hat{d}\,(s) V(s) \tag{7}$$

$$\hat{i}_g(s) = D \hat{i}_c(s) + \hat{d}(s)\left(-\frac{\hat{v}(s)}{R}\right) + D'\left(\hat{i}_c(s) + \frac{\hat{v}(s)}{R}\right) \tag{8}$$

From (7)

$$\hat{d}\,(s) = \frac{S L \hat{i}_C(s) - \hat{v}_g(s) + D' \hat{v}_c(s)}{V(s)} \tag{9}$$

Substituting $\hat{d}\,(s)$ in (5)

$$S C \hat{v}(s) = D' \hat{i}_C(s) - \frac{\hat{v}(s)}{R} - I_L\left[\frac{S L \hat{i}_C(s) - \hat{v}_g(s) + D' \hat{v}_c(s)}{V(s)}\right] \tag{10}$$

For boost converter output voltage

$$v = \frac{1}{D'} v_g \tag{11}$$

and load current

$$I_L = \frac{v}{R} = \frac{v_g}{D' R} \tag{12}$$

Substitution of (12) in (10) gives

$$S C \hat{v}(s) = D' \hat{i}_C(s) - \frac{\hat{v}(s)}{R} - \frac{v_g}{D' R}\left[\frac{S L \hat{i}_C(s) - \hat{v}_g(s) + D' \hat{v}_c(s)}{V(s)}\right] \tag{13}$$

$$S C \hat{v}(s) = \hat{i}_C(s)\left[D' - \frac{S L}{D' R}\right] - \hat{v}(s)\left[\frac{1}{R} + \frac{1}{R}\right] + \hat{v}_g(s)\left[\frac{1}{D' R}\right] \tag{14}$$

Similarly substitution of (9) and (12) in (8) gives

$$\hat{i}_g(s) = \hat{i}_C(s)\left[1 - \frac{S L}{R}\right] + \frac{\hat{v}_g(s)}{R} \tag{14a}$$

From (14) and (14a), the two port equivalent circuit used to model the current programmed boost converter is obtained and is shown in Fig. 2.

In Fig. 2 by making $\hat{v}_g(s) = 0$, the control to output transfer function is expressed as

$$G_{V_c}(s) = D'\left(1 - \frac{S L}{D'^2 R}\right)\left[R \text{ parallel } R \text{ parallel } \frac{1}{S C}\right] \tag{15}$$

Simplifying (15) results in

$$G_{V_c}(s) = \frac{D' R}{2} \frac{\left(1 - (S L / D'^2 R)\right)}{1 + (R C S / 2)} \tag{16}$$

Similarly by making $\hat{i}_C(s) = 0$, the line to output transfer function

$$G_{V_g}(s) = \frac{1}{D' R}\left[R \text{ parallel } R \text{ parallel } \frac{1}{S C}\right] \tag{17}$$

Simplifying (17) gives

$$G_{V_g}(s) = \frac{1}{2D'} \frac{1}{1 + (R C S / 2)} \tag{18}$$

Equations (16) and (18) give the transfer function of boost converter by assuming an inductor current equal to the control current (*ie*) $\hat{i}_L(s) = \hat{i}_C(s)$. Two port equivalent circuits to model parallel connected current programmed boost converter are shown in Fig. 3.

Equations (16) and (18) show that controlling converter output using indirect adjustment of duty ratio reduces number of poles of line to output transfer function and control to output transfer function. Minimising number of poles makes designing the controller easier. Figs. 3*a* and *b* show line to output frequency response of boost converter for direct duty ratio control and indirect duty ratio control, respectively.

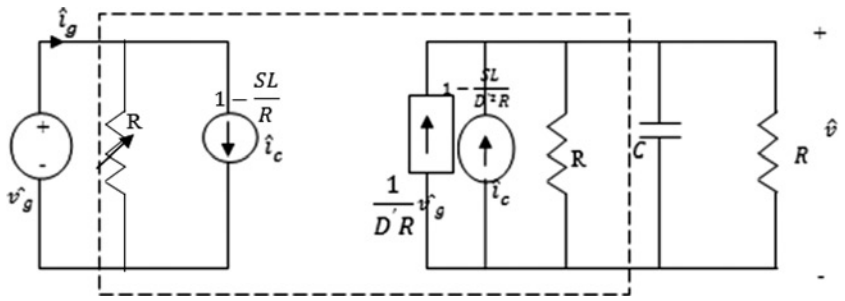

Fig. 2 *Two port equivalent circuit of boost converter*

J Eng, 2016, Vol. 2016, Iss. 12, pp. 444–452
doi: 10.1049/joe.2016.0238

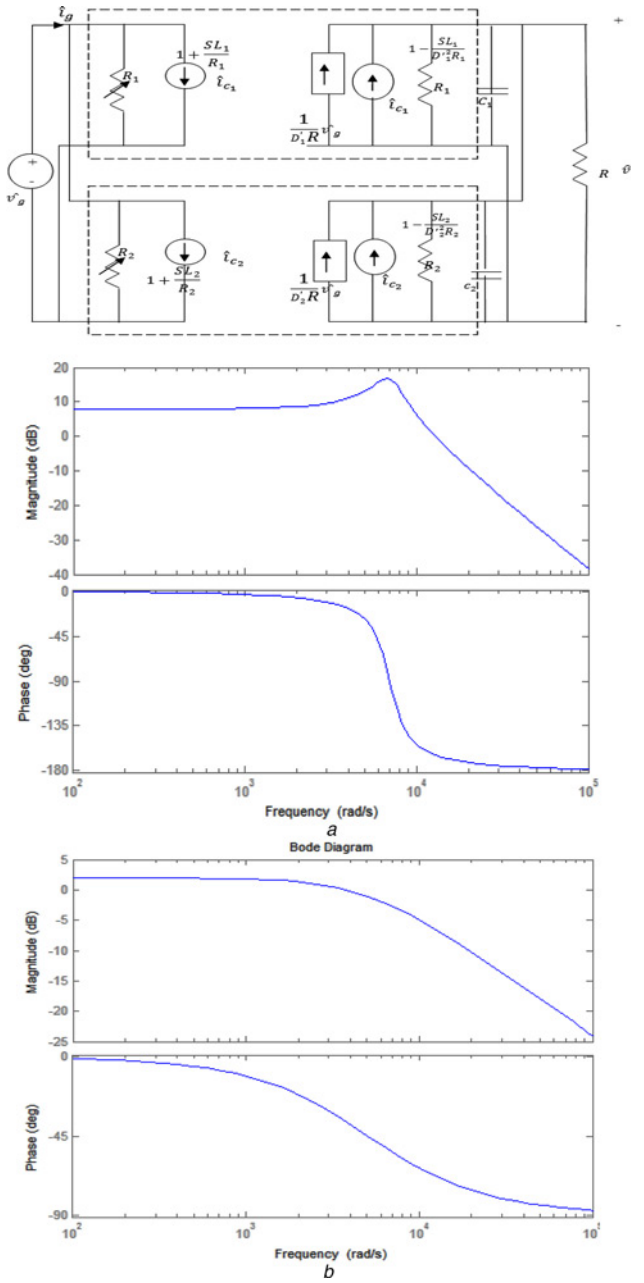

Fig. 3 *Two port equivalent circuit of parallel connected boost converter*
a Line to output frequency response of boost converter using duty cycle control
b Line to output frequency response of boost converter using current programming mode control

3 Stability analysis

The proposed current programmed controller results in unstable operation for duty cycle $(d) > 0.5$. To maintain stability for $d > 0.5$, an artificial ramp is added to the transistor switch current. This section analyses the stability of boost converter for $d > 0.5$ and < 0.5. Fig. 4 shows that during the first sub-interval, current $\hat{i}_L(t)$ increases with slope m_1 until it reaches the control signal $\hat{i}_c(t)$

$$i_L(dT_s) = i_c(t) = i_L(0) + m_1 dT_s \tag{19}$$

Hence duty cycle

$$d = \frac{i_c(t) - i_L(0)}{m_1 T_s} \tag{20}$$

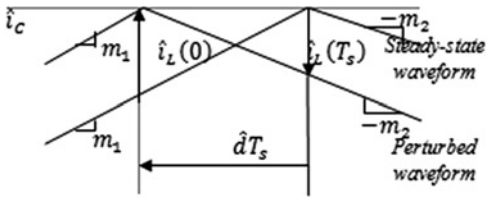

Fig. 4 *Steady state and perturbed inductor current waveforms*

Similarly during second sub-interval

$$i_L(T_s) = i_L(0) + m_1 dT_s - m_2 d'T_s \tag{21}$$

Under steady state $i_L(T_s) = i_L(0)$, $d = D$, $m_1 = M_1$ and $m_2 = M_2$.
So that $M_1 DT_s - M_2 D'T_s$

$$\frac{M_1}{M_2} = \frac{D}{D'} \tag{22}$$

Applying perturbation to initial current $i_L(0)$, an expanded view of steady state and perturbed inductor current waveforms near the peak of $i_L(t)$ is shown in Fig. 4.
From Fig. 4

$$\hat{i}_L(0) = -m_1 \hat{d} T_s \tag{23}$$

$$\hat{i}_L(T_s) = m_2 \hat{d} T_s \tag{24}$$

Eliminating $\hat{d}$ from (30)

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2}{m_1}\right) \tag{25}$$

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right) \tag{26}$$

The above expression gives inductor current for the first switching period. For the second switching period

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s)\left(-\frac{D}{D'}\right) \tag{27}$$

Substituting (26) into (27)

$$\hat{i}_L(2T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^2 \tag{28}$$

For n switching period

$$\hat{i}_L(2T_s) = \hat{i}_L((n-1)T_s)\left(-\frac{D}{D'}\right) \tag{29}$$

$$\hat{i}_L(2T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^n \tag{30}$$

Above equation indicates that perturbation increases with increase in $-(D/D')$ and decreases with decrease in $-(D/D')$.
Assuming $D > 0.5$

$$-\frac{D}{D'} = \frac{0.7}{0.3} = -2.33.$$

It indicates that perturbation in inductor current increases by a factor

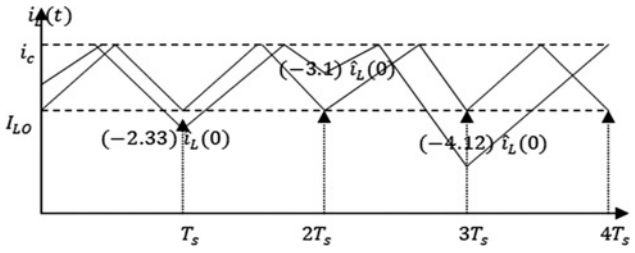

Fig. 5 *Unstable oscillation for* $d > 0.5$

of −2.33 for every switching period and is shown in Fig. 5. It results in unstable operation.

Assuming $D < 0.5$, $-(D/D') = -(0.4/0.6) = -0.6$. It indicates that perturbation in inductor current decreases by a factor of −0.6 for every switching period and is shown in Fig. 6. It results in stable operation.

To maintain stability for $D > 0.5$, an artificial ramp (m_a) is added to the transistor switch current and is shown in Fig. 6*a*.

From Fig. 6*a*

$$\hat{i}_L(0) = -\hat{d}T_s(m_1 + m_a) \tag{31}$$

and

$$\hat{i}_L(T_s) = -\hat{d}T_s(m_a - m_2) \tag{32}$$

Eliminating $\hat{d}$ from (31) and (32)

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{33}$$

Above equation gives perturbed inductor current for the first switching period.

For the *n*th switching period

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{34}$$

$$\hat{i}_L(nT_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n \tag{35}$$

$$\hat{i}_L(nT_s) = \hat{i}_L(0)(\alpha)^n \tag{36}$$

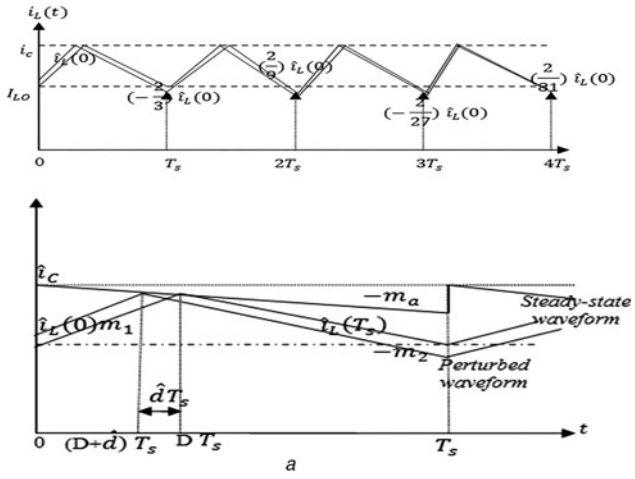

Fig. 6 *Stable transient for* $d < 0.5$
a Inductor current waveform of boost converter with artificial ramp (m_a)

where

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} \tag{37}$$

If the value of α increases, perturbation increases and perturbation decreases with decrease in value of α. Thus, to maintain stability choose the value of m_a in such a way that α is <1. Choose the value of m_a to be equal to m_2 or half of the value of m_2.

If $m_a = m_2$, $\alpha = 0$, hence $\hat{i}_L(T_s) = 0$ for any value of $\hat{i}_L(0)$. As a result any error present in system gets removed after one switching period. This process is referred to as dead beat control.

For the proposed system choose $m_a = m_2$. For boost converter

$$m_a = m_2 = \frac{\hat{v} - \hat{v}_g}{L}$$

$$m_a = \frac{120 - 48}{100e - 6}$$

$$m_a = 7.2e5$$

This is the magnitude of artificial ramp that is added to the transistor switch current of boost converters 1 and 2 to enhance stability.

4 Current programmed controller model of boost converter

This section explains the current controller model of boost converter. The waveform of inductor current of boost converter 1 is shown in Fig. 7.

From Fig. 7, the average inductor current of boost converter 1 can be expressed as

$$< i_{L_1}(t) > T_s = < i_{c_1}(t) > T_s - m_a d_1 T_s - d_1\left(\frac{m_{1d_1T_s}}{2}\right) - d_1'\left(\frac{m_{2d_1'T_s}}{2}\right) \tag{38}$$

$$< i_{L_1}(t) > T_s = < i_{c_1}(t) > T_s - m_a d_1 T_s - \left(\frac{m_{1d_1^2T_s}}{2}\right) - \left(\frac{m_{2d_1'^2T_s}}{2}\right) \tag{39}$$

After perturbation and linearisation and eliminating higher-order

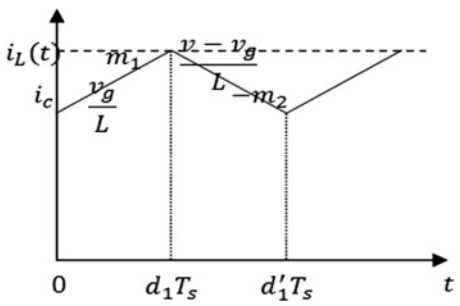

Fig. 7 *Inductor current waveform*

doi: 10.1049/joe.2016.0238

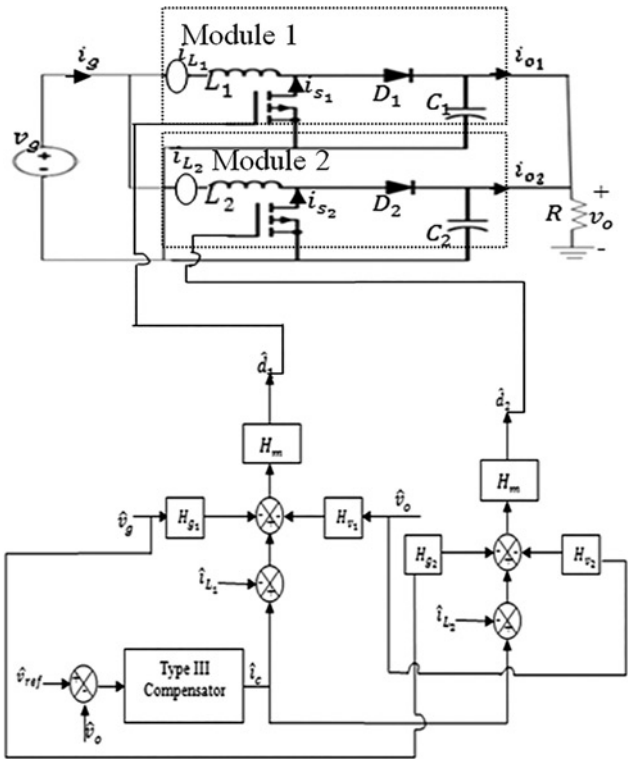

Fig. 8 *Proposed block diagram with new current-sharing scheme*

terms, the simplified form of above expression is written as

$$\hat{i}_{L_1}(t) = \hat{i}_{c_1}(t) - M_a T_s \hat{d}_1(t) - \frac{T_s}{2}(2D_1 - 1)\hat{m}_1(t) - D_1^{'2}\frac{T_s}{2}\hat{m}_2(t) \quad (40)$$

$$M_a T_s \hat{d}_1(t) = \hat{i}_{c_1}(t) - \hat{i}_{L_1}(t) - \frac{T_s}{2}(2D_1 - 1)\hat{m}_1(t) - D_1^{'2}\frac{T_s}{2}\hat{m}_2(t) \quad (41)$$

$$\hat{d}_1(t) = \frac{1}{M_a T_s}\left[\hat{i}_{c_1}(t) - \hat{i}_{L_1}(t) - \frac{T_s}{2}(2D_1 - 1)\hat{m}_1(t) - D_1^{'\hat{m}_2 2}\frac{T_s}{2}(t)\right] \quad (42)$$

The change in slope for boost converter is

$$\widehat{m_1} = \frac{\hat{v}_g}{L} \quad \text{and} \quad \widehat{m_2} = \frac{\hat{v} - \hat{v}_g}{L}$$

Therefore, equation becomes

$$\hat{d}_1(t) = \frac{1}{M_a T_s}\left[\hat{i}_{c_1}(t) - \hat{i}_{L_1}(t) - \frac{T_s}{2}(2D_1 - 1)\frac{\hat{v}_g}{L} - D_1^{'2}\frac{T_s}{2}\frac{\hat{v} - \hat{v}_g}{L}\right] \quad (43)$$

$$\hat{d}_1(t) = H_m\left[\hat{i}_{c_1}(t) - \hat{i}_{L_1}(t) - H_{g_1}\hat{v}_g - H_{v_1}(\hat{v} - \hat{v}_g)\right] \quad (44)$$

where $H_m = (1/M_a T_s)$, $H_{g_1} = (T_s/2L_1)(2D_1 - 1)$ and $H_{v_1} = D_1^{'2}(T_s/2L_1)$ are loop gains of boost converter 1. Equation (26) gives duty ratio for boost converter 1.

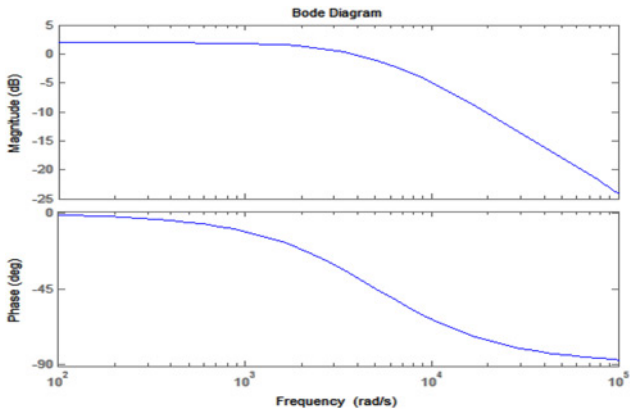

Fig. 9 *Open-loop response of boost converter*

Similarly for boost converter 2

$$\hat{d}_2(t) = \frac{1}{M_a T_s}\left[\hat{i}_{c_2}(t) - \hat{i}_{L_2}(t) - \frac{T_s}{2}(2D_2 - 1)\hat{m}_1(t) - D_2^{'2}\frac{T_s}{2}\frac{\hat{v} - \hat{v}_g}{L}\right] \quad (45)$$

$$\hat{d}_2(t) = H_m\left[\hat{i}_{c_2}(t) - \hat{i}_{L_2}(t) - H_{g_2}\hat{v}_g - H_{v_2}(\hat{v} - \hat{v}_g)\right] \quad (46)$$

where $H_m = (1/M_a T_s)$, $H_{g_2} = (T_s/2L_2)(2D_2 - 1)$ and $H_{v_2} = D_2^{'2}(T_s/2L_2)$ are loop gains of boost converter 2.

On the basis of (45) and (46), the duty ratio of boost converter 1 and 2 gets adjusted for controlling load current and to share the load current equally between two parallel connected boost converters.

5 Block diagram description and control scheme

The block diagram of parallel connected boost converters is shown in Fig. 8. Once input voltage v_g is applied, transistor Q_1 and Q_2 conducts, minimum current flows through the circuit. If the minimum current is positive, diodes D_1 and D_2 become forward biased and the converter modules operate in continuous conduction mode. The output current flows through boost converter modules 1 and 2 are i_{o_1} and i_{o_2}, respectively. Control of output currents i_{o_1} and i_{o_2} depends on proper selection of transistor switch currents i_{s_1} and i_{s_2} of modules 1 and 2, respectively. The control input signal i_c is generated based on the difference between output voltage v_o and the reference voltage (v_{ref}). The difference between i_c and respective transistor switch currents, together with converter gains adjust the duty ratio of converter modules. This results in perfect current sharing [19–23] between converter modules even if parameters of converter modules are different.

6 Design of controllers

6.1 Type III compensators

Generally compensator acts as a controller. Type III compensator improves transient and steady-state response. In this paper, Type III compensator is used to design voltage controller.

From open-loop response of boost converter, Type III voltage compensator is designed. Fig. 9 gives the open-loop response of boost converter. The designed voltage compensator from open-loop response of boost converter is shown in Table 1.

Table 1 Voltage compensator

Compensator	Transfer function of voltage compensator
Type III	$\frac{5.81e-7s^2+1.79e-3s+1}{5.81e-7s^2+1.57e-3s+1}$

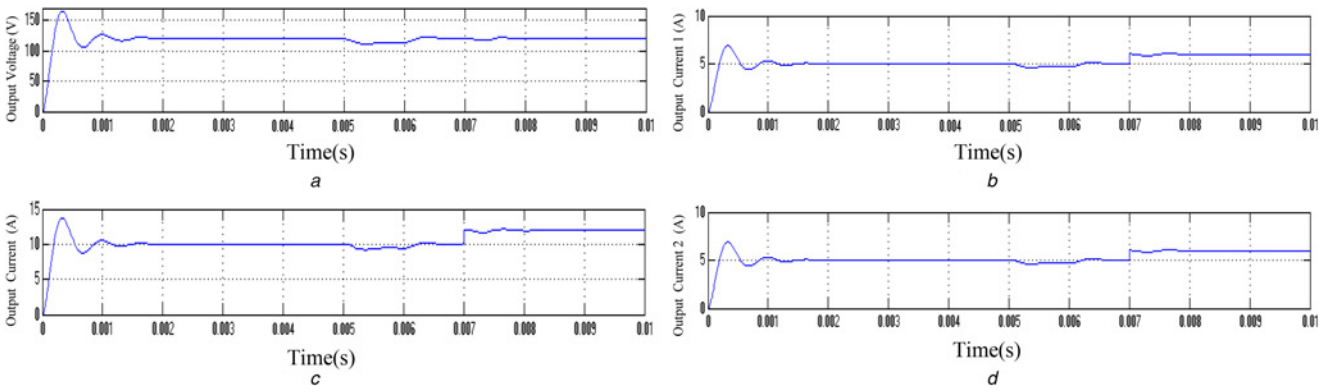

Fig. 10 *Current sharing among each boost converter module $L_1 = 100\ \mu H$ and $L_2 = 110\ \mu H$ with direct duty ratio adjustment*
a Output voltage
b Output current
c Output current of boost converter 1
d Output current of boost converter 2

7 Results and discussion

This section presents the simulation and experimental results of IPOP connected boost converters. The specifications of boost converter are given as follows: (i) the input dc voltage of 44–52 V; (ii) output voltage of 120 V, regulated by closed-loop controller; and (iii) maximum output current of 10 A.

The component values for power stage are designed as follows: capacitances C_1 and C_2 are equal to 33 µF; input-filter inductances of L_1 and L_2 are same at 100 µH; and duty ratios d_1 and d_2 are between 0.3 and 0.9. The switching frequencies for individual converter modules are 100 kHz.

7.1 Simulation results

The parallel connected boost converter is simulated in MATLAB in which the output voltage is controlled by Type III compensator and the output current is regulated by current programmed controller.

Fig. 10 shows the simulation results of IPOP connected boost converter which is controlled by direct choice of duty ratio. It uses a dedicated current-sharing controller (Type III compensator). The line disturbance is given at $t = 0.005$ s from 48 to 44 V and from 44 to 48 V at $t = 0.006$ s.The load disturbance is given at $t = 0.007$ s from $R = 12$ to $10\ \Omega$. Fig. 10*a* shows that response of output voltage has an overshoot of 165 V and settles at 0.0018 s. The response acts well for line and load disturbances. The output voltage is 120 V.

Fig. 10*b* shows that the overshoot of output-current response is at 13.75 V and settles at 0.0018 s. The output current is 10 A. Figs. 10*c* and *d* show that output current 1 and output current 2 of boost converter has an overshoot of 6.8728 V and settles at 0.0018 s. Fig. 10 indicates that the start-up transient is more and takes time to settle.

Fig. 11 shows the simulation results of IPOP connected boost converter with current programmed controller without proper choosing of loop gain H_m (7.2e5). The line disturbance from 48 to 44 V is given at time $t = 0.005$ s and from 44 to 48 V at $t = 0.006$ s. The load disturbance is given at $t = 0.007$ s from $R = 12$ to $10\ \Omega$. The response indicates that the line disturbance is not rejected because of wrong selection of loop gain H_m. Fig. 11 shows that start-up transient is reduced because of using current programmed controller. In addition, the response settles faster. Figs. 11*c* and *d* show that the output current of boost converter 1 and boost converter 2 shares equally even if $L_1 = 100$ µH and $L_2 = 110$ µH. Hence, the proposed current programmed controller regulates load current and shares the output current equally between parallel connected boost converter modules.

Fig. 12 shows the simulation results of IPOP connected boost converter with current programmed controller with proper selection of loop gain H_m (1/7.2*e*5). The line disturbance is given at time $t = 0.005$ s from 48 to 44 V and from 44 to 48 V at $t = 0.006$ s. The load disturbance is given at $t = 0.007$ s from $R = 12$ to $10\ \Omega$. Fig. 12*a* indicates that the line disturbance is rejected

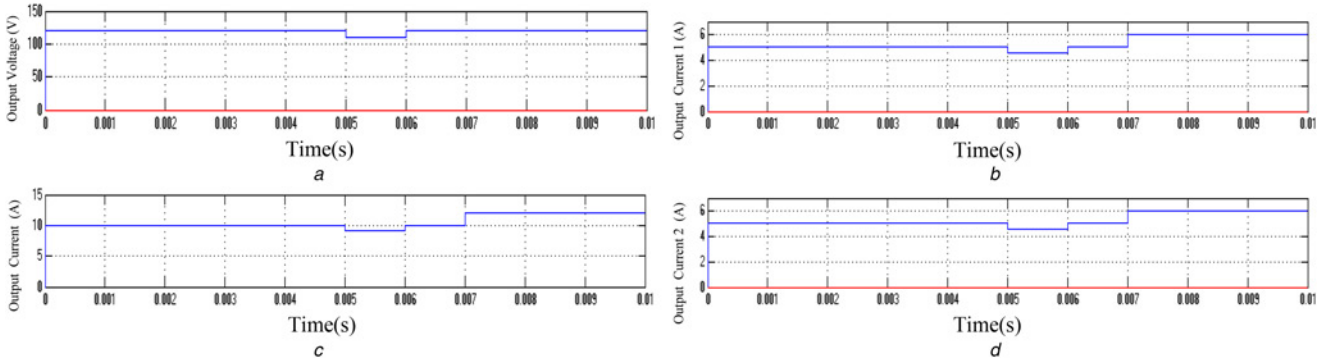

Fig. 11 *Current sharing among each boost converter module using current programmed controller with loop gain $H_m = 7.2e5$ and with $L_1 = 100\ \mu H$ and $L_2 = 110\ \mu H$*
a Output voltage
b Output current
c Output current of boost converter 1
d Output current of boost converter 2

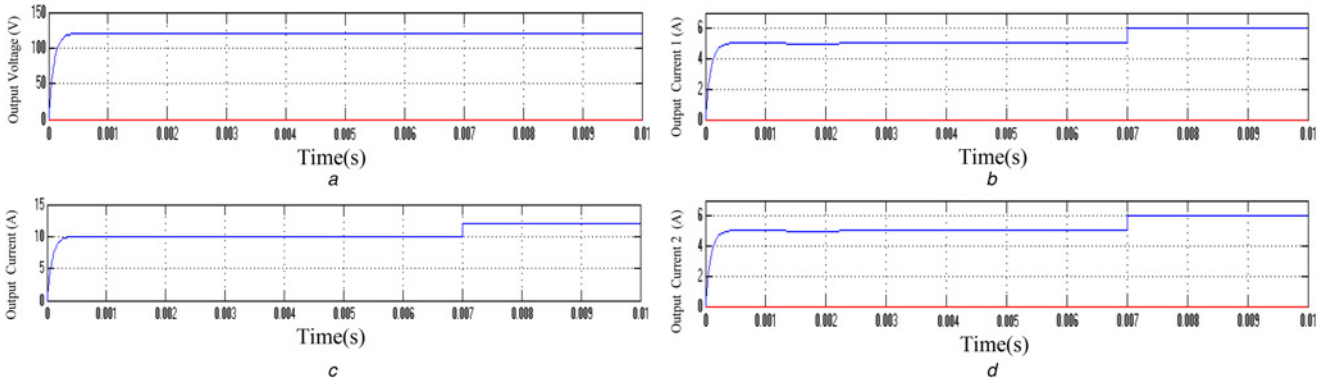

Fig. 12 *Current sharing among each boost converter module using current programmed controller with loop gain $H_m = 1/7.2e5$ and with $C_1 = 33\ \mu F$ and $C_2 = 40\ \mu F$*
a Output voltage
b Output current
c Output current of boost converter 1
d Output current of boost converter 2

because of correct selection of loop gain H_m. Fig. 12 shows that the response settles faster and reduces start-up transient. Figs. 12*c* and *d* indicate that the output current of boost converter 1 and boost converter 2 shares equally even if $C_{11} = 33\ \mu F$ and $C_2 = 40\ \mu F$.

From Fig. 12, it is inferred that the current programmed controller works well than direct duty ratio adjustment. It reduces start-up transient and makes response settle faster. Also, it rejects line disturbance because of proper selection of loop gain H_m. The loop gain H_m depends on magnitude of artificial ramp m_a added to transistor switch current $i_s(t)$.

7.2 Experimental results

An experimental setup consisting of IPOP connected boost converter modules as shown in Fig. 8 has been built to validate the proposed current-sharing scheme with current programmed controller.

The specifications of components used are capacitances $C_1 = C_2 = 33\mu F$ and inductances $L_1 = L_2 = 100\mu H$ and $L_{21} = 30\mu F$, duty ratio of converter modules are 0.7, input voltage is 44–48 V and output voltage is 120 V. The switching frequencies of parallel connected boost converters are 100 kHz.

Figs. 13*a–d* show the waveform of input voltage and output voltage, output current, output currents 1 and 2 of IPOP connected boost converters with same parameters in module 1 and module 2. Figs. 13*b* and *c* indicate that the performance of output voltage and current is good. Fig. 13*d* shows that output currents 1 and 2 share equally between converter modules 1 and 2, respectively.

To prove that current programmed controller share output current equally between IPOP connected boost converters with different

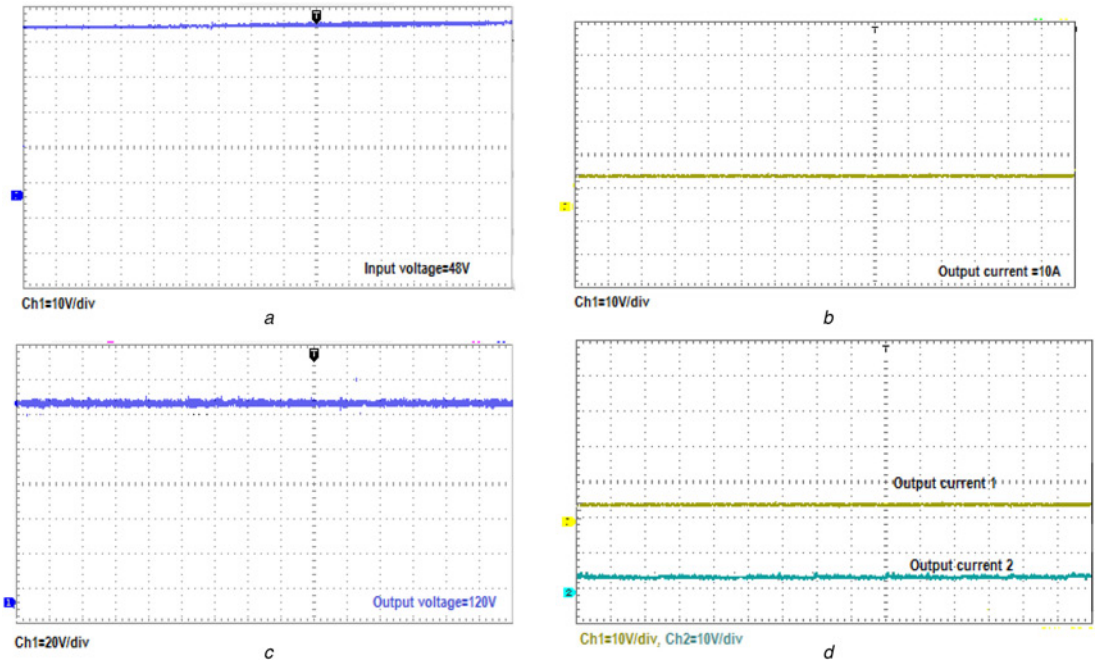

Fig. 13 *Output waveforms of IPOP connected modules with same parameters*
a Input-voltage waveform
b Output-voltage waveform
c Output-current waveform
d Individual output currents of two modules

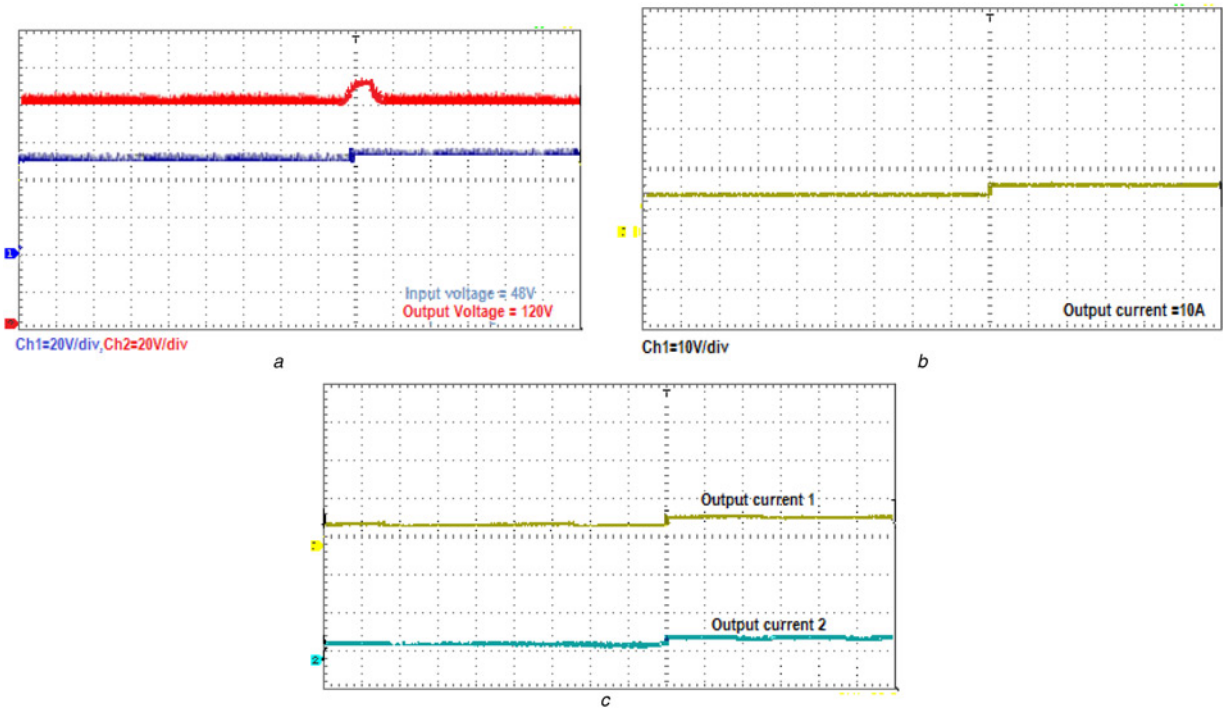

Fig. 14 *Output waveforms with $L_1 = 100\,\mu H$ and $L_2 = 110\,\mu H$ and loop gain $H_m = 7.2e5$ for change in line and load disturbances*
a Input-voltage and output-voltage waveform
b Output-current waveform
c Individual output currents of two modules

circuit parameters, choose $L_1 = 100$ and $L_2 = 110\,\mu H$. In addition, choose loop gain $H_m = 7.2e5$. Fig. 14 shows waveform at full load of 10 A with $L_1 = 100$ and $L_2 = 110\,\mu H$. Fig. 14*c* indicates that even with step change from 48 to 50 V and for load change from $R = 12$ to $10\,\Omega$ well sharing of output current takes place. Fig. 14*a* indicates due to incorrect choice of loop gain

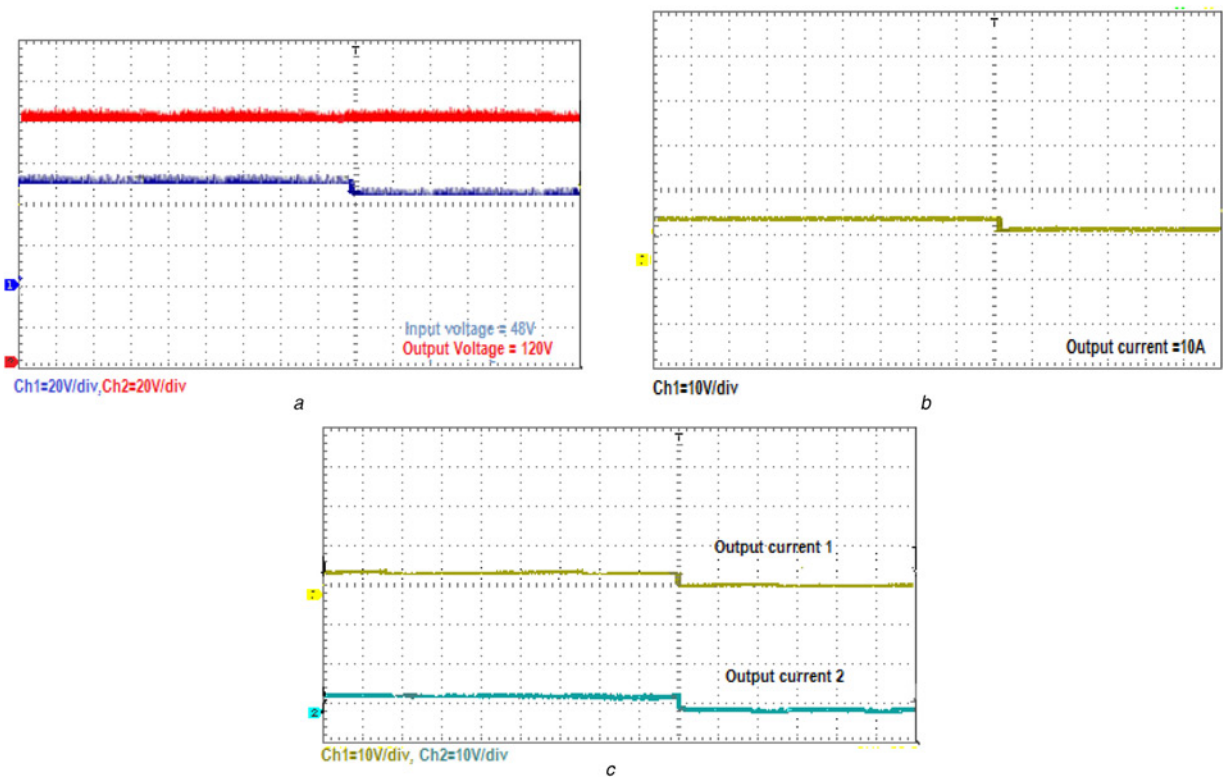

Fig. 15 *Output waveforms with $C_1 = 33\,\mu F$ and $C_2 = 40\,\mu F$ and loop gain $H_m = 1/7.2e5$ for change in line and load disturbances*
a Input-voltage and output-voltage waveform
b Output-current waveform
c Individual output currents of two modules

$H_m = 7.2e5$, the line disturbance is not rejected. Fig. 14 indicates that the proposed IPOP connected boost converter with current programmed controller has very good closed-loop performance.

Fig. 15 shows experimental waveform of IPOP connected boost converter with $C_1 = 33$ and $C_2 = 40\,\mu\text{F}$ and loop gain $H_m = 1/\ 7.2e5$. Fig. 15*a* indicates that even with line disturbance from 48 to 44 V, the output-voltage waveform does not have any effect on line disturbance. The line disturbance is totally rejected because of correct choice of loop gain $H_m = 1/\ 7.2e5$. This proves the effectiveness of the proposed system with current programmed controller. Fig. 15*c* shows that even for load disturbance from $R = 12$ to $15\,\Omega$, good sharing of load current takes place. Fig. 15 indicates that even with changes in circuit parameters good current sharing takes place and the proposed system has good closed-loop performance.

8 Conclusion

In this paper, a new controller known as current programmed controller was used to regulate load current and to share current equally between parallel connected boost converters. On the basis of modelling of current programmed controller it has been shown that good current sharing can be achieved and stability can be improved. With difference in parameters of converter modules, it is showed that good current sharing takes place between parallel connected boost converter modules. Stability of the proposed system is examined by perfect selection of loop gain H_m which depends on artificial ramp. The proposed system is verified through simulation and experimental results.

9 References

[1] Abu-Qahouq J.A.: 'Analysis and design of N-phase current-sharing auto tuning controller', *IEEE Trans. Power Electron.*, 2010, **25**, (6), pp. 1641–1651

[2] Yoon C., Kim J., Choi S.: 'Multiphase DC–DC converters using a boost-half-bridge cell for high-voltage and high-power applications', *IEEE Trans. Power Electron.*, 2011, **26**, (2), pp. 381–388

[3] Wang D., He X., Shi J.: 'Design and analysis of an interleaved flyback–forward boost converter with the current autobalance characteristic', *IEEE Trans. Power Electron.*, 2010, **25**, (2), pp. 489–498

[4] Kim H., Falahi M., Jahns T.M., *ET AL.*: 'Inductor current measurement and regulation using a single DC link current sensor for interleaved DC–DC converters', *IEEE Trans. Power Electron.*, 2011, **26**, (5), pp. 1503–1510

[5] Zhou X., Xu P., Lee F.C.: 'A novel current-sharing control technique for low-voltage high-current voltage regulator module applications', *IEEE Trans. Power Electron.*, 2000, **15**, (6), pp. 1153–1162

[6] Kim J.-W., Choi H.-S., Cho B.H.: 'A novel droop method for converter parallel operation', *IEEE Trans. Power Electron.*, 2002, **17**, (1), pp. 25–32

[7] Johnsy A.: 'Analysis of a control strategy for parallel operation of single phase voltage source inverters', *Int. J. Adv. Res. Electr. Electron. Instrum. Eng.*, 2014, **3**, (2), pp. 148–154

[8] Abu-Qahouq J.A.: 'Analysis and design of N-phase current-sharing autotuning controller', *IEEE Trans. Power Electron.*, 2010, **25**, (6), pp. 1641–1651

[9] Peng Y.L., Cheng C., Zheng C., *ET AL.*: 'DSP-based control of parallel dc–dc boost converters by adaptive fuzzy sliding-mode control scheme'. Proc. ICGEC, 2012, pp. 130–133

[10] Sha D., Guo Z., Lio X.: 'Control strategy for input-parallel–output-parallel connected high-frequency isolated inverter modules', *IEEE Trans. Power Electron.*, 2011, **26**, (8), pp. 2237–2248

[11] Sha D., Guo Z., Lio X.: 'Cross-feedback output-current-sharing control for input-series-output-parallel modular DC–DC converters', *IEEE Trans. Power Electron.*, 2010, **25**, (11), pp. 2762–2277

[12] Panov Y., Jovanovic M.M.: 'Loop gain measurement of paralleled dc–dc converters with average current sharing control', *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2942–2948

[13] Sha D., Gu Z., Liao X.: 'DSP based series–parallel connected two full-bridge dc–dc converter with interleaving output current sharing', *J. Power Electron.*, 2010, **10**, (6), pp. 673–679

[14] Cai W., Huang Y., Fangyuan Z., *ET AL.*: 'DC voltage balancing and current sharing control of parallel multiple modules static var generator based on CPS-SPWM', *J. Int. Counc. Electr. Eng.*, 2013, **3**, (1), pp. 73–78

[15] Sha D., Guo Z., Liao X.: 'Input series connected high frequency DC–DC converters with one transformer'. Proc. Applied Power Electronics Conf., 2010, pp. 662–665

[16] Shi J., Zhou L., Xiangning H.: 'Common-duty-ratio control of input-parallel output-parallel (IPOP) connected DC–DC converter modules with automatic sharing of currents', *IEEE Trans. Power Electron.*, 2012, **27**, (7), pp. 3277–3291

[17] Shi J., Liu T., Cheng J, *ET AL.*: 'Automatic current sharing of an input-parallel output-parallel (IPOP)-connected DC–DC converter system with chain-connected rectifiers', *IEEE Trans. Power Electron.*, 2015, **30**, (6), pp. 2997–3016

[18] Joseph Basanth A., Natarajan S.P., Sivakumaran T.S.: 'Performance analysis of positive output super-lift re-lift luo converter with PI and neuro controllers', *IOSR J. Electr. Electron. Eng.*, 2013, **6**, (3), pp. 21–27

[19] Cheng J., Shi J., He X.: 'A novel input-parallel output-parallel connected DC–DC converter modules with automatic sharing of currents'. Seventh Int. Power Electronics and Motion Control Conf. (IPEMC), 2012, pp. 1871–1876

[20] Jassim B.M.H., Zahawi B., Atkinson D.J.: 'Simple control method for parallel connected three-phase PWM converters'. IET Conf. Publications, Issue 592 CP, in Proc. IET Int. Conf. on Power Electronics, Machines and Drives (PEMD 2012), 2012

[21] Xu Z., Li R., Zhu H., *ET AL.*: 'Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems', *IEEE Trans. Power Electron.*, 2012, **27**, (3), pp. 1259–1270

[22] Sha D., Guo Z., Deng K., *ET AL.*: 'Parallel connected high frequency AC link inverters based on full digital control', *J. Power Electron.*, 2012, **12**, (4), pp. 595–603

[23] Guo Z., Sha D., Liao X.: 'Wireless paralleled control strategy of three-phase inverter modules for islanding distributed generation systems', *J. Power Electron.*, 2013, **13**, (3), pp. 479–485