Three-level boost converter with zero voltage transition

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Published in *The Journal of Engineering*; Received on 24th April 2017; Accepted on 24th May 2017

Abstract: As compared with the traditional boost converter, the three-level boost converter possesses several advantages, such as lower switch voltage stresses and lower inductor current ripple. To improve the efficiency, this paper proposes a zero voltage transition (ZVT) three-level boost converter. With the proposed ZVT circuit, the switches can achieve soft switching. Moreover, by using the voltage balance control, the output voltage can be equally across the output capacitors. In this study, the effectiveness of the proposed topology is verified by the experimental results based on the field-programmable gate array control.

1 Introduction

The traditional boost converter is widely used to step-up the low input voltage. However, the switches of the traditional boost converter have to block a high output voltage. To reduce the switch voltage stresses, the three-level DC–DC converters were presented [1–4].

To improve the efficiency, the soft-switching technique is used. For the traditional soft-switching DC–DC converters, they can be classified into two types. The first one belongs to the load-resonant converters, and the second one belongs to the switch-resonant converters.

The load-resonant converters use the resonant tank connected in series with the load [5–10] or in parallel with the load [11–13]. Besides, the voltage conversion ratios are dependent on the switching frequency. Thus, the variable frequency control is necessary for the load-resonant converters. For the switch-resonant converters, they use the resonant tank connected with switches to achieve soft switching. These switch-resonant converters can be classified into general mode [14–17], full-wave mode [18–20], half-wave mode [21–23], active clamp [24–36], zero voltage transition (ZVT) [37–48], zero current transition [49–51], and ZCTZVT [52, 53].

In this paper, a ZVT three-level boost converter is proposed. With the proposed ZVT circuit, the switches of the three-level boost converter can be turned on at zero voltage. Moreover, since the output voltage is shared by two output capacitors, a voltage balance control is employed to balance the output capacitor voltages.

2 Three-level boost converter with the proposed ZVT circuit

The circuit within the dotted line shown in Fig. 1*a* displays the proposed ZVT circuit, named auxiliary circuit, which is applied to the three-level boost converter to realise soft switching of the main switches S_1 and S_2. This circuit consists of two auxiliary switches S_a and S_b, two voltage clamp diodes D_a and D_b, two auxiliary diodes D_{r1} and D_{r2}, used to avoid the inverse resonant currents, and only one resonant inductor L_r. The three-level boost converter contains two main switches S_1 and S_2 with the parasitic diodes D_{s1} and D_{s2} and the parasitic capacitances C_{s1} and C_{s2}, one input inductor L, two output capacitors C_1 and C_2, two output diodes D_1 and D_2, and one output load resistor R_o.

3 Basic operating principles

The voltage and current symbols shown in Fig. 1*b*, and the assumptions are given as follows: (i) V_i is the DC input voltage; (ii) V_o is the DC output voltage; (iii) i_{L_r} is the current flowing through the resonant inductor L_r; (iv) v_{Cs1} and v_{Cs2} are the voltages across the parasitic capacitances C_{s1} and C_{s2} or the main switches S_1 and S_2, respectively; (v) the components are ideal except that the parasitic diodes and capacitances on the main switches are taken into account; (vi) the value of the input inductor L is large enough to keep the input current constant at a given value I_i, which is the DC component of the input current; and (vii) the values of the output capacitors C_1 and C_2 are large enough to keep the output voltages constant at given values, V_{C1} and V_{C2}, which are both equal to $0.5V_o$.

It is noted that Fig. 1*b* shows the equivalent circuit of the proposed circuit in Fig. 1*a*. There are seven operating states in the proposed ZVT three-level boost converter as follows. Fig. 2 shows the illustrated waveforms.

(1) *State 1* $[t \le t_o]$: As shown in Fig. 3*a*, during this state, the auxiliary switch S_a and the main switch S_1 are both turned off, but the diode D_1 is turned on. At the same time, the current I_i flows through the diode D_1 and hence the current i_{d1} is equal to the current I_i. Also, the voltage across the parasitic capacitor C_{s1} is $0.5V_o$. As soon as the auxiliary switch S_a is turned on, the operating state proceeds to state 2.

(2) *State 2* $[t_0 \le t \le t_1]$: As shown in Fig. 3*b*, during this state, the auxiliary switch S_a and the diode D_1 are still turned on but the main switch S_1 is still turned off. At the same time, the current in the resonant inductor L_r, i_{L_r}, is linearly increasing and the current in the diode D_1, i_{d1}, is linearly decreasing. Before the resonant current i_{L_r} reaches the current I_i, the diode D_1 still keeps turned on. In addition, the voltage across the parasitic capacitor C_{s1} still keeps constant at $0.5V_o$. Once the current i_{L_r} rises to the current I_i, the diode D_1 is turned off and the operating state goes to state 3. The associated equations can be obtained:

$$\begin{cases} i_{L_r}(t) = \dfrac{1}{L_r}\displaystyle\int_{t_0}^{t} \frac{V_o}{2}\,\mathrm{d}t + i_{L_r}(t_0) = \frac{V_o}{2L_r}(t - t_0) \\ v_{Cs1}(t) = \dfrac{V_o}{2} \end{cases} \tag{1}$$

doi: 10.1049/joe.2017.0149

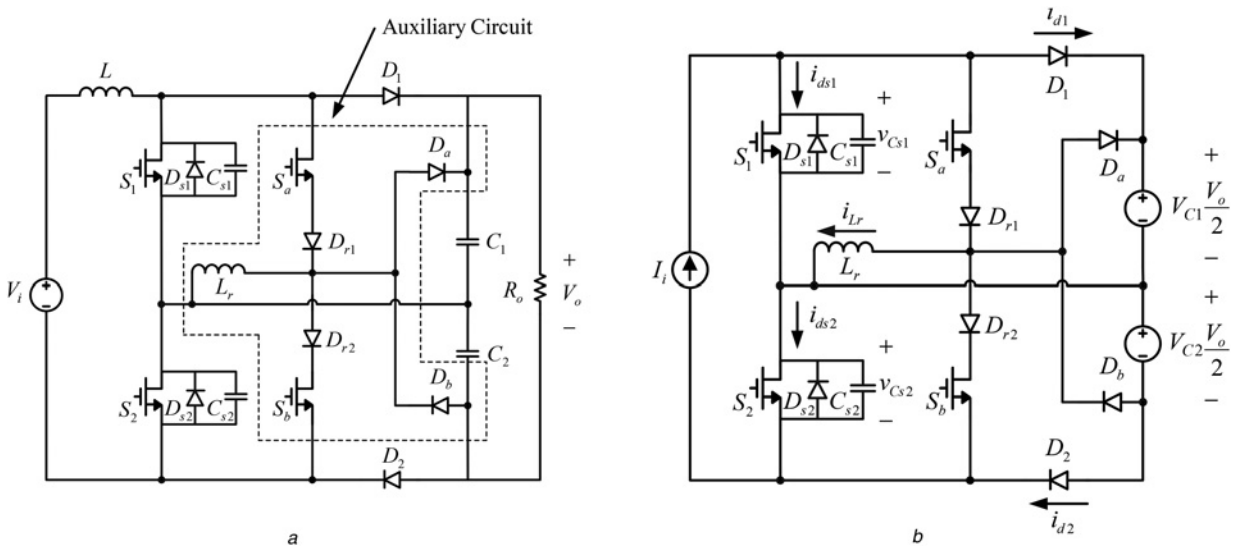

Fig. 1 *Proposed three-level boost converter with ZVT*
a Original circuit
b Equivalent circuit

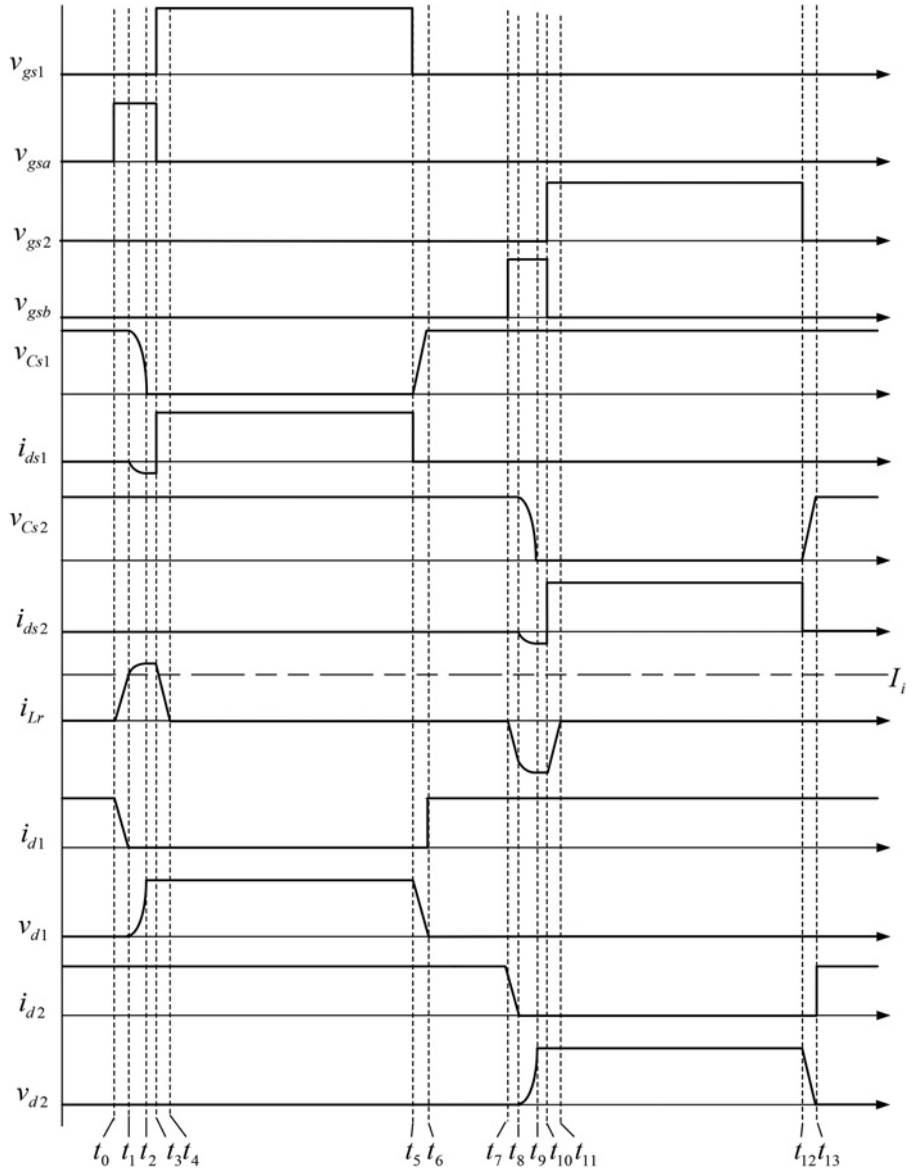

Fig. 2 *Illustrated waveforms relevant to the proposed converter*

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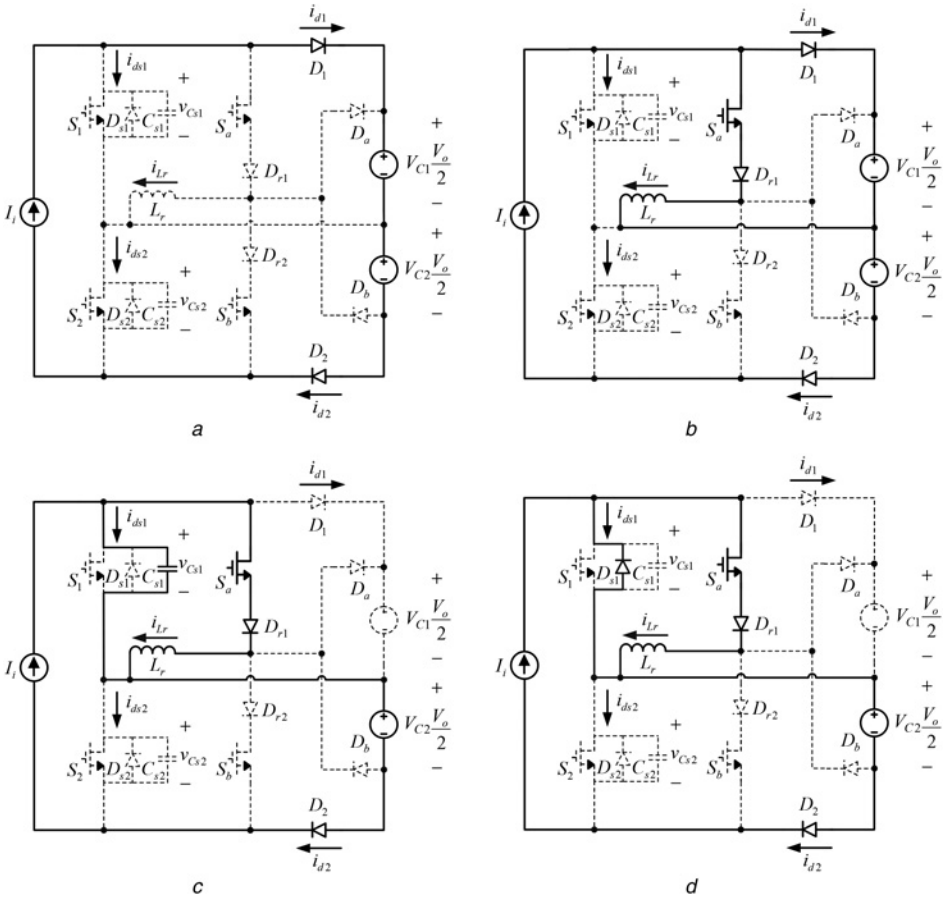

Fig. 3 *Current flow paths*
a State 1
b State 2
c State 3
d State 4

Also, the elapsed time can be obtained to be

$$(t_1 - t_0) = \frac{2I_i L_r}{V_o} \tag{2}$$

(3) *State 3* $\left[t_1 \le t \le t_2\right]$*:* As shown in Fig. 3*c*, during this state, the auxiliary switch S_a still keeps turned on so as to make the resonant inductor L_r resonate with the parasitic capacitor C_{s1}. At the same time, the resonant capacitor C_{s1} discharges such that the voltage v_{Cs1} decreases but the current i_{L_r} increases. The moment the voltage v_{Cs1} drops to zero, the operating state proceeds to state 4. The relevant equations can be obtained to be

$$\begin{cases} i_{L_r}(t) = I_i + \dfrac{V_o}{2Z_r}\sin\omega_r(t - t_1) \\ v_{Cs1}(t) = \dfrac{V_o}{2}\cos\omega_r(t - t_1) \end{cases} \tag{3}$$

Also, the elapsed time required in this state can be obtained to be

$$t_2 - t_1 = \frac{\pi}{2}\sqrt{L_r C_{s1}} \tag{4}$$

The maximum resonant current $I_{\text{Lr-max}}$ can be expressed by

$$I_{\text{Lr}-\max} = I_i + \frac{V_o}{2Z_r}\sin\left(\frac{1}{\sqrt{L_r C_{s1}}} \times \frac{\pi}{2} \times \sqrt{L_r C_{s1}}\right) = I_i + \frac{V_o}{2Z_r} \tag{5}$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{6}$$

(4) *State 4* $\left[t_2 \le t \le t_3\right]$: As shown in Fig. 3*d*, during this state, the auxiliary switch S_a still keeps turned on. Since the voltage across the parasitic capacitor C_{s1} is zero, the body diode of the main switch S_1, called D_{s1}, is turned on, thereby making the resonant current kept constant. At the instant of t_3, if the main switch S_1 is turned on, then the ZVT turn-on of S_1 can be achieved. As soon as S_1 is turned on, the operating state goes into state 5. Also, the elapsed time required in this state should be as short as possible, so as to reduce the loss created from the circulating current. Accordingly, the elapsed time from state 1 to state 4 can be estimated to be

$$0 \sim t_3 \cong \frac{2I_i L_r}{V_o} + \frac{\pi}{2}\sqrt{L_r C_{s1}} \tag{7}$$

(5) *State 5* $\left[t_3 \le t \le t_4\right]$*:* As shown in Fig. 4*a*, during this state, the auxiliary switch S_a is turned off but the main switch S_1 is turned on. At the same time, the voltage across S_a is clamped at the output voltage V_o, and the energy stored in the resonant inductor L_r is transferred to the output capacitor C_2, thereby causing the current i_{L_r} to be decreased. Once the current i_{L_r} drops to zero, the operating state proceeds to state 6.

(6) *State 6* $\left[t_4 \le t \le t_5\right]$*:* As shown in Fig. 4*b*, during this state, the auxiliary switch S_a is still turned off but the main switch S_1 is still turned on. Since the current i_{L_r} is zero, the voltage clamp diode D_b

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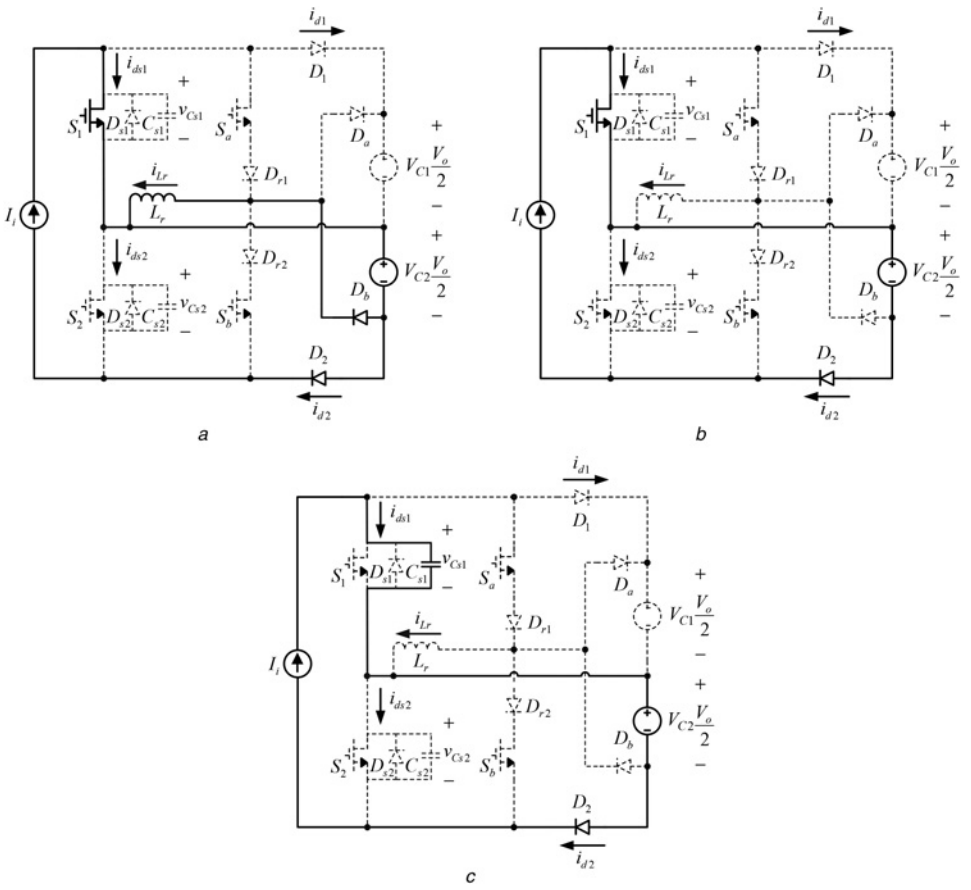

Fig. 4 *Current flow paths*
a State 5
b State 6
c State 7

is naturally turned off. At the same time, the current flowing through S_1 is kept constant at the current I_i. The moment the main switch S_1 is turned off, the operating state goes into state 7.

(7) *State 7* $[t_5 \le t \le t_6]$: As shown in Fig. 4*c*, during this state, the auxiliary switch S_a is still turned off and the main switch S_1 is turned off. At the same time, the current I_i charges the parasitic capacitance C_{s1}, thereby causing v_{Cs1} to linearly rise. As soon as the output diode D_1 is conducted, the operation of phase 2 begins, similar to the operation of phase 1 from state 1 to state 7. As soon as the operation of phase 2 comes to an end, the next cycle begins.

4 Output voltage balance strategy

Fig. 5 shows the voltage balance strategy without the ZVT circuit taken into account. First, the voltage divider ratios k_1 and k_2 are used to obtain the voltage messages on V_o and V_{C2}, respectively, where the value of k_2 is double the value of k_1. These sensed voltages are sent to the analogue-to-digital converters *ADC*1 and *ADC*2 to get the digital values V_1 for V_o and V_2 for V_{C2}, respectively. After that, the voltage reference V_{ref} minus the voltage V_1 is sent to the controller $G_{C1}(z)$ to generate the voltage V_a, whereas the voltage V_1 minus the voltage V_2 is sent to the controller $G_{C2}(z)$ to yield the voltage V_b. Finally, V_a plus V_b is sent to the pulse width modulation (PWM) generator 1 to create a suitable gate driving signal M_1 to drive the main switch S_1, whereas V_a minus V_b is sent to the PWM generator 2 to create a suitable gate driving signal M_2 to drive the main power switch S_2. It is noted that $V_o = V_{C1} + C_{C2}$.

For analysis convenience, it is assumed that the voltage V_{C1} is larger than the voltage V_{C2}. From Fig. 5 and the preceding

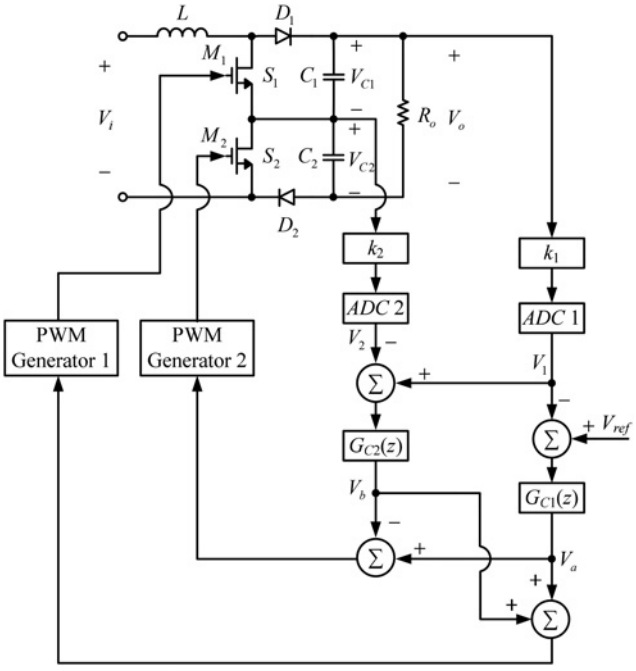

Fig. 5 *Voltage balance control strategy*

description, the voltage V_b is larger than zero, meaning that the duty cycle for the gate driving signal M_2 is reduced, whereas the duty cycle for the gate driving signal M_1 is increased.

doi: 10.1049/joe.2017.0149

Accordingly, the voltage V_{C2} will be increased and the voltage V_{C1} will be decreased. Regarding the condition that V_{C1} is smaller V_{C2}, the corresponding operation principle is similar to the condition that V_{C1} is larger than V_{C2}.

5 Design considerations

The specifications of the system and components are described in Table 1 as follows.

5.1 Design of input inductor

Since the input voltage range is from 21.6 to 26.4 V, and the proposed ZVT three-level converter operates in continuous current mode (CCM) above the output power of 10 W, the minimum value of the input inductor L, $L_{\min}$, can be obtained based on the following equation:

$$L_{\min} = \frac{V_{\text{in,max}}^2 D_{\min} T_s}{2P_{\text{o, min}}} = \frac{26.4^2 \times 0.267 \times 10\,\mu}{2 \times 10} = 93\,\mu\text{H} \quad (8)$$

Finally, the value of L is set at 100 μH.

Table 1 Specifications of the system and components

Operating mode	CCM
input voltage V_{in}	$24\,V \pm 10\%$
output voltage V_{o}	36 V
input inductor L	100 μH
resonant inductor L_{r}	0.9 μH
switching frequency f_{s}	100 kHz
rated output power $P_{\text{o-rated}}$/ rated output current $I_{\text{o-rated}}$	100 W/2.78 A
minimum output power $P_{\text{o-min}}$/ minimum output current $I_{\text{o-min}}$	10 W/0.278 A
parasitic capacitances C_{s1}, C_{s2} ($C_{s1} = C_{s2}$)	140 pF
output capacitors C_1, C_2 ($C_1 = C_2$)	330 μF

5.2 Design of output capacitors

It is assumed that two output capacitors C_1 and C_2 are identical and both have the capacitance C, and the voltage ripples on C_1 and C_2 are smaller than 0.1% of the output voltage V_{o}, the minimum capacitance C, $C_{\min}$, is

$$C_{\min} = \frac{V_{\text{o}} D_{\max} T_s}{\Delta V_{\text{o}} R_{\text{o}}} = \frac{36 \times 0.4 \times 10\,\mu}{0.001 \times 36 \times 13} \cong 308\,\mu\text{F} \quad (9)$$

Eventually, the values of C_1 and C_2 are both set at 330 μF.

5.3 Determination of C_{s1} and C_{s2}

Since both the main switches S_1 and S_2 have the maximum voltage stress of 18 V and the maximum current stress of 4.75 A without considering voltage and current spikes, two IRFZ24N metal-oxide semiconductor field-effect transistors (MOSFETs) with the parasitic capacitance of 140 pF are chosen for S_1 and S_2.

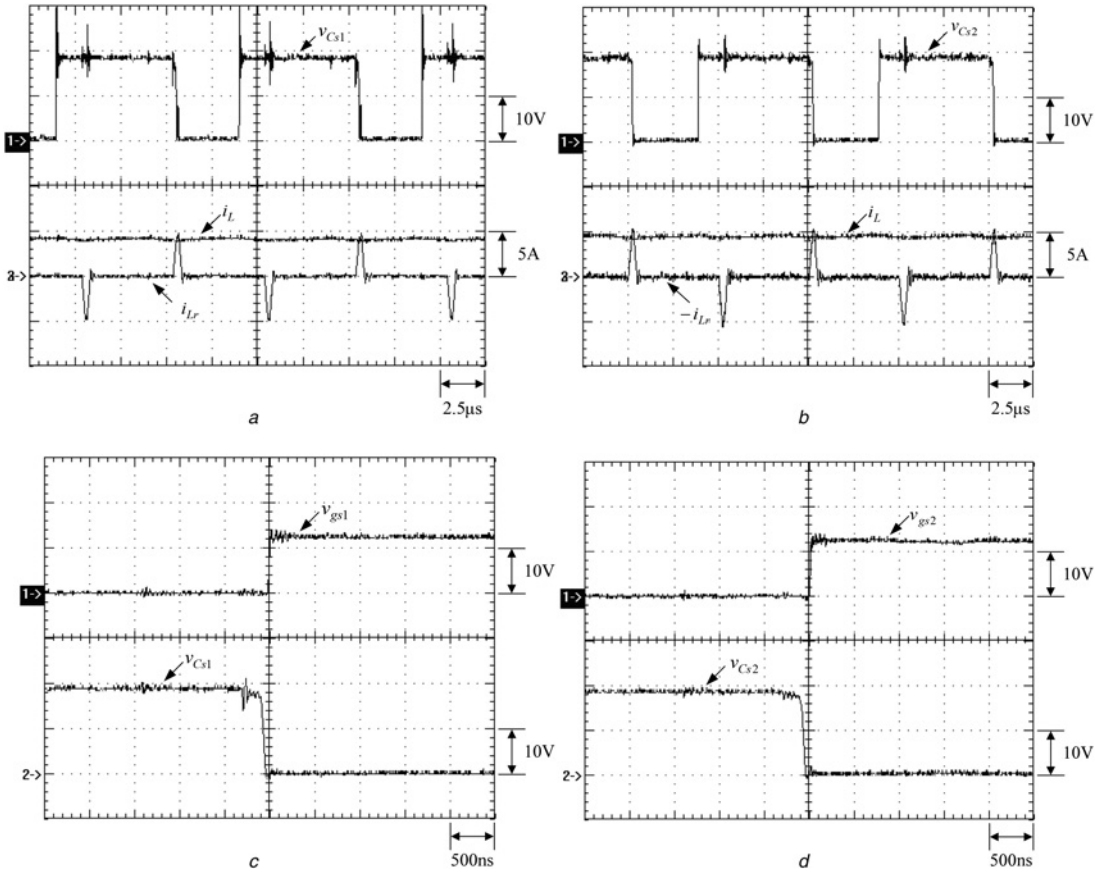

Fig. 6 *Waveforms at 100% load relevant to main switch voltages and inductor currents*
a (1) v_{ds1}, (2) i_L, (3) i_{L_r}
b (1) v_{ds2}, (2) i_L, (3) $-i_{L_r}$
c (1) v_{gs1}, (2) v_{Cs1}
d (1) v_{gs2}, (2) v_{Cs2}

doi: 10.1049/joe.2017.0149

5.4 *Determination of* L_r

Before the main switch S_1 (or S_2) is turned on, the auxiliary switch S_a (or S_b) should be conducted to achieve ZVT of S_1 (or S_2). The turn-on interval for S_a (or S_b) is generally set to be one-tenth of that for S_1 (or S_2), namely $D_{\min}T_s$, equal to 0.267 µs. From Section 3, it can be seen that there are three subintervals in the turn-on interval for S_a. The first subinterval is T_a from t_0 to t_1, and at the end of this subinterval, the current in the resonant inductor L_r is the input current I_i; the second subinterval is T_b from t_1 to t_2, and at the end of this subinterval, the voltage across the parasitic capacitor C_{s1} (or C_{s2}) is zero; the third subinterval is T_c from t_2 to t_3, and during this subinterval, only the current flowing through the body diode of S_1 (or S_2) makes T_c too small and

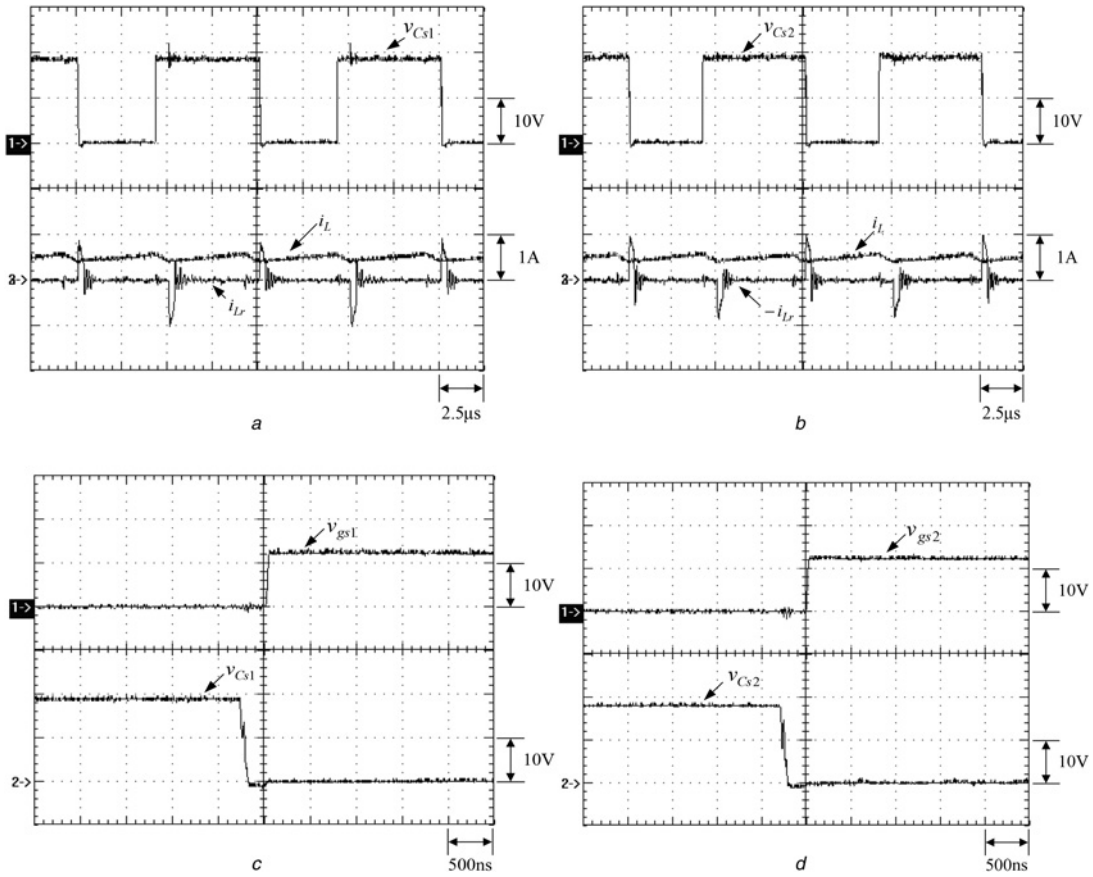

Fig. 7 *Waveforms at 10% load relevant to main switch voltages and inductor currents*
a (1) v_{ds1}, (2) i_L, (3) i_{L_r}
b (1) v_{ds2}, (2) i_L, (3) $-i_{L_r}$
c (1) v_{gs1}, (2) v_{Cs1}
d (1) v_{gs2}, (2) v_{Cs2}

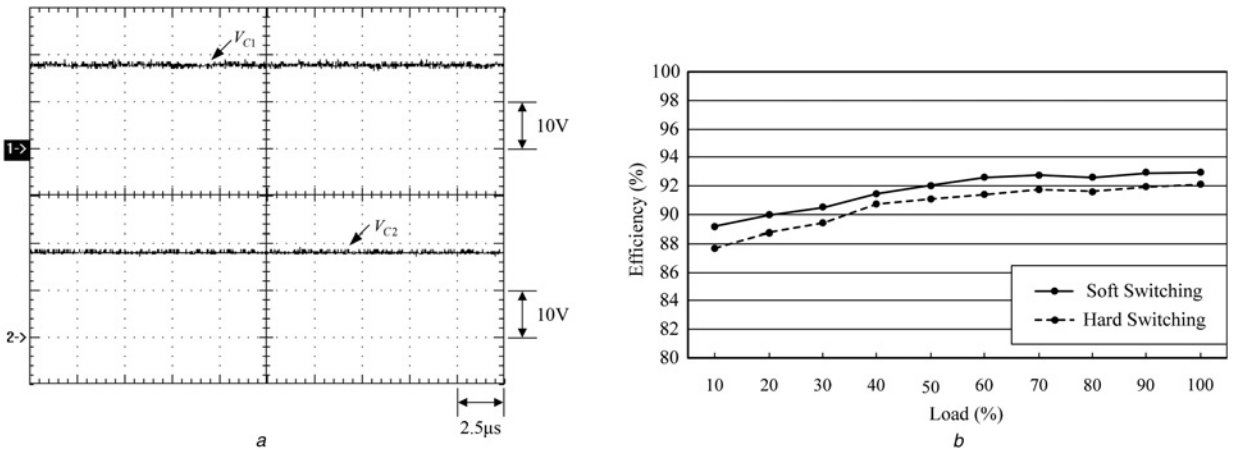

Fig. 8 *Voltages across the output capacitors*
a Waveforms at rated load: (1) V_{C1}; (2) V_{C2}
b Curves of efficiency versus load with soft switching and hard switching

doi: 10.1049/joe.2017.0149

omitted. As S_1 (or S_2) is turned on at the instant of t_3 or later, S_1 (or S_2) is turned on with ZVT. Therefore,

$$T_a + T_b = \frac{2I_i L_r}{V_o} + \frac{\pi}{2}\sqrt{L_r C_{s1}} = 0.267\,\mu s \tag{10}$$

Substituting $C_{s1} = C_{s2} = 140\,pF$, $I_i = 4.63\,A$ and $V_o = 36\,V$ into (10) yields

$$L_r = 1.03\,\mu H \tag{11}$$

Eventually, the value of L_r is set at 1 μH.

6 Experimental results

Under the input voltage of 24 V and 100% of the rated load, Fig. 6*a* shows the voltage across S_1, v_{Cs1}, the current in the inductor L, i_L, and the current in the resonant inductor L_r, i_{L_r}, whereas Fig. 6*b* shows the voltage across S_2, v_{Cs2}, the current in the inductor, i_L, and the current in the resonant inductor L_r, $-i_{L_r}$; Fig. 6*c* shows the gate driving signal for S_1, v_{gs1}, and the voltage across S_1, v_{Cs1}, whereas Fig. 6*d* shows the gate driving signal for S_2, v_{gs2}, and the voltage across S_2, v_{Cs2}. Under the input voltage of 24 V and 10% of the rated load, Fig. 7 shows the same waveform items as Fig. 6; Fig. 8*a* shows the voltages across the output capacitors C_1 and C_2, V_{C1} and V_{C2}; Fig. 8*b* shows the curves of efficiency versus load for soft switching and hard switching.

From Figs. 6*a* and 7*a* or (Figs. 6*b* and 7*b*), it can be seen that once the absolute value of i_{L_r} (or $-i_{L_r}$) is larger than the value of i_L, the value of v_{Cs1} (or v_{Cs2}) will drop to zero, the main switch S_1 (or S_2) is turned on with ZVT as shown in Figs. 6*c* and 7*c* (or Figs. 6*d* and 7*d*). That is, two main switches have ZVT turn-on from the minimum load to the rated load. In addition, from Fig. 8*a*, the voltages across C_1 and C_2 are almost equal to 12 V, meaning that the voltage balance performs well. Furthermore, Fig. 8*b* shows that as compared with the hard-switching three-level boost converter, the efficiency of the soft-switching three-level boost converter can be improved up to ∼1.4% and the efficiency at the rated load is improved by 0.8%.

7 Conclusion

In this paper, a ZVT three-level boost converter is presented. The experimental results that the main switches S_1 and S_2 can be turned on at zero voltage during from the minimum load to the rated load. With the voltage balance control, the output voltage can be equally shared by the capacitors C_1 and C_2. Moreover, as compared with the hard-switching three-level boost converter, the efficiency of the soft-switching three-level boost converter can be improved up to ∼1.4% and the efficiency at the rated load is improved by 0.8%.

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