

Performance analysis of single-electron transistor at room-temperature for periodic symmetric functions operation

Mostafa Miralaie, Ali Mir

Faculty of Engineering, Lorestan University, Khoram-Abad, Iran
E-mail: mir.a@lu.ac.ir

Published in *The Journal of Engineering*; Received on 14th May 2016; Accepted on 19th May 2016

Abstract: For the first time, the authors have investigated the analysis of the room-temperature operation of single-electron transistor (SET) for periodic symmetric functions (PSFs). They demonstrate that in SETs due to the Pauli exclusion principle the distance between current peaks against bias voltage in coulomb oscillations will be asymmetric. Also, because the separated energy levels have unequal tunnel-barrier resistance, different tunnelling current rates are obtained for each level. So, the unequal peak-to-valley current ratio (PVCR) will be observed in the coulomb oscillations, and therefore the operation of room-temperature of silicon SET-based PSFs is impossible.

1 Introduction

Attempt to integrate sub-10 nm scaled complementary metal-oxide-semiconductor (CMOS) devices will face physical limitations in the near future. To tackle this problem several ideas have been proposed, where one of the most promising tends to use the Coulomb blockade mechanism in conducting island/tunnel junction systems to accurately control the current in single-electron devices [1–6]. The single-electron transportation regime is a direct result of the addition of an electron to the island. The average number of electrons on the island can change discretely due to quantum mechanical effects and electron–electron interactions. The electron addition energy, E_a , associated with changing the charge on the island can be defined as the energy involved in adding a single electron and is generally written as the sum of two contributions. The first contribution is the energy gap between the quantised energy levels, ΔE , which is the energetic cost of promoting an electron on the island from the highest occupied energy level to the lowest unoccupied energy level. The second contribution is the charging energy, E_c , which accounts for the Coulomb interactions on the island. A common approximation for the electron–electron fsinteractions on the island is to define a classical total capacitance, C_Σ , which can be calculated as $E_c = e^2/C_\Sigma$ [1–6].

Single-electron transistors (SETs) have been widely studied because of their unique multifunctionality with ultra-low power dissipation and scalability down to the sub-nanometre regime and several SET modelling approaches have been proposed in the literature [4–8]. However, almost Coulomb blockade and Coulomb oscillation manner have fully explored the inherent SET characteristics, and also the temperature effect is usually ignored in the design.

Thermal variations stifle most of the single-electron effects and ruin the ideal transport mechanism barring $k_B T \ll E_a$. In this condition, during operation at room-temperature, the electron addition energy, E_a , may be as large as a few electron-volts (eV) that can be implemented by diminishing the size of the SET island to less than a few nanometres. Reduction in the size of island below ~ 2 nm can lead to a drastic improvement in the performance of a room-temperature SET. At this scale, the total island capacitance C_Σ may be ~ 0.5 aF or even smaller, with single-electron charging energies $E_c \gg k_B T \sim 26$ meV at room-temperature. Hence, SETs with islands of about 2 nm in size are more encouraging than islands > 2 nm. Moreover, the effects of the discrete energy levels of islands on SET may become important, especially at room-temperature.

The metallic islands of about 2 nm and quantum dots (QDs) of about 10 nm in size have an energy-levels spacing, ΔE , which is typically smaller than the charging energy. This means that only a

discrete electron charge reveals in the conductance as a result of the Coulomb repulsion of individual electrons ($E_a = E_c$). Therefore, the blockade behaviour is notable since $k_B T \ll E_c$ which is known as the classical Coulomb blockade regime (Orthodox theory). For quantisation of energy levels of the non-metallic islands (QDs smaller than 10 nm in size) and ultra-small nanoparticles (metallic islands smaller than 2 nm in size), ΔE will be comparable with the charging energy E_c . This leads to $E_a = E_c + \Delta E$. In this situation, the blockade behaviour is notable at higher temperatures as the quantum Coulomb blockade regime [9–17]. Therefore, we can identify three temperature regimes: (i) $e^2/C_\Sigma \ll k_B T$, where the discreteness of charge cannot be discerned. (ii) $\Delta E \ll k_B T \ll e^2/C_\Sigma$, the classical or metallic Coulomb blockade regime, where many levels are excited by thermal variations. (iii) $k_B T \ll (\Delta E, e^2/C_\Sigma)$, the quantum Coulomb blockade regime, where only one or a few levels contribute in transport. SETs are typically analysed using Orthodox theory (the classical Coulomb blockade regime), where quantisation of energy levels in the island is entirely ignored. It should be noted that this assumption is valid only for the metallic islands of about 2 nm and QDs of about 10 nm in size. Therefore, the quantum Coulomb blockade regime should be considered in calculating the transport characteristics of 2 nm or < 2 nm silicon (Si) QD-based SET.

Periodic symmetric functions (PSFs) based on SET fully utilises Coulomb oscillation effect. SETs based PSF implementation is based on a two-SET complementary structure [18]. This class of functions is of particular interest as numerous computer arithmetic operations belong to it, e.g. parity, counting, and addition [19]. Moreover, digital converter operation can be described as a PSF [20]. Though PSF based on SETs has shown good advantages such as high integration density, ultra-low power dissipation, and extremely simple structure, but a serious problem will be remained. PSF based on the SETs are validated only within lower-temperature operation. So, for the first time, this paper has challenged the performance of the SETs based PSF operating at the room-temperature.

This paper is organised as follows. In Section 2, the modelling theory and the voltage–current characteristics of 2 nm islands based SET are presented. The challenges of the room-temperature operation of PSF based on SETs are stated at Section 3. Finally, conclusion is brought in Section 4.

2 Modelling and simulation methodology

2.1 Change in the free energy of the system

Schematic of an equivalent circuit of an SET is shown in Fig. 1, where an island is surrounded by drain, source, and gate electrodes.

The all mentioned electrodes are coupled to the island, capacitively. Any change in the applied potential of each of the SET electrodes, enforces an electrostatic energy variation of the island. Only the electrodes of source and drain are coupled to the island by tunnelling capability, so transportation of electron is allowed only between the island and these two electrodes. Therefore, the number of electrons in the island, n , is well defined. We assume that all electron–electron interactions in the island or on the electrodes can be parameterised by the total capacitance C_Σ and it does not depend on different charge states of the island. Considering into account that the total capacitance with an r -diameter island equals $C_\Sigma = 4\pi\epsilon_0\epsilon_r r$, one can measure the exact value of the source, drain, and gate capacitors using the equation $C_\Sigma = C_s + C_d + C_g$.

Helmholtz's free energy is responsible of electron transportation through an SET, and is defined as difference between the total energy stored in the SET and the work is required to be done by the power sources [5, 6]. When, the amount of the electrons changes from n to $n+1$, the free energy of the system changes from $F(n)$ to $F(n+1)$. The variation in the free energy can be expressed as

$$\Delta F(n, n+1) = F(n+1) - F(n) \quad (1)$$

In the Orthodox theory which is commonly used for describing the SET devices operation based on islands where energy quantisation is ignored (The metallic islands of about 2 nm and QDs of about 10 nm in size.), the variation of free energy, ΔF , for electrons during electron tunnelling from the 'initial' to the 'final' regions equals to the electrostatic energy contributed by Helmholtz's free energy. By introducing energy quantisation for islands, energy gaps between the quantised energy levels should be added to ΔF . An analytical model for SETs considering the discrete quantum energy states is proposed by two different groups, Miyaji *et al.* [21] and Dan and Mahapatra [22]. Implicit in their discussion is the assumption that energy-levels degeneracy and the Pauli exclusion principle (the spin degeneracy of the energy level) can be ignored. The first assumption is valid because, under realistic conditions of room-temperature operation of QD-based SETs, the interactions usually involve just the first energy levels (ground state and first excited state). The second assumption is the influence of spin-up and spin-down degenerate energy levels in deriving the ΔF equations for $n \rightarrow n+1$ transitions has not been considered. Here, we have no reason to distinguish spin polarisation, and therefore we assume that both configurations contribute in equal part to the state occupation. However, spin-dependent transport occurs in the presence of ferromagnetic electrodes [23, 24]. This assumption causes an unrealistic intuition with respect to the position of each current peaks. That is why, the Pauli's exclusion principle should considering into ΔF . The modified equations will become

$$\Delta F_{s,i} = \frac{e}{C_\Sigma} \left[C_d V_{ds} + C_g V_{gs} - ne - \frac{e}{2} \right] - N\Delta E \quad (2-1)$$

$$\Delta F_{i,s} = \frac{e}{C_\Sigma} \left[-C_d V_{ds} - C_g V_{gs} + ne - \frac{e}{2} \right] - N\Delta E \quad (2-2)$$

$$\Delta F_{i,d} = \frac{e}{C_\Sigma} \left[(C_s + C_g) V_{ds} - C_g V_{gs} + ne - \frac{e}{2} \right] - N\Delta E \quad (2-3)$$

$$\Delta F_{d,i} = \frac{e}{C_\Sigma} \left[-(C_s + C_g) V_{ds} + C_g V_{gs} - ne - \frac{e}{2} \right] - N\Delta E \quad (2-4)$$

where N equals to

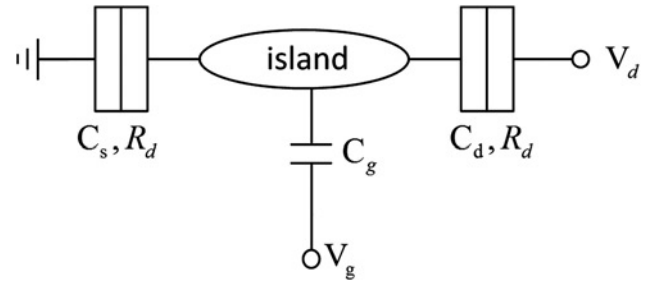


Fig. 1 Equivalent circuit model for an SET device

$$N = \begin{cases} \left(\frac{n+2}{2} \right), & \text{even } n \\ \left(\frac{n+1}{2} \right), & \text{odd } n \end{cases} \quad (3)$$

Here, e is the electron charge, C_Σ is the total island capacitance with respect to ground (equals to $C_G + C_D + C_S$), n denotes the number of electrons in the island, and s , i , and d refer to the source, island, and drain regions, respectively.

In [21, 22], Miyaji *et al.* and Dan and Mahapatra also assumed equal broadening for all energy levels; however, this assumption cannot be included because, as illustrated in the next section, different energy levels are associated with distinct energy broadenings when coupled with electrodes.

2.2 Tunnelling rates across the tunnel junctions

Si SETs are appearing to be more promising than metallic SETs for their possible integration with CMOS and requirements for CMOS-compatible processes. SETs are normally studied on the basis of the Orthodox theory, but one cannot neglect the energy quantisation in a small island (metallic islands smaller than 2 nm and QDs smaller than 10 nm in size), and also it is extremely important to study the effects of energy quantisation on Si SET circuit performance.

In this paper, SIMON Monte Carlo simulator has been used [25]. Simulation of energy quantisation effect in SIMON is not so straightforward such as simulation of metallic SETs where energy quantisation was ignored. SIMON simulates the discrete energy levels of the island as Lorentzian-shape functions, whose height H and width W parameters are related to the energy dependence of the transmission probability, which depends on the tunnel-barrier resistance [22]. Also assumed that the single-electron charging energy, E_c , and the energy-levels spacing, ΔE , are two separate processes.

The Orthodox theory describes charge transport under the influence of Coulomb blockade and its expression for single-electron tunnelling rate across the junction is [4, 6]

$$\Gamma(n, n+1) = \frac{1}{e^2 R_T} \frac{-\Delta F}{[1 - \exp(\Delta F/k_B T)]} \quad (4)$$

Here, R_T is the resistance of the tunnel junction involved in the tunnelling (or tunnel resistance), and ΔF is the corresponding variation in the electrostatic energy of the circuit when an electron tunnels on/off the island. For islands with discrete energy levels, in order to calculate the total tunnelling rate one typically starts from Fermi's Golden Rule (as followed in Orthodox theory). However, it is not possible to consider the tunnelling transmission probability, $T_{i,f}$, to be constant at all energy levels given the energy-level broadening concept. A realistic point of view requires different broadening levels for each discrete energy level. This can be modelled by including the contribution of a Lorentzian function in the tunnelling

transmission probability as follows [26]

$$T_{i,f}(E) = \sum_n \alpha_n \frac{(\gamma_n/2)^2}{(E - E_n)^2 + (\gamma_n/2)^2} \quad (5)$$

where E_n ($n = 0, 1, 2, \dots$) are discrete energy levels (due to quantisation) in the island, determined by solving the Schrodinger equation, and γ_n , which describes the half-width of the local density of states peak, is a parameter related to the ‘escape frequency’ of an electron on the island (a term used to denote the amount of broadening for any particular energy state). The transmittance strength parameter, α_n , with $(0 \leq \alpha_n \leq 1)$, allows us to classify tunnel barriers according to their transparency, i.e. height and width. Using this formulation, deriving the tunnelling rate expression from first principles (as followed in Orthodox theory) for the realistic case of infinite number of energy states, leads to the same expression (4), with the tunnelling resistance term changing into

$$R_T^{\text{discrete}} = (R_T^{\text{orthodox}} \times T_{i,f}^{\text{orthodox}}) / \left[\alpha_n \frac{(\gamma_n/2)^2}{(E - E_n)^2 + (\gamma_n/2)^2} \right] \quad (6)$$

In this equation, R_T^{orthodox} and R_T^{discrete} represent the Orthodox theory tunnelling resistance for islands with continuous energy levels and the tunnelling resistance for islands with discrete energy levels, respectively. $T_{i,f}^{\text{orthodox}}$ also stands for the Orthodox theory transmission probability, which has a constant value.

According to (6), H and W parameters are used to determine the tunnel-barrier resistance in the quantum Coulomb blockade regime in SIMON. W represents the broadening size of any clear energy level in an island (γ_n) and determines the tunnelling transmission probability spectrum, and H used to determine the final height of the probability spectrum.

2.3 Calculation of the V - I characteristics

Now, we sweep the gate voltage and calculate the drain current (transconductance) as a function of V_g for 2 nm Si QD-based SET (Fig. 2). The values of the parameters used in simulations are given in Table 1.

It is obvious from Fig. 2 and Table 1 that the transconductance plot would be tracked precisely with the one obtained by experimental investigation, as illustrated in [10].

We found that in the linear response regime (i.e. $V_{ds} \ll \Delta E/e$, e/C_Σ) to an electrochemical potential, transconductance is changed linearly by the gate voltages proportional to α ($=C_g/C_\Sigma$) factor. The α -factor relates the peak spacing in the gate voltage to the addition energy: $E_a(n) = e\alpha(V_g^{n+1} - V_g^n)$ where V_g^n and V_g^{n+1} are the gate voltages of the n th and $(n+1)$ th Coulomb peaks, respectively.

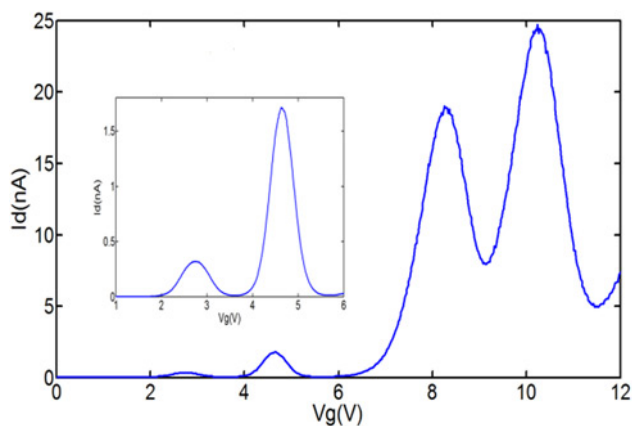


Fig. 2 Drain current against gate voltage of a 2 nm Si QD-based SET

Table 1 Parameters used in the simulation

2 nm Si QD-based SET parameters	Unit	Value
C_s , source junction capacitance	F	1.71×10^{-19}
C_d , drain junction capacitance	F	1.71×10^{-19}
C_g , gate capacitance	F	0.92×10^{-19}
C_Σ , island total capacitance	F	4.34×10^{-19}
$R_{T\text{orthodox}}$, Orthodox tunnelling resistance	Ω	1.5×10^6
ΔE , levels spacing	eV	0.43
H , height multiplication factor	–	1
W_1 , first energy-state broadening	eV	0.0005
W_2 , second energy-state broadening	eV	0.005
W_3 , third energy-state broadening	eV	0.06
W_4 , fourth energy-state broadening	eV	0.12
V_{ds} , drain–source voltage	V	0.05
T , temperature	K	300

So, the corresponding gate voltage difference between any two current peaks, with respect to the number of electrons in the QD, can be calculated as

$$\begin{cases} \Delta V_{\text{peak}}^n = \frac{C_\Sigma}{C_g} \left(\frac{e}{C_\Sigma} \right) = \frac{e}{C_g} & n \text{ odd} \\ \Delta V_{\text{peak}}^n = \frac{C_\Sigma}{C_g} \left(\frac{e}{C_\Sigma} + \Delta E \right) & n \text{ even} \end{cases} \quad (7)$$

As illustrated in Fig. 2 and (7), the distance between current peaks are unequal. The reason for this phenomenon is the Pauli’s exclusion principle. Also Fig. 2 states that the magnitude of the current peak increases with improvement in the number of electrons in the QD. This may be due to the exponential dependence of energy level broadening on the height and the width of the potential barrier (i.e. the tunnel-barrier resistance). On the other hand, the height of the tunnel barrier degrades by the electric field of the gate, and consequently a corresponding enhancement in the broadening of energy level has occurred (i.e. unequal energy levels broadening), which leads to an exponential growth in tunnelling probability [see, (6)]. Therefore, the current peaks become broader and higher by enlargement in the V_g , i.e. the unequal peak-to-valley current ratio (the unequal peak-to-valley current ratio (PVCR)). Our description matches completely with the experimental results [10–16]. The two first current peaks, attributed to the up-spin and down-spin energy states of the ground level, are much lower than the third and the fourth energy states, which are related to the two energy states (up-spin and down-spin) of the first excited level. Therefore, PVCR due to the ground level is smaller than the

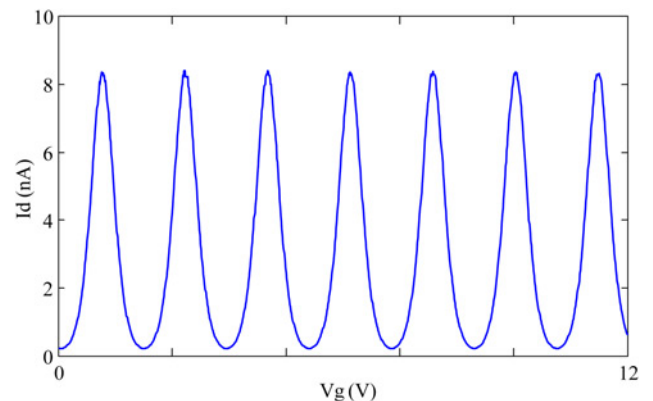


Fig. 3 Drain current against gate voltage of the 2 nm metal island-based SET

excited level. This is well known to be the smearing out of the Coulomb blockade condition by tunnel-barrier lowering effect.

To show differences between the results of simulation with broadening and without broadening on each energy level, we have drawn the drain current against gate voltage of the 2 nm metallic island-based SET in Fig. 3.

It is obvious that current peak magnitudes are constant in 2 nm metallic island because the tunnelling transmission probability is considered as constant at all energy levels. However, in Si QD with 2 nm diameter due to the unequal energy levels broadening (i.e. unequal tunnelling transmission probability), current peak magnitudes are not equal to each other. So, the energy levels broadening phenomenon and its effect on the amplitudes of the current peaks are obvious, while it can be neglected in metallic islands of about 2 nm in diameter.

3 Results and discussion

The complementary structure with two SETs was first proposed by Tucker and is similar to a CMOS inverter circuit in structure [6]. Tucker is focused on the inverter behaviour of such a structure in [7]. However, this topology can be used to produce more than an inverter function. In this section, we implement a simple PSF circuit based on a complementary SET inverter consisting of two SETs [18, 20]. Fig. 4 shows the equivalent circuit for SET-based PSF.

3.1 Performance analysis of metal SET-based PSFs at room-temperature

From Fig. 3, one can conclude that due to the periodic Coulomb oscillations and equal current peaks, designing PSFs based on these islands at room-temperature is achievable. Therefore in the following, we discuss the possibility of implementation of the 2 nm metallic island-based-SET PSF at the room-temperature. Figs. 5 and 6 indicate $I_{ds}-V_g$ characteristics of the upper and lower SETs, respectively. The circuit parameters used in simulation are as follows: the supply voltage is 0.12 V and $V_{t2}=0.63$ V, $V_{t1}=-0.24$ V, $C_g=0.092$ aF, $C_\Sigma=0.434$ aF, and $R_1=R_2=1.5$ M Ω . The operating temperature is set at 100 and 300 K. Figs. 5 and 6 reveal that PVCr deteriorates with increasing the temperature (i.e. low PVCr at high temperatures).

To implement an SET-based PSF (with 50% duty ratio), we adjusted $V_{t1}=-0.24$ V and $V_{t2}=0.63$ V to attain a half-period phase shift of the Coulomb oscillations. Owing to the SET inherent Coulomb oscillations characteristics with the period of e/C_g , when the upper SET turns ON, the lower SET will switch to OFF. The

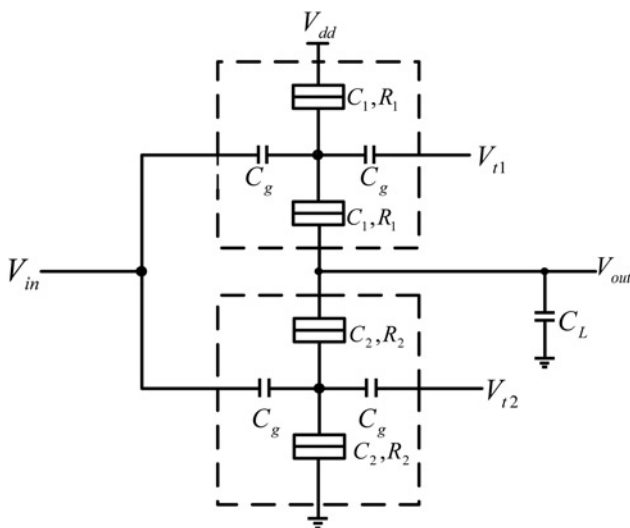


Fig. 4 Schematic of the generic PSF structure

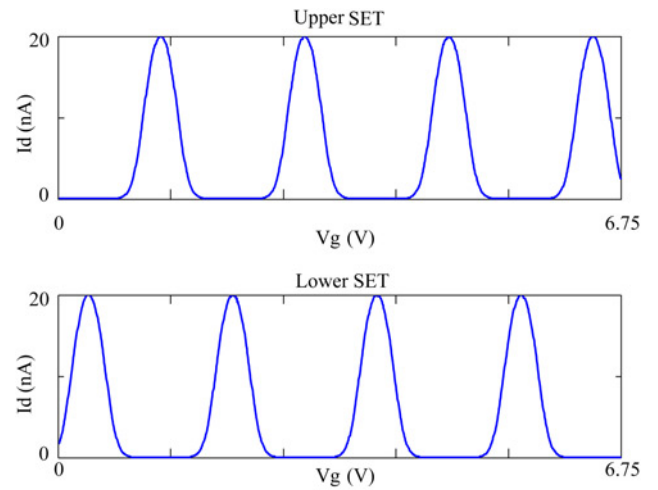


Fig. 5 I - V characteristics of upper and lower SET at 100 K

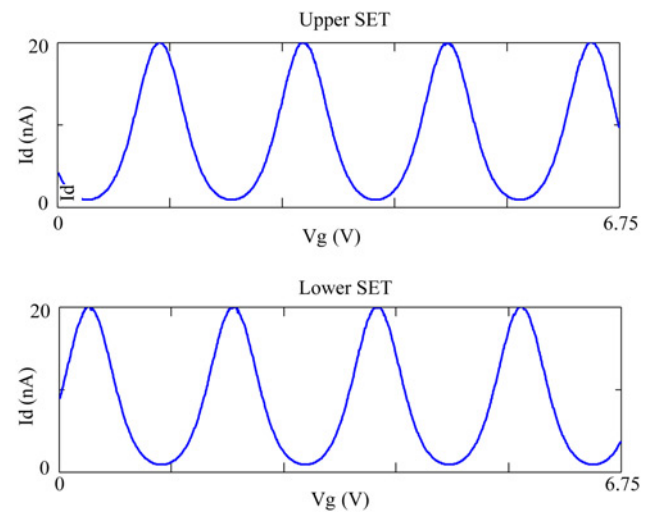


Fig. 6 I - V characteristics of upper and lower SET at 300 K

circuit parameters used in simulation are as follows: the supply voltage is 0.12 V, $V_{t2}=0.63$ V, $V_{t1}=-0.24$ V, $C_g=0.092$ aF, $C_\Sigma=0.434$ aF, $R_1=R_2=1.5$ M Ω , and $C_{Load}=10$ fF. Figs. 7 and 8 indicate the simulated conversion characteristics of the SET-based PSF at 100 and 300 K, respectively.

Fig. 7 demonstrate that a PSF circuit based on a 2 nm metallic island SET has an acceptable conversion characteristics at 100 K. However, it is clearly obvious from Fig. 8 that at the room-temperature (300 K) the signal conversion becomes more

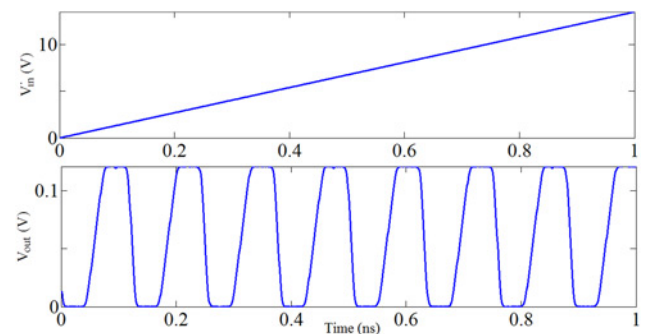


Fig. 7 Conversion characteristic of the PSF based on metal SET at 100 K

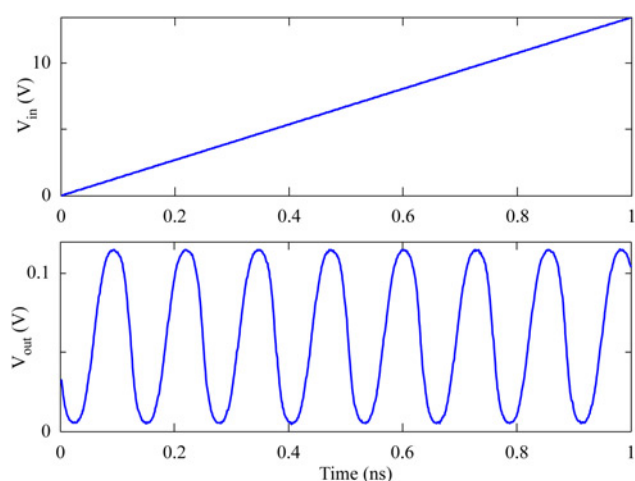


Fig. 8 Conversion characteristic of the PSF based on metal SET at 300 K

inaccurate. Switching performance degradation due to PVCRC reduction is its main reason in the SET current at high temperatures.

3.2 Performance analysis of Si SET-based PSFs at room-temperature

Using Fig. 2, one can conclude that due to the asymmetric Coulomb oscillations and the unequal PVCRC, designing PSFs based on these islands at room-temperature is impossible. According to the mentioned unequal energy-levels broadening and Pauli exclusion principle effects (due to the energy-levels quantisation), we can conclude that SET characteristics at room-temperature has asymmetric Coulomb oscillations and also unequal current peaks.

One challenge of the implementation of the Si SET-based PSFs operating at the room-temperature is the Pauli's exclusion principle effect, because the distance between current peaks in Coulomb oscillations are unequal (the asymmetric Coulomb oscillations). So, operation of the PSFs at the room-temperature is limited. The other challenge is the degradation of the switching performance due to the unequal PVCRC in the SET current at high temperatures. Therefore, Si QD-based SET PSFs at room-temperature never has a suitable output and operating Si SET-based PSFs at room-temperature is impossible.

4 Conclusion

We have been demonstrated the impossibility of the implementation of the PSFs operation based on 2 nm island-based SET operating at the room-temperature. The main reason of this challenge is the degradation of the switching performance due to the decreased PVCRC and the unequal PVCRC in the SET current at high temperatures. It was proposed that PVCRC can be improved by the scaling of the island size, but, for small islands, i.e. metallic islands smaller than 2 nm and QD smaller than 10 nm in size (due to the energy-levels quantisation effect), asymmetric Coulomb oscillations and unequal PVCRC would happen in the SET current. So, SET-based PSFs at room-temperature never had an accurate output.

5 References

- [1] Berman D., Brodsky M.G., Chan H.B., *ET AL.*: 'Single-electron transistor as a charge sensor for semiconductor applications', *Sci. Technol. B*, 1997, **15**, (6), pp. 2844–2847
- [2] Grabert H., Devoret M.H.: 'Single charge tunneling: coulomb blockade phenomena in nanostructures', NATO ASI Series (Plenum, New York, 1992)
- [3] Ferry D.K., Goodnick S.M.: 'Transport in nanostructures' (Cambridge University Press, Cambridge, England, 1997)
- [4] Likharev K.K.: 'Single-electron devices and their applications', *Proc. IEEE*, 1999, **87**, (4), pp. 606–632
- [5] Wasshuber C.: 'Computational single-electronics' (Springer-Verlag Press, New York, 2001)
- [6] Durrani Z.A.: 'Single-electron devices and circuits in silicon' (Imperial College Press, 2010)
- [7] Tucker J.R.: 'Complementary digital logic based on the Coulomb blockade', *J. Appl. Phys.*, 1992, **72**, (9), pp. 4399–4413
- [8] Heij C.P., Hadley P., Mooij J.E.: 'Single-electron inverter', *Appl. Phys. Lett.*, 2001, **78**, (8), pp. 1140–1142
- [9] Graf H., Vancea J., Hoffmann H.: 'Single-electron tunneling at room temperature in cobalt nanoparticles', *Appl. Phys. Lett.*, 2002, **80**, (7), pp. 1264–1266
- [10] Wang B., Wang K., Lu W., *ET AL.*: 'Effects of discrete energy levels on single-electron tunneling in coupled metal particles', *Appl. Phys. Lett.*, 2003, **82**, (21), pp. 3767–3769
- [11] Shin S.J., Jung C.S., Park B.J., *ET AL.*: 'Si-based ultra-small multi-switching single-electron transistor operating at room-temperature', *Appl. Phys. Lett.*, 2010, **97**, (10), pp. 103101–103103
- [12] Shin S.J., Lee J.J., Kang H.J., *ET AL.*: 'Room-temperature charge stability modulated by quantum effects in a nanoscale silicon Island', *Nano Lett.*, 2011, **11**, (4), pp. 1591–1597
- [13] Choi J.B.: 'Enhanced quantum effects in room-temperature coulomb blockade devices based on ultrascaled finFET structure'. Toward Quantum FinFET, October 2013 (*Lecture Notes in Nanoscale Science and Technology*, **17**), pp. 285–303, Chapter 12
- [14] Lee S., Lee Y., Song E.B., *ET AL.*: 'Observation of single electron transport via multiple quantum states of a silicon quantum dot at room temperature', *Nano Lett.*, 2014, **14**, pp. 71–77
- [15] Lee S., Lee Y., Song E.B., *ET AL.*: 'Gate-tunable selective operation of single electron/hole transistor modes in a silicon single quantum dot at room temperature', *Appl. Phys. Lett.*, 2013, **102**, p. 083504
- [16] Lee S., Lee Y., Song E.B., *ET AL.*: 'The characteristic of elongated Coulomb-blockade regions in a Si quantum-dot device coupled via asymmetric tunnel barriers', *J. Appl. Phys.*, 2013, **114**, p. 164513
- [17] Lee Y., Lee S., Hiramoto T.: 'Transport behaviors and mechanisms in cuspidal blockade region for silicon single-hole transistor', *Curr. Appl. Phys.*, 2014, **14**, pp. 428–432
- [18] Hu C., Cotofana S.D., Jiang J.F.: 'Single-electron tunneling transistor implementation of periodic symmetric functions', *IEEE Trans. Circuits Syst. II*, 2004, **51**, (11), pp. 593–597
- [19] Cotofana S.D., Vassiliadis S.: 'Periodic symmetric functions, serial addition and multiplication with neural networks', *IEEE Trans. Neural Netw.*, 1998, **9**, pp. 1118–1128
- [20] Hu C., Cotofana S.D., Jiang J.F., *ET AL.*: 'Analog-to-digital converter based on single-electron tunneling transistors', *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 2004, **12**, (11), pp. 1209–1213
- [21] Miyaji K., Saitoh M., Hiramoto T.: 'Compact analytical model for room-temperature operating silicon single-electron transistors with discrete quantum levels', *IEEE Trans. Nanotechnol.*, 2006, **5**, (3), pp. 167–173
- [22] Dan S.S., Mahapatra S.: 'Impact of energy quantization on the performance of current-biased SET circuits', *IEEE Trans. Electron Devices*, 2009, **56**, (8), pp. 1562–1566
- [23] Zwolak M., Di Ventra M.: 'DNA spintronics', *Appl. Phys. Lett.*, 2002, **8**, (5), pp. 925–927
- [24] Emberly E.G., Kirczenow G.: 'Molecular spintronics: spin-dependent electron transport in molecular wires', *Chem. Phys.*, 2002, **281**, pp. 311–324
- [25] Wasshuber C., Kosina H., Selberherr S.: 'SIMON a simulator for single electron tunnel devices and circuits', *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, 1997, **16**, (9), pp. 937–944
- [26] Datta S.: 'Quantum transport: atom to transistor' (Cambridge University Press, 2005)