Effect of input noise on phase coherence in a lattice of memristors acting as a voltage divider

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Abstract: It is known that Fibonacci numbers emerge from a network of voltage dividers comprising just resistors. The authors find that the same happens to a lattice of memristors as recently devised. Between the memristor dividers there is a phase coherence with respect to a sinusoidal input signal. Interestingly, they show that the effect of Gaussian distributed random noise, which adds to the voltage signal at the input of the memristor lattice, may affect the coherence. It is shown that when the signal-to-noise ratio goes below 3 dB and the number of dividers in the lattice is ten there is an abrupt reduction of phase coherence typical of non-linear systems. This behaviour does not happen with a lattice of normal resistors. A tolerance analysis of the classical resistor components as well as of the memristor parameters is also presented.

1 Introduction

The discovery of memristor is due to Chua [1] who proposed it as a fourth element of circuits having the property that its resistance depends on the charges it carries [Incidentally, Leon Chua showed that a memristor was already known in the 19th century: this is the carbon arc discharge realised by Humphry Davy in 1801 [2].]. This leads to a non-linear circuital equation with a voltage–current (V–I) characteristics described by a Lissajous curve when the input signal is sinusoidal in time. A technological realisation of a memristor has been successfully accomplished by an HP group [3]. It is also possible to obtain a memristor by combining diodes and RLC passive components, as recently shown in [4, 5]. The main difference between these two realisations of a memristor is in their dimensions. The HP memristor is in the nanometric scale, and so significantly smaller than the same component realised with discrete components even with CMOS technology. Memristors were recently fully characterised in [6] and classified [7]. An implementation through superconductors was also provided [8].

Our paper develops along the following path. We start by reviewing the lattice of resistor dividers described in a paper by Morgan-Voyce [9]. This author shows that such a lattice, with identical values of resistance, displays a fixed value of resistance at the input that is the golden ratio. This is so because such an input resistance is determined by the ratio of Fibonacci numbers that, in the limit running to infinity, is exactly the golden ratio. The output resistance shows identically that a fixed value holds as the number of dividers goes to infinity. This is exactly the inverse of the golden ratio. From a practical point view, this is an interesting observation that could provide a way to produce communication channels with a fixed value of resistance independently of the length. In an actual realisation the resistances are not exactly equal and the result holds approximately. With this result in hand, known from the literature, we have attempted to extend it to a lattice of memristors. To this end, we implement the nonlinear differential equation of the non-linear HP device with the Kirchhoff law in closed form for two dividers and numerically for a large number up to, say, 1000 dividers. The input signal is a sinusoid. We find that coherence on the input signal is kept along, the entire lattice which seems an interesting result. Furthermore, to emulate more realistic conditions we added some noise at the input signal. The noise has been taken to be independent Gaussian distributed with zero mean and suitable standard deviation. We note that for high signal-to-noise ratio (SNR) the phase coherence across the dividers is essentially maintained also up to 1000 dividers. When the SNR decreases below a critical value, the coherence is lost. We study in detail the behaviour of a lattice of ten dividers and show that, when a threshold of about 3 dB for decreasing SNR is overcome, the behaviour changes abruptly and phase coherence is rapidly lost. The reason to limit the analysis to just ten dividers is bounded to the computational burden and also to keep under control the accuracy of the ODE (ordinary differential equation) solver that we used. Nonetheless, we observed a critical behaviour in the SNR. This is due to the fact that the convergence of the lattice ODE is rapid enough in time. The analysis we performed makes substantial use of the HP model [3]. The reason relies on the fact that this yields a satisfactory description of a memristor and circuital analysis has already been performed in this case [10].

The reason to consider such a circuital configuration arises from the hypothesis that synapses are well described by memristors [11, 12]. In this paper, we try to understand the fate of a large number of such interconnected synapses. As we will show, the result is highly non-trivial.

The choice of a proper model for the memristor is a key one. A set of possible choices are given in [13]. Our aim here is to depict the memristor in its essence showing how, given a proper V–I behaviour, an interesting effect appears when noise is present. In this view, it is not so important to give an exact description of a physical device rather, a model like that yielded in [3] is enough for our aims, leaving a study for more involved model to future work.

The paper is organised as follows. Section 2 recalls the lattice of resistors. Section 3 describes the non-linear differential equation that models the behaviour of the HP memristor. The deleterious effect of noise added to the input signal is described in Section 4. A relevant result has been achieved showing the coherence loss depicted through the behaviour of the Frechet distance between the first and the last dividers. A check with respect to the tolerance of the parameters of the memristors is also presented. Finally, conclusions and future research avenues are given in Section 5.

2 Lattice of resistors and relations to Fibonacci sequence

A voltage divider is represented in Fig. 1.

The main equations are

$$V_{\text{in}} = (R_1 + R_2)I \tag{1}$$

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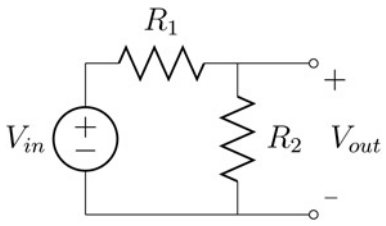


Fig. 1 *Voltage divider*

where V_{in} is the input voltage, R_1 and R_2 are the resistors in the divider and I is the current, so

$$V_{\text{out}} = \frac{R_2}{R_1 + R_2} V_{\text{in}} \tag{2}$$

is the voltage output from the divider. This means that

$$A = \frac{V_{\text{in}}}{V_{\text{out}}} = 1 + \frac{R_1}{R_2} \tag{3}$$

is the attenuation of the divider. We can introduce a constant K as

$$K = \frac{R_1}{R_2} \tag{4}$$

that characterises the transfer function of the divider as $H = (1 + K)^{-1}$. This has an input impedance $Z_{\text{in}} = (1 + K)R_2$ and an output impedance $Z_{\text{out}} = R_1/(1 + K)$. We can extend a divider to form a lattice with cascade of dividers as shown in Fig. 2.

The input impedance is given now by

$$Z_{\text{in}} = R_1 + \cfrac{1}{(1/R_2) + \cfrac{1}{R_3 + \cfrac{1}{R_4 + \cdots}}} \tag{5}$$

and when we assume all resistors to have the same value R we obtain the sequence for dividers (pairs of resistances)

$$\begin{aligned} n &= 1 \quad Z_{\text{in}} = 2R \\ n &= 2 \quad Z_{\text{in}} = \frac{5}{3}R \\ n &= 3 \quad Z_{\text{in}} = \frac{13}{8}R \\ &\vdots \end{aligned} \tag{6}$$

Equation (5) tells us that in this case

$$1 + K = \frac{1}{R_n}\left(R_1 + \cfrac{1}{(1/R_2) + \cfrac{1}{R_3 + \cfrac{1}{R_4 + \cdots}}}\right). \tag{7}$$

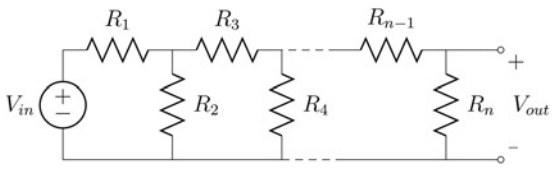


Fig. 2 *Net of voltage dividers*

It is easy to recognise from (6) that these are just the ratios between Fibonacci numbers F_n/F_{n-1} [9]. If the lattice is taken to go to infinity we reach the golden ratio $\phi = (\sqrt{5} + 1)/2 \simeq 1.61803398875$ (see figures below). In [9], it is also shown that the corresponding output resistance is the inverse of the golden ratio. This is a quite interesting result. In fact, ideally, however long the lattice of resistances, the equivalent resistance seen from the output has a constant value which is $\phi^{-1} = \phi - 1$. These results are presented in Fig. 3.

Our aim is to understand how the above results generalise to a lattice of memristors.

3 Model of memristor

The memristor model recently proposed is the following [We are aware that more accurate but more mathematically involved equations for the memristor exist. For the sake of simplicity, we have the more tractable model proposed by HP [3]. A complete description of models can be found in [13].]. We assume a semiconductor film with one side more doped than the other and sandwiched between metallic contacts. The higher doped side has a very low resistance $\mathcal{R}_{\text{ON}}$ and the other side has a much higher resistance $\mathcal{R}_{\text{OFF}}$. Then, the voltage–current relation has the form [3]

$$V(t) = \left[\mathcal{R}_{\text{ON}} \frac{w(t)}{D} + \mathcal{R}_{\text{OFF}}\left(1 - \frac{w(t)}{D}\right)\right] I(t) \tag{8}$$

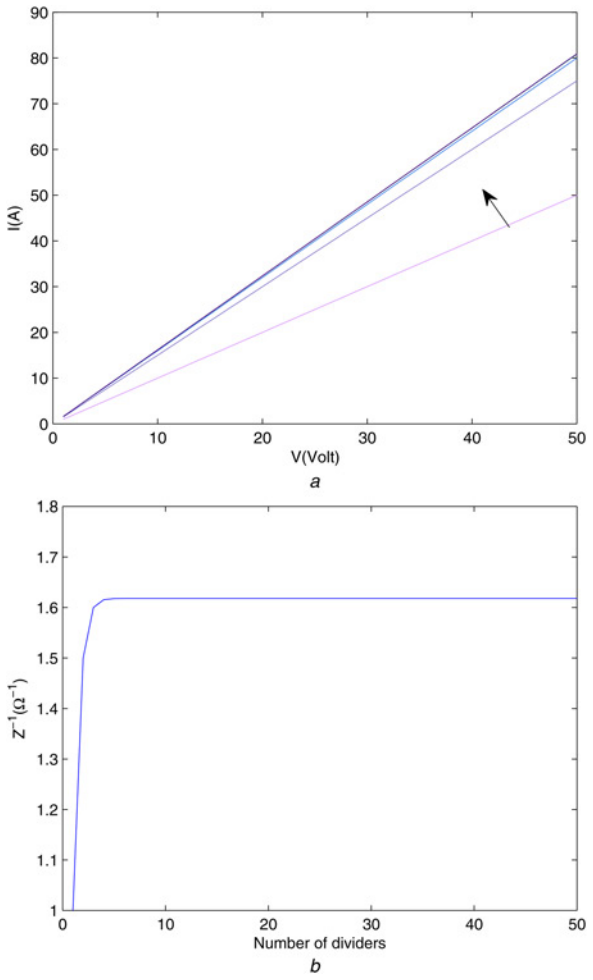


Fig. 3 *Dividers with resistors. This is just an application of Ohm's law iterated on the number of dividers*
a Converging of the Ohm's law to the golden ratio
b Golden ratio in the limit of a large number of dividers

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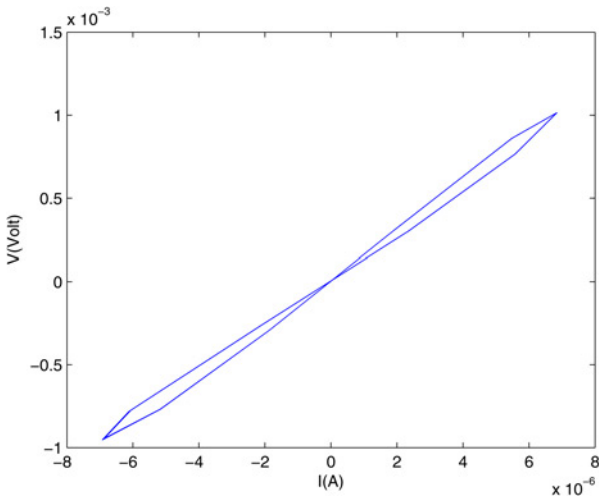


Fig. 4 *Lissajous figure in the plane V–I typical of a memristor obtained by solving (11). Applied voltage is a sinusoid with 1 V of amplitude and 100 Hz of frequency*

where D is the thickness of the film, and $w(t)$ is a function of the current yielded by

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_V \frac{\mathcal{R}_{\mathrm{ON}}}{D} I(t) \tag{9}$$

where μ_V is the average ion mobility. Now V and I are functions of time. The latter equation can be immediately solved to give

$$w(t) = \mu_V \frac{\mathcal{R}_{\mathrm{ON}}}{D} q(t) \tag{10}$$

in which $q(t)$ is the charge. This yields a non-linear differential equation

$$V(t) = \left[\mu_V \mathcal{R}_{\mathrm{ON}}^2 \frac{q(t)}{D^2} + \mathcal{R}_{\mathrm{OFF}}\left(1 - \mu_V \frac{\mathcal{R}_{\mathrm{ON}}}{D^2} q(t)\right)\right] \frac{\mathrm{d}q(t)}{\mathrm{d}t}. \tag{11}$$

This equation can be solved exactly but instead we provide an example of a physical solution in Fig. 4 displaying a Lissajous figure as expected for the memristor when a sinusoid with 1 V of amplitude and 100 Hz frequency is applied at the input.

The next step is to extend this analysis to the voltage divider using memristors as shown in Fig. 5.

To solve for the memristor divider (Fig. 5) we apply Kirchhoff's theorem (conservation of charge $q(t)$) and write

$$V(t) = [M_1(q(t)) + M_2(q(t))] \cdot I \tag{12}$$

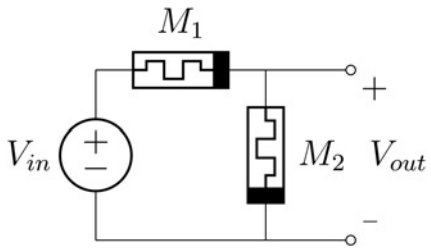


Fig. 5 *Voltage divider using memristors*

where M_1 and M_2 are the memristors in the circuit. Then, we rewrite the given memristor equation as

$$V(t) = \left[M_0 + (M_1 - M_2)q(t)\right] \frac{\mathrm{d}q(t)}{\mathrm{d}t} \tag{13}$$

where $M_0 = \mathcal{R}_{\mathrm{OFF}}$, $M_1 = (\mu_V \mathcal{R}_{\mathrm{ON}}^2 / D^2)$ and $M_2 = \mu_V(\mathcal{R}_{\mathrm{ON}}\mathcal{R}_{\mathrm{OFF}}/D^2)$. The constants will be different for the two memristors. So, one has for the divider

$$V(t) = \left[M_0^{(1)} + M_0^{(2)} + (M_1^{(1)} + M_1^{(2)} - M_2^{(1)} - M_2^{(2)})q(t)\right] \frac{\mathrm{d}q(t)}{\mathrm{d}t}. \tag{14}$$

This can be immediately rewritten as

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[(M_0^{(1)} + M_0^{(2)})q(t) + \frac{1}{2}(M_1^{(1)} + M_1^{(2)} - M_2^{(1)} - M_2^{(2)})q^2(t)\right] = V(t). \tag{15}$$

Introducing the magnetic flux of the voltage $V(t)$ as $\phi(t) = \int_0^t \mathrm{d}t' V(t')$ according to the Faraday–Neumann–Lenz induction law, we can write the solution as

$$q(t) = \frac{M_0^{(1)} + M_0^{(2)}}{-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)}} \times \left(1 - \sqrt{1 - \frac{2(-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)})}{(M_0^{(1)} + M_0^{(2)})^2}\phi(t)}\right) \tag{16}$$

for $q(0) = 0$. Finally, the current is given by (see (17))

The output voltage will be given by (see (18))

We note that when the contribution from the flux $\phi(t)$ is negligible, that is for $\mathcal{R}_{\mathrm{OFF}} \gg \mathcal{R}_{\mathrm{ON}}$, at high enough frequencies, the

$$I(t) = \frac{V(t)}{M_0^{(1)} + M_0^{(2)}} \frac{1}{\sqrt{1 - \left(\left(2(-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)})\right)/\left((M_0^{(1)} + M_0^{(2)})^2\right)\right)\phi(t)}}. \tag{17}$$

$$\begin{aligned} V_{\mathrm{out}} &= \left[M_0^{(2)} + (M_1^{(2)} - M_2^{(2)})q(t)\right] I(t) \\ &= \left[M_0^{(2)} + (M_1^{(2)} - M_2^{(2)}) \frac{M_0^{(1)} + M_0^{(2)}}{-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)}} \left(1 - \sqrt{1 - \frac{2(-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)})}{(M_0^{(1)} + M_0^{(2)})^2}\phi(t)}\right)\right] \\ &\quad \times \frac{1}{\sqrt{1 - \left(\left(2(-M_1^{(1)} - M_1^{(2)} + M_2^{(1)} + M_2^{(2)})\right)/\left((M_0^{(1)} + M_0^{(2)})^2\right)\right)\phi(t)}} \frac{V(t)}{M_0^{(1)} + M_0^{(2)}}. \end{aligned} \tag{18}$$

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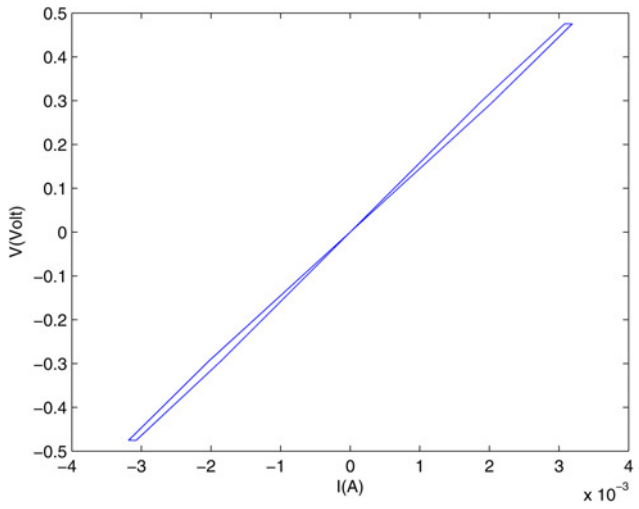


Fig. 6 *Lissajous figure in the plane V–I typical of a memristor voltage divider for equal values of memristors. Applied voltage is a sinusoid with 1 V of amplitude and 100 Hz frequency*

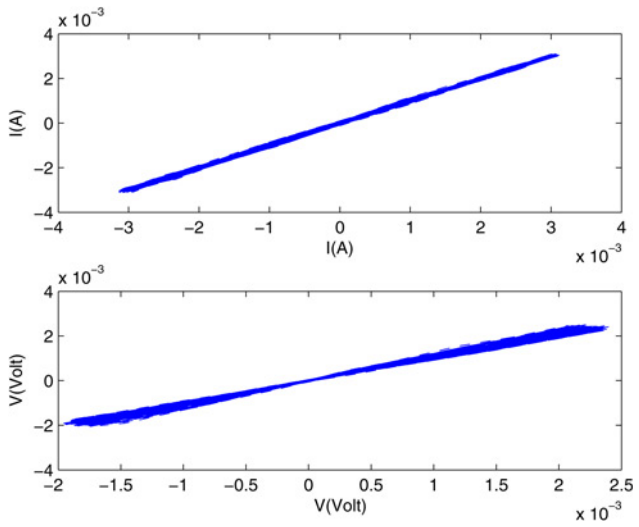


Fig. 7 *I–I and V–V planes for the phase relation between the case of 200 dividers (abscissa) and 700 dividers (ordinate) with noise added having $\sigma = 0.1$ V*

memristors behave like ordinary resistors and we recover the result for a standard voltage divider as discussed in the preceding section. Now, assuming identical memristors in the circuit, the above equation becomes

$$V_{\text{out}} = \frac{V(t)}{2} \tag{19}$$

and acts exactly as the voltage divider of the preceding section but with a substantial difference: the voltage $V(t)$ is properly modified as already seen for a memristor in the plane V–I producing a Lissajous figure. Indeed, in the approximation where $\mathcal{R}_{\text{OFF}} \gg \mathcal{R}_{\text{ON}}$ and we are permitted to neglect terms like $\mathcal{R}^2_{\text{ON}}$, it is easy to obtain in Fig. 6, where we see that the initial voltage is divided by a factor 2 at its maximum and minimum.

4 Effect of noise

In the presence of independent Gaussian distributed noise samples, we show that there is a threshold on the signal-to-noise-power ratio that, when goes below a critical value, it causes loss of phase between the dividers. We show here a pair of cases with $\sigma = 0.1$ V and $\sigma = 1$ V for the noise amplitude and 1 V for the signal amplitude [The code of this analysis and following is available on request from the corresponding author.]. For the 0.1 V case, this can be seen in Fig. 7.

In the presence of phase coherence, we expect to see a straight line as the difference between the behaviours for 200 dividers and 700 dividers could be just a proportionality factor. However, if the phase changes, signalling a loss of coherence, we will observe rotation of this straight lines due to a residual frequency that moves them. In our pictures, we see that the variation with respect to straight lines is small enough to provide coherence along the dividers also with this level of noise. Anyhow, it is possible that with longer integration times the coherence loss could appear. The level of noise determines the duration of coherence along the dividers. The hysteresis curves have the form given in Fig. 8*a*. With a low level of noise the points belong to a hysteresis curve with a regular behaviour. This does not happen when noise is high making the curves somewhat irregular. Our figure shows how all the hysteresis curves tend to gather around the line having as a slope the inverse of the golden ratio. Finally, the SNR behaves as given in Fig. 8*b*.

Here we see that the SNR is almost constant around a given value as should be expected in an almost deterministic behaviour. Indeed, moving to $\sigma = 1$ V we get from Fig. 9.

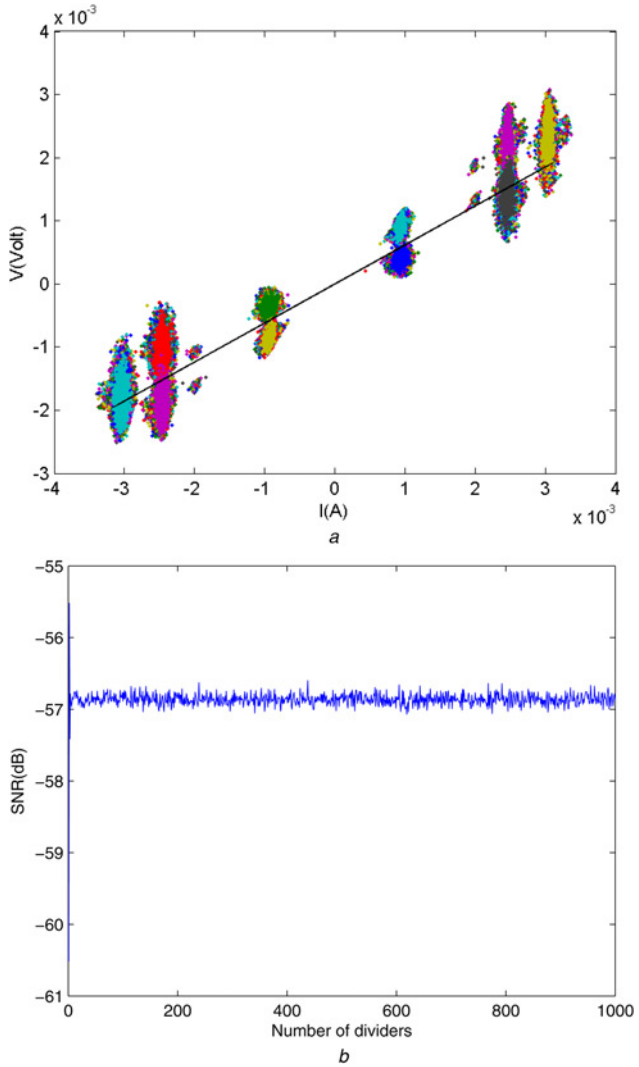


Fig. 8 *1000 voltage dividers with noise added having $\sigma = 0.1$ V*
a Hysteresis curves for 1000 dividers. The black line represents the curve $V = (1\ \Omega) \cdot I/\phi$ being $\phi = (\sqrt{5}+1)/2$ the golden ratio
b SNR for 1000 dividers

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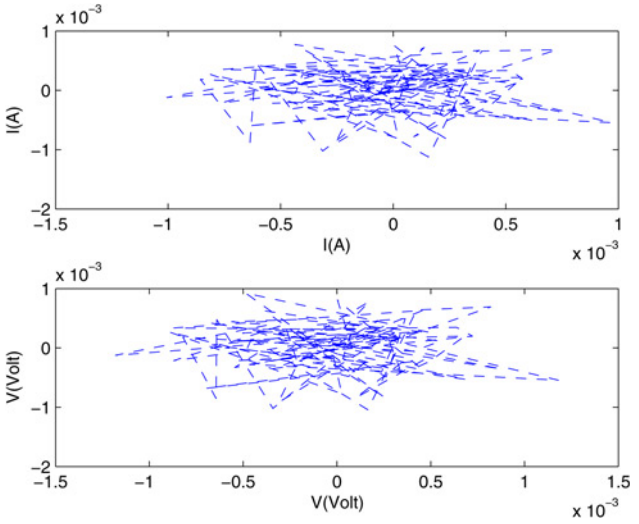


Fig. 9 *I–I and V–V planes for the phase relation between the case of 200 dividers (abscissa) and 700 dividers (ordinate) with noise added having* $\sigma = 1$ *V*

Now the coherence is completely lost and the straight lines are seen to rotate. In this case, the hysteresis curves have the form given in Fig. 10.

We see that now that the points are covering all the surfaces of the hysteresis curves indicating an ergodic-like behaviour, which means that, on a long enough time, almost all available space in the *V–I* domain is covered by the curves. Again, we see that all the hysteresis curves tend to gather around the line having as a slope the inverse of the golden ratio. Finally, the histogram of the SNR behaves as given in Fig. 11. showing a good fit with a Gaussian probability distribution. Then the behaviour is essentially noisy.

From the above analysis, it is clear that there has to exist a threshold of noise that, when overcome, makes the coherence loss through the divider chain appear very early. On the other hand, this kind of device is seen to be rather robust with respect to noise. This gave us a motivation to define a proper observable to determine when the effect of noise destroys the coherence property of the memristor lattice. To this aim, we introduced the L^2 distance, a form of Frechet distance, as a function of the level of noise taking the

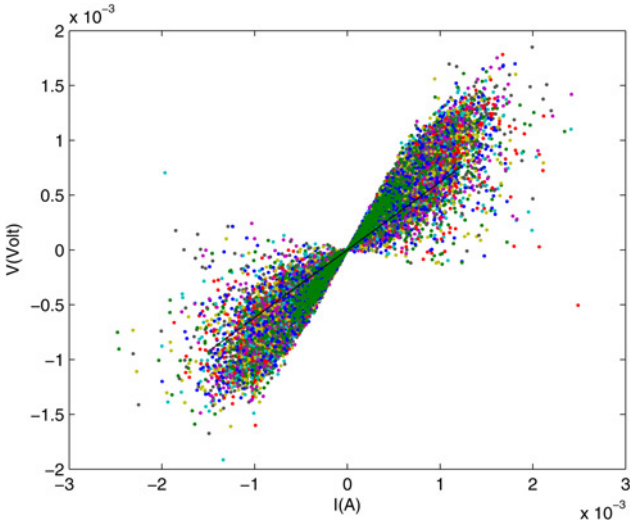


Fig. 10 *Hysteresis curves for 1000 dividers with noise added having* $\sigma = 1$ *V. The black line represents the curve* $V = (1\ \Omega) \cdot I/\phi$ *where* $\phi = (\sqrt{5} + 1)/2$ *is the golden ratio*

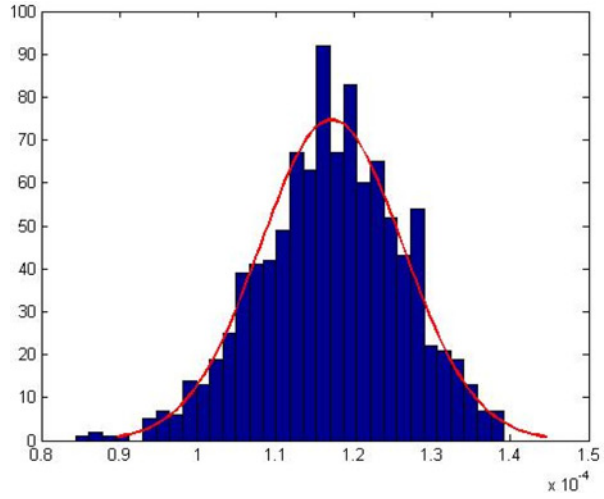


Fig. 11 *Histogram of the SNR for 1000 dividers with noise added having* $\sigma = 1$ *V*

number of dividers fixed. We take a lattice with 10 dividers and make 100 independent Monte Carlo runs for each configuration of noise. The Frechet (L^2) distance is given by

$$d(V_1, V_{10}) = \sum_{i=1}^{n} |V_1(t_i) - V_{10}(t_i)| \tag{20}$$

assuming that the output voltages at the first divider V_1 and at tenth divider V_{10} are sampled on $n = 500$ points t_i, $i = 1, \ldots, n$. We can fix our 0 by measuring this distance in the absence of noise. Assuming a sinusoidal input signal of 5 V at 100 Hz, we get for the distance with no noise 0.0064 V. The effect of noise is, as expected, to increase the distance and this growth is rectilinear until $\sigma = 3.5$ V. Beyond this value, the effect of noise makes the behaviour essentially erratic. This is shown in Fig. 12*b* where we arrive to a noise level of 5 V and SNR = 0 dB. From the figure, it is evident that, above $\sigma = 3.5$ V for the noise level (below 3 dB for the SNR), the behaviour of the lattice changes abruptly similarly to a statistical mechanics phase transition. The linear fit leaves the place to a somewhat erratic behaviour and the phase coherence can be lost very early depending on the configuration of the noise. For a consistency check, we yield also the plot for normal resistors of Fig. 12*a*, fed by zero mean independent Gaussian distributed noise with increasing value of variance, where it is seen that the linear behaviour is overall maintained.

Concerning tolerance analysis, approximately this same figure is obtained with a Gaussian distributed tolerance on all $\mathcal{R}_{ON}$ and $\mathcal{R}_{OFF}$ of 1%. Similarly, the tolerance analysis on the classic lattice of resistors brings to the conclusion that small changes in the values of the resistors do not affect the expected behaviour. This is due to the fact that we have Ohm's law and so, there is just an algebraic relation rather than an ODE to solve. We leave for the future a more accurate analysis of tolerances entering into the characterisation of a memristor.

5 Conclusions

We have reviewed the lattice of resistors and exploited the computations in [9] to show them in suitable graphs. The ladder of resistors is used in industrial applications in ADC technology [E.g. see the article https://en.wikipedia.org/wiki/Resistor_ladder in Wikipedia]. Similarly, the output impedance is the inverse of the golden ratio. This is interesting because, however long the ladder is, the output impedance is ideally always the same assuming all equal resistors. This classical result has triggered us the idea to extend the lattice also to the

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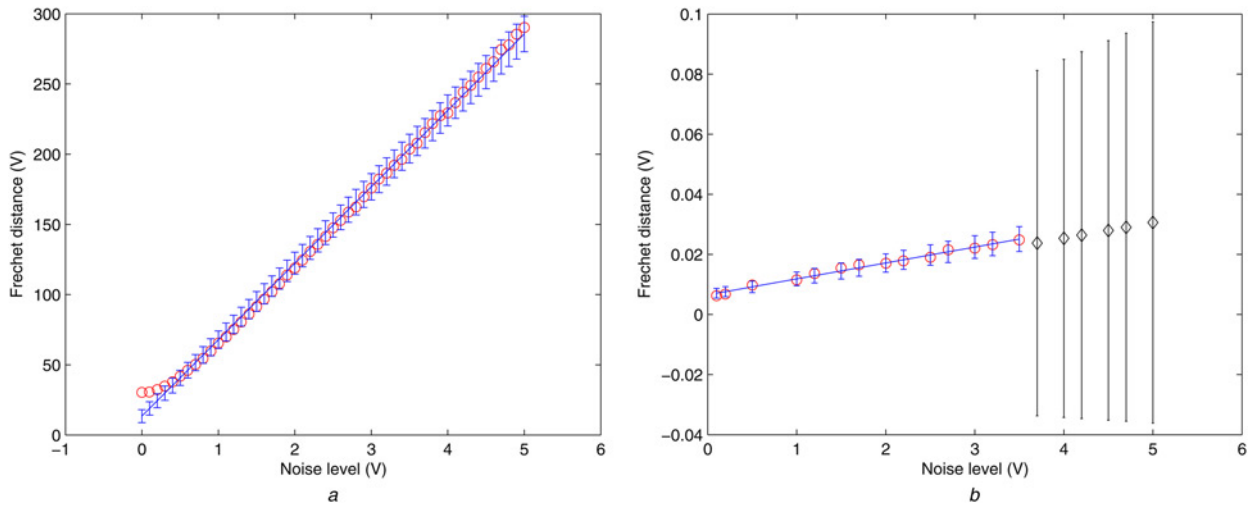


Fig. 12 *Monte Carlo studies for memristors and resistors with noise*
a Linear fit to Monte Carlo results for a lattice of resistors. Red circles are the measured values and the straight line is the fitted curve with relative errors given by bars
b Linear fit to Monte Carlo results. Beyond $\sigma = 3.5$ V the behaviour changes abruptly

recently realised memristor. We have found that also the input impedance of the memristor lattice converges towards the golden ratio seen as the slope of the hysteresis curve when the input signal is a sinusoid. Furthermore, we have shown that there is a perfect coherence between the hysteresis curves across the lattice of memristors. Of course, this is an ideal situation. Thus we have added a white Gaussian distributed noise to the input signal in order to check when the phase coherence gets lost as the noise level increases with respect to the signal level. We find that when the SNR goes below 3 dB the behaviour changes abruptly and the lattice, taken here with ten dividers, cannot hold phase coherence. We have verified this in a range of noise power running from 3.5 to 5 V.

From the perspective of a network (in this study, a ladder) of synapses, these appear rather robust and the intensity of the noise needed to disrupt a coherent behaviour is rather high. Anyway, this can happen and a synapse network can lose its phase coherence.

Future work will refer to hardware realisation of the lattice of memristors with five cells resorting to hardware approach proposed in [4]. We hope to be able to find by measurements the analytical results we have shown in the absence and in the presence of noise as described in this paper.

6 References

[1] Chua L.O.: 'Memristor – the missing circuit element', *IEEE Trans. Circuit Theory*, 1971, **CT-18**, pp. 507–519

[2] Lin D., Chua L., Hui S.-Y.: 'The first man-made memristor: circa 1801 [scanning our past]', *Proc. IEEE*, 2015, **103**, (1), pp. 131–136

[3] Strukov D.B., Snider G.S., Stewart D.R., *ET AL.*: 'The missing memristor found', *Nature*, 2008, **453**, pp. 80–83. Corrigendum: Nature 459, 1154 (2009)

[4] Corinto F., Ascoli A.: 'Memristive diode bridge with LCR filter', *Electron. Lett.*, 2012, **48**, (14), pp. 824–825

[5] Corinto F., Ascoli A., Gilli M.: 'A novel elementary memristor device'. IEEE/IFIP 20th Int. Conf. on VLSI and System-on-Chip, 2012 (VLSI-SoC), 2012, pp. 76–81

[6] Corinto F., Civalleri P.P., Chua L.O.: 'A theoretical approach to memristor devices', *IEEE J. Emerg. Sel. Top. Circuits Syst.*, 2015, **5**, (2), pp. 123–132

[7] Corinto F., Civalleri P.P., Chua L.O.: 'Classification of memdevices'. IEEE 15th Int. Conf. on Nanotechnology (IEEE-NANO), 2015, 2015, pp. 629–632

[8] Peotta S., Di Ventra M.: 'Superconducting memristors', *Phys. Rev. Appl.*, 2014, **2**, p. 034011

[9] Morgan–Voyce A.M.: 'Ladder-network analysis using Fibonacci numbers', *IRE Trans. Circuit Theory*, 1959, **6**, (3), pp. 321–322

[10] Kavehei O., Iqbal A., Kim Y.S., *ET AL.*: 'The fourth element: characteristics, modelling and electromagnetic theory of the memristor', *Proc. R. Soc. A*, 2010, **466**, pp. 2175–2202

[11] Chua L., Sbitnev V., Kim H.: 'Hodgkin-Huxley axon is made of memristors', *Int. J. Bifurcation Chaos*, 2012, **22**, (3), p. 1230011

[12] Chua L.O., Adamatzky A.: 'Memristor networks' (Springer, Berlin, 2014), pp. 76ff

[13] Radwan A.G., Fouda M.E.: 'On the mathematical modeling of memristor, memcapacitor, and meminductor' (Springer, Berlin, 2015)

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