Noise Minimization in CMOS Current Mode Circuits That Employ Differential Input Stage

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***Abstract*—In this paper, a new noise minimization approach is proposed for CMOS current-mode (CM) circuits whose input stage is differential. This is realized by focusing on input stage and some output stage transistors' transconductance. Effect of output stage over the noise model depends on output stage's operation. This minimization is introduced to designers as a trade-off between design parameters and noise reduction. Analyses are presented in basis of Differential Difference Current Conveyor (DDCC) for simplicity. To reinforce theoretical concept, simulation results are given both in schematic and layout based. Moreover, a DDCC filter application, which has single input and four outputs is presented to verify theoretical minimization approach. After minimization, it is shown that significant noise reduction is obtained up to 50%. In addition, Monte Carlo analysis is given in order to investigate process variations and temperature effects on measured input referred noise.**

***Index Terms*—noise minimization, current mode circuits, DDCC, DVCC, input referred noise, active elements.**

I. Introduction

This explosive growth of high speed and low voltage operation increase the interest in CM signal processing due to potential of this technique [1]. A CM approach is useful if we focus on all of IC technology which conventionally is designed in voltage-mode (VM). The research papers published regarding this topic tackle mostly with the speed performance of CM circuits and CM or VM filters based on differential input stage which are used in very different analog circuit applications [1]-[5]. However, little work has been published regarding noise performance of current mode basic blocks such as current conveyors [1], [6]-[10].

In this paper, we present a noise minimization model for differential input stage based CMOS CM circuits and show how the model can be used to evaluate the noise performance of CM signal processing functions. Furthermore, we analyze the noise characterization of CMOS implementation of a DDCC[11]/DVCC[12] (Differential Voltage Current Conveyor) and we evaluate design issues to develop the noise performance and design trade-off between noise effect and low voltage signal processing key issues.

In this respect, we have a novel scope, because the published papers related to DDCC/DVCC are interested only in input and output referred noise simulation [2]-[5].

The noise minimization which is presented based on the DDCC [12] can be generalized for all CM circuits including differential input stage. Proposed noise minimization model also will be beneficial for a great deal of application circuits based on DDCC/DVCC such as VM filters [13], [14], CM filters [15], [16], mixed mode filters [17], oscillators [18], [19] rectifier circuits [20] and inductance simulators [21], [22].

In this regard, theoretical approach based on thermal noise for a wide frequency range is presented in sections II and III. To empower aforementioned noise minimization approach, post layout simulations of DDCC given in Fig.2 are presented in section IV and V. In addition to current conveyor characteristics, a filter application which has multiple outputs and single input is given with post layout results in the last section. To exemplify promising outcomes of the proposed minimization technique, the input referred noise values of a band pass filter circuit is given with post layout and Monte Carlo analysis in this section.

II. The Differential Current Conveyor Basics

A novel CM scheme called DDCC is proposed in [12]. The DDCC has some main advantages such as high input impedance and arithmetic operation property. In this view, DDCC contains powerful sides of both the CCII and the differential difference amplifier (DDA). Its input-output behavior can be described as:

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix} \quad (1)$$

DDCC which is shown in Fig.1 has four high impedance terminals and a low impedance input terminal called Y1, Y2, Y3, Z, and X, respectively. We interest in single output case but results in this paper can be applied to multiple output configurations. Resistances of X and Z terminals in a real DDCC can be described in terms of transistor parameters in the Fig.2 as:

$$R_X = \frac{g_{ds4} + g_{ds8}}{g_{m4} g_{m9}} \quad (2)$$

$$R_Z = \frac{1}{g_{ds10} + g_{ds12}} \quad (3)$$

where, g_{ds} and g_m denote the drain-to-source conductance and the transconductance, respectively. It is very important to mention that a first or third generation current conveyor can be formed from a DDCC by feeding back an appropriate Z-output to the Y-input terminal in order to construct required characteristics such as $I_Y=I_X$ and $I_Y=-I_X$ [1], [23].

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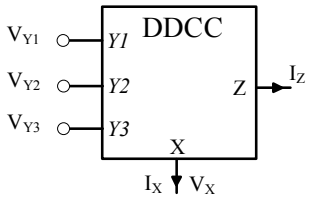

Figure 1. Circuit symbol of DDCC

Taking some non-idealities into account, the relationship of the terminal voltages and currents can be described as $V_X=\beta_1 V_{Y1}-\beta_2 V_{Y2}+\beta_3 V_{Y3}$ and $I_Z=\alpha I_X$. where, βi (i=1,2,3) is the voltage transfer gain from V_{Yi} terminal to the V_X terminal of the DDCC and α is the current transfer gain from I_X terminal to I_Z terminal of the DDCC. Owing to those facts, these non-idealities will be affected by noise reduction that is focused on the next parts.

III. Application Example

To [7], [8] presents some design issues for the noise evaluation in differential pair based CCIIs. It evaluates the input referred noise model using fundamental quantities and g_m values of the transistors. A powerful noise model of the differential current conveyor contains noise generators referred to *X* and *Y* terminals. The noise model is constructed by the input referred noise voltage at high impedance terminal *Y* and input referred noise current at low impedance terminal *X*. Using the noise model enables both a fair noise comparison and minimization based on basic transistor parameters.

In this manner, Fig. 2 can be constructed based on [12]. The total noise voltage at *Y* ports is the combination of thermal noises of NMOS differential pairs and PMOS loads. So, transistors M_3, M_4, M_7 and M_8 give rise to the thermal noise voltage at *Y1* terminal and it can be calculated as:

$$\overline{V_{Y1}^2}=\frac{1}{g_{m4}^2}\left[\overline{I_{DS4}^2}+\overline{I_{DS8}^2}+\left(\frac{g_{m8}}{g_{m7}}\right)^2\overline{I_{DS7}^2}+\left(\frac{g_{m8}}{g_{m7}}\right)^2\overline{I_{DS3}^2}\right] \quad (1)$$

M_1-M_2 and M_3-M_4 are differential pairs. Dimensions of the transistors are taken as in Table III. So, we have $\overline{I_{DS1}^2}=\overline{I_{DS2}^2}=\overline{I_{DS3}^2}=\overline{I_{DS4}^2}$ and $\overline{I_{DS7}^2}=\overline{I_{DS8}^2}$. Using the thermal noise equation:

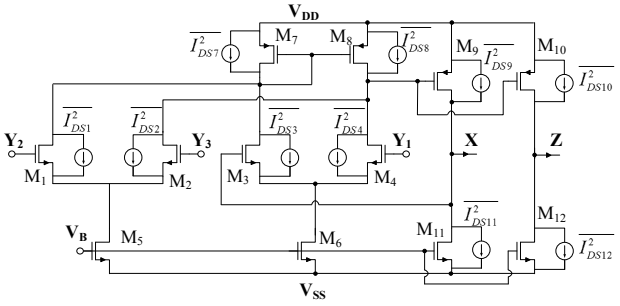

Figure 2. CMOS DDCC proposed in [12] with noise sources

$$\overline{I_{DSj}^2}=4kTg_{mj} \qquad \text{j=1,2,…n} \quad (2)$$

(1) can be re-written as:

$$\overline{V_{Y1}^2}=4kT\left(\frac{1}{g_{m4}}\left(2+\frac{2g_{m8}}{g_{m4}}\right)\right) \quad (3)$$

This analysis can be repeated for *Y2* and *Y3* terminals in the same way. For simplicity, only voltage noise at *Y1* is considered. As for the low impedance terminal *X*, calculation of the equivalent thermal noise at this port is realized by the help of some nodal equations. It is easy to see that transistors M_9 - M_{12} reinforce to the thermal noise current at *X* terminal while the noise effect arising from M_5 and M_6 is eliminated because they are common mode noise in the differential pairs and can be suppressed [24]. In this respect, total thermal noise at *X* can be calculated as:

$$\overline{I_X^2}=\overline{I_{DS9}^2}+\left(\frac{g_{m9}}{g_{m10}}\right)^2\overline{I_{DS10}^2}+\overline{I_{DS11}^2}+\left(\frac{g_{m11}}{g_{m12}}\right)^2\overline{I_{DS12}^2} \quad (4)$$

If (2) is replaced in (8), it yields to the following equation:

$$\overline{I_X^2}=4kT\left[\left(g_{m9}\left(1+\frac{g_{m9}}{g_{m10}}\right)\right)+\left(g_{m11}\left(1+\frac{g_{m11}}{g_{m12}}\right)\right)\right] \quad (5)$$

The basic sense is to reduce those noise effects. However, the minimization in noise values will enhance some non-idealities of DDCC. This trade-off will be evaluated as noise minimization over transistor parameters. It is deeply underscored in simulation results part.

In ideal case, we have zero R_X and infinite R_Z. Intuitively, these ideal values cannot be obtained due to non-ideal bias generator and transistor characteristics. Furthermore, to reduce input referred noise values at *Y* and *X* port will deteriorate those values. The next part deals with this problem. Meanwhile, these noise characterizations can be applied for DVCC in the same way because there is no difference between DDCC and DVCC except a grounded Y_3 terminal. In this regard, the noise minimization keys presented in this paper also can be considered in DVCC.

IV. Simulation Results

To verify theoretical approach presented in the previous section and to establish a noise minimization structure for DDCC, simulation analyses are given in this part. For SPICE simulations, dimensions of transistors in [25] are considered and analyses are realized in 0.18µm TSMC CMOS technology. Also, supply and biasing voltages are V_{DD}=-V_{SS}=1.25V and V_B=-0.45V, respectively.

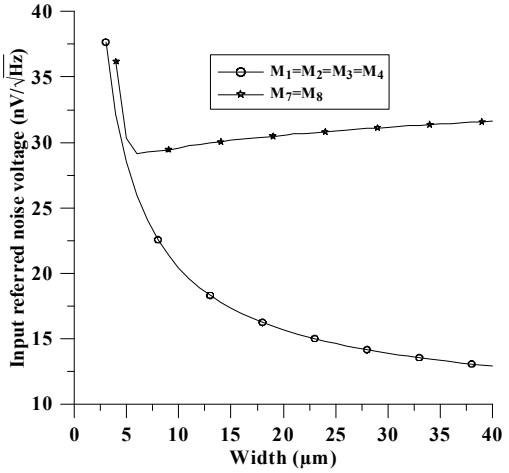

Figure 3. Input referred noise voltage at Y terminal with regard to channel widths of relevant transistors

To investigate the effects of each transistor to the overall input referred noise in DDCC, the channel width of only relevant transistor is changed whereas the others' are constant. Fig.3 and 4 can be evaluated in this respect. It is

easy to see that there is explicit agreement between theoretical sense in (3)-(5) and simulations due to the fact that g_m is proportional to the square root of the channel width. In this section, noise simulations are presented at 1MHz.

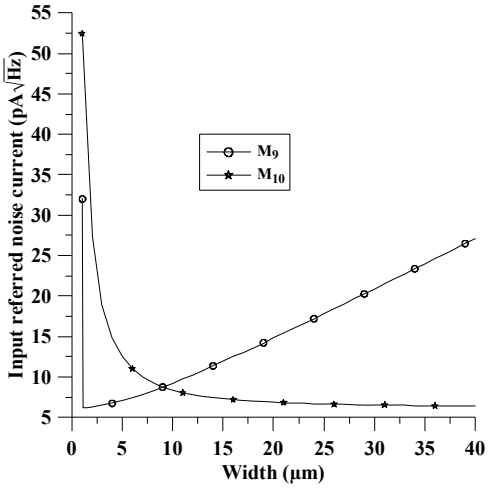

Figure 4. Input referred noise current at X terminal with regard to channel widths of relevant transistors

Drastic change of input referred noise, where width of relevant transistor is very small, arises from linear region operation. Relevant transistor in linear region can be evaluated as voltage controlled resistor and a powerful thermal noise generator. As it can be seen in (3) and (5), if channel widths of M_1-M_4 and M_{10} increase independently, current and voltage referred noise will be decreasing. Moreover, if channel widths of M_7-M_8 and M_9 decrease, these referred noise values decrease.

As it can be observed in Fig.3, 4, 5 decreasing the channel width of M_7-M_8 increases the bandwidth and decreases the noise. On the other hand, when the input differential pair transistors dominate the input referred voltage noise, increasing the channel width of M_1-M_4 will reduce the voltage noise but decrease the bandwidth.

As for the input referred current noise, the width of M_{10} not only decreases the total noise, but it also decreases the bandwidth as shown in Fig.5. However, when M_9's channel width is decreased, the current noise and bandwidth will get better till a specific point as it can be observed in Fig.5. These results strictly compromise (3) and (5).

Current gain counts upon channel widths of M_9 and M_{10}. According to (5), to reduce input referred current noise, g_{m9} must be decreased and g_{m10} must be increased. In this respect, we will have a strong trade-off between this noise and current gain. If the designer wishes to reduce the current noise at *X* port, he will take a current gain. It can be seen as important challenge about noise minimization.

The parasitic resistance at *X* terminal depends on M_1-M_4, M_9 and M_{11} as seen in (2) and (3) in the previous section. As observed in Fig.6, if channel width of M_1-M_4 increases, input resistance at *X* port will decrease. At the same time, voltage noise at *Y* terminal will decrease regarding (3). To minimize total input referred voltage noise at *X* terminal, whereas channel width of M_7-M_8 is decreased, M_1-M_4's must be increased. However, this reduction in M_7-M_8 may be deteriorating parasitic resistance at *X* port in very small widths. In the other case, when M_{10}'s channel width is increased, parasitic resistance seen from *Z* terminal will decrease whilst input referred current noise is reducing as observed in (5) and Fig.7.

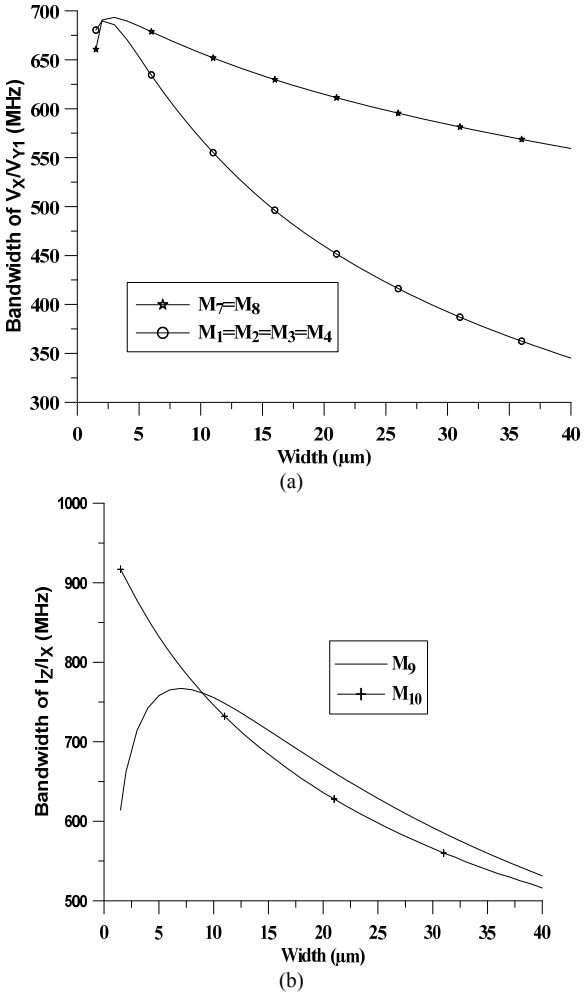

Figure 5. DDCC bandwidth with regard to channel widths of relevant transistors. a. Bandwidth of V_X/V_{Y1} b. Bandwidth of I_Z/I_X

TABLE 1. TRANSISTOR CHANNEL WIDTHS (W) EFFECTS IN TOTAL NOISE AND OTHER DESIGN KEY ISSUES OF DDCC

Noise Effect	V-noise	I-noise	BW of X	BW of Z	$\alpha=I_Z/I_X$	R_X	R_Z
W_i (i=1,2,3,4)↑	↓	-	↓	-	-	↓	-
W_j (j=7,8)↓	↓	-	↑	-	-	-	-
W_9↓	-	↓	-	↑	↑	↑	-
W_{10}↑	-	↓	-	↓	↑	-	↓

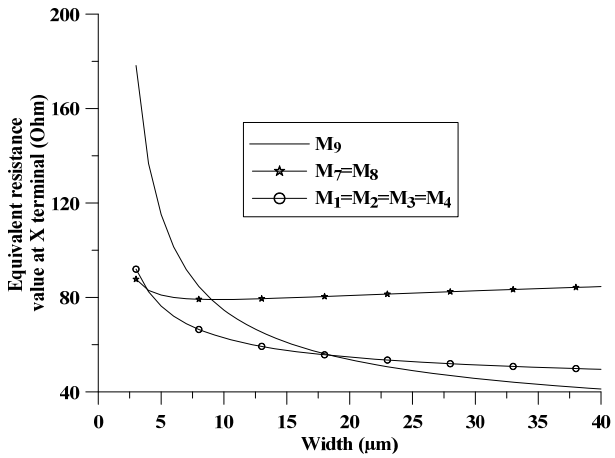

Figure 6. DDCC parasitic resistances at X port with regard to channel widths of relevant transistors.

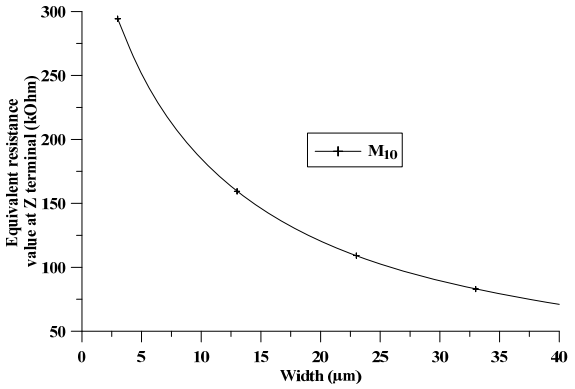

Figure 7. DDCC parasitic resistances at Z port width regard to channel width of M_{10}.

It will be beneficial to summarize all factors to designers for DDCC as observed in Table I. It establishes a noise minimization model depending on other key issues of the design such as bandwidth, current gain and parasitic resistances. This table presents a detailed map for noise minimization with regard to demands of designers. In this manner, noise minimization can be realized by decreasing channel width of M_7-M_8 and M_9 whereas increasing M_1-M_4 and M_{10}'s. However, the noise values at *X* and *Y* terminal can be optimized by considering R_X and R_Z, other enhanced non-idealities of DDCC and drawbacks.

TABLE 2. NOISE MINIMIZATION OF DDCC IN FIG.2

	Before	After	Post Layout
Input referred noise voltage (nV√Hz)	31.5	12.3	13.74
Input referred noise current (pA√Hz)	9.2	8.52	8.6
Bandwidth of X terminal (MHz)	672	412	369
Bandwidth of Z terminal (MHz)	862	508	452
R_X (Ω)	80	67.3	70.8
R_Z (kΩ)	195	196.3	198.8
Voltage swing at V_{Y1} (V)	-0.845/1.09	-0.957/0.825	-0.947/0.805

According to Table I, a robust noise minimization can be realized. When new transistor dimensions are specified in basis of aforementioned compromising of theoretical and simulation results, Table II can be obtained. Generic scheme for DDCC in Fig. 2 is re-dimensioned and significant noise reduction is obtained. Post layout results are presented with regard to optimized dimensions as well in Fig.10. These dimensions to reduce noise are given in Table III. At the end of noise minimization presented in this paper, voltage noise reduction is bigger than %55 whereas bandwidth of *X* and *Z* terminals get smaller than [25]. Parasitic resistances of *X* and *Z* port change slightly and *X* terminal resistance gets better.

TABLE 3. NEW TRANSISTOR DIMENSIONS OF DDCC IN FIG.2

Before [25]
M_1=M_2=M_3=M_4=4.5µm/0.9µm M_7 =M_8=M_9= M_{10}=9 µm/0.9µm M_5=M_6=M_{11}=M_{12}=4.5µm/0.9µm
After
M_1=M_2=M_3=M_4=30µm/0.9µm M_7 =M_8=4µm/0.9µm, M_9=M_{10}=6µm/0.9µm M_5=M_6=M_{11}=M_{12}=4.5µm/0.9µm

Moreover, current noise gets smaller and DC characteristics of DDCC are kept after minimization as shown in linearity. If one would like to reduce the current noise as well, it can be obtained by means of current gain which is about 3. In this respect, input referred current noise reduction can be given approximately %25 by keeping parasitic resistances at *X* and *Z* ports in acceptable bounds.

V. APPLICATION EXAMPLE

In the final step of simulation analyses, a filter application is presented as it can be observed in Fig.8 [5]. Second order filter circuit is constructed with DDCC and grounded passive components.

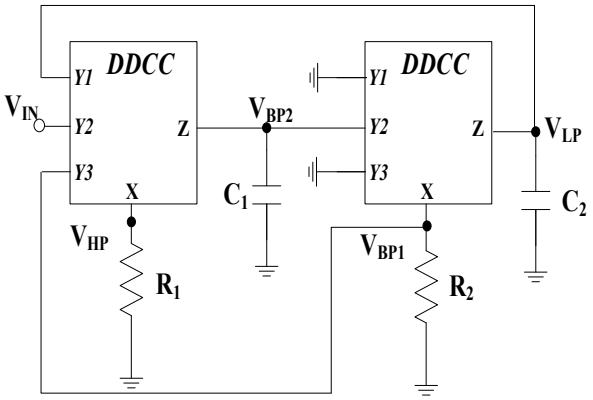

Figure. 8. DDCC filter structure (single input-four outputs) [5]

In this respect, (9) is regarding outputs of the filter in terms of passive components. In addition, natural frequency and quality factor of the circuit are given in (10) and (11). For R_1=R_2=1kΩ and C_1=C_2=150pF, *Q* and f_0 equal to 1 and 1.06MHz respectively.

$$\begin{aligned}
\frac{V_{LP}}{V_{IN}} &= \frac{\alpha^2\beta_2^2}{\alpha^2\beta_1\beta_2 + sC_2R_2\alpha\beta_2\beta_3 + s^2C_1C_2R_1R_2} \\
\frac{V_{BP1}}{V_{IN}} &= \frac{sC_2R_2\alpha_1\beta_2^2}{\alpha^2\beta_1\beta_2 + sC_2R_2\alpha\beta_2\beta_3 + s^2C_1C_2R_1R_2} \\
\frac{V_{BP2}}{V_{IN}} &= -\frac{sC_2R_2\alpha_1\beta_2}{\alpha^2\beta_1\beta_2 + sC_2R_2\alpha\beta_2\beta_3 + s^2C_1C_2R_1R_2} \\
\frac{V_{HP}}{V_{IN}} &= -\frac{s^2C_1C_2R_1R_2\beta_2}{\alpha^2\beta_1\beta_2 + sC_2R_2\alpha\beta_2\beta_3 + s^2C_1C_2R_1R_2}
\end{aligned} \tag{6}$$

$$\omega_0 = \sqrt{\frac{\alpha^2\beta_1\beta_2}{R_1R_2C_1C_2}} \tag{7}$$

$$Q = \sqrt{\frac{R_1C_1\beta_1}{R_2C_2\beta_2\beta_3}} \tag{8}$$

To verify filter characteristics over optimized dimensions, all of outputs are given in Fig.10 based on schematic and layout in Fig.9.

Post layout and schematic results are perfectly matched. In this manner, band pass filter input referred noise is measured at 1 MHz in Fig.11. This voltage noise is measured with regard to V_{BP1} terminal. Our minimization scheme successes in reduction of that input referred noise voltage approximately up to %50 as it can be seen in Fig.11. If one would like to investigate this promising result for the other output terminals, significant reductions can be obtained as well. However, the most of noise reduction is

obtained in V_{BP} terminal of this filter configuration.

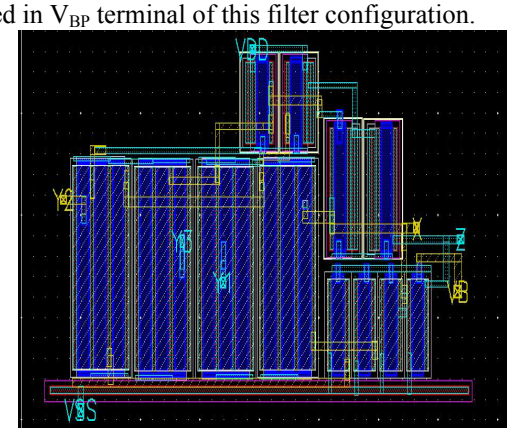

Figure 9. Layout of DDCC in Fig.2 based on optimized dimensions in Table III. (Total Area = 391,55µm^2)

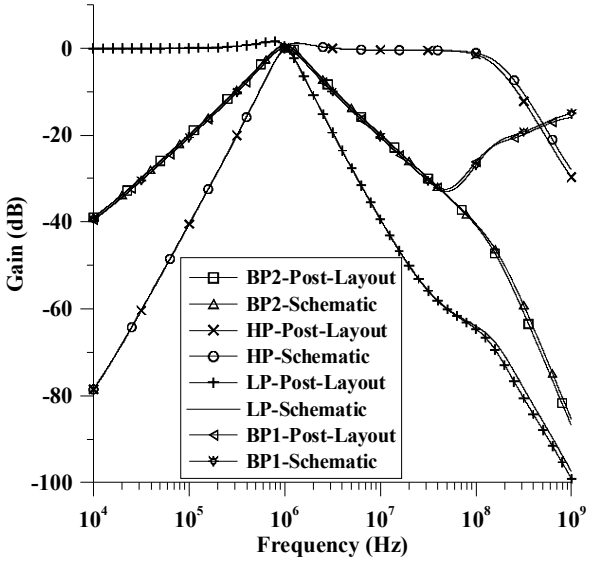

Figure 10. Simulation results of DDCC filter configurations

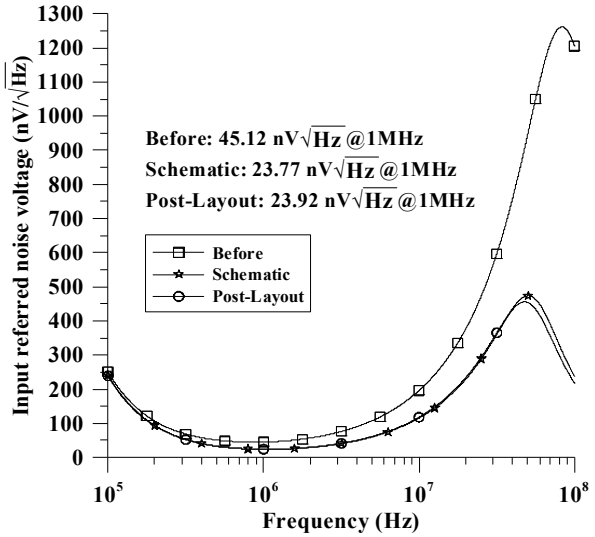

Figure 11. Input referred noise voltage of DDCC filter BP configuration

Finally, to empower the promising result of our approach, Monte Carlo analysis is presented. Monte Carlo simulations represent to designer how our optimized scheme is affected from process variations, mismatches and changes in temperature.

In Fig.12, all of process variations and mismatches are characterized for three different temperature conditions such as -40^{0}C, 25^{0}C and 105^{0}C respectively. For input referred voltage noise at 1MHz in band pass configuration of Fig.8, measurement results can be given as Fig.12. As a result, noise reduction over our optimized dimensions is kept for 100 random Monte Carlo points.

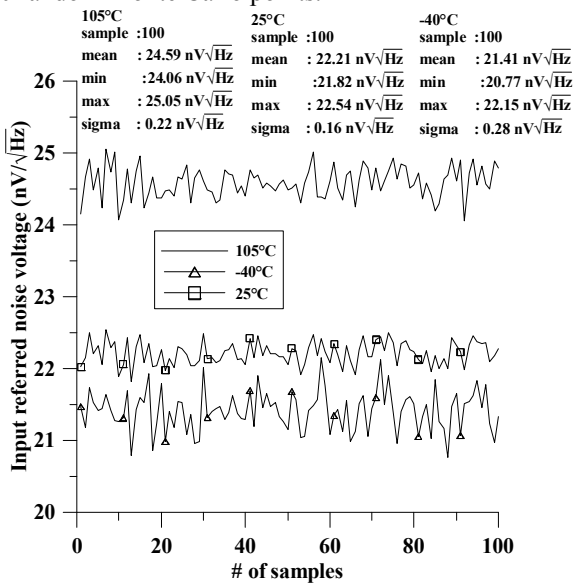

Figure 12. DDCC filter input referred voltage noise @ 1MHz for 100 random Monte Carlo points in BP configuration

VI. Conclusion

In this paper, a powerful noise minimization model is proposed for CMOS CM circuits including differential input stage. This approach is reinforced with post layout simulations and application example including Monte Carlo analysis. Furthermore, generalized noise minimization scheme presented in this paper can be useful for VM circuits employing basic components such as current conveyors as well.

In this respect, designers can elaborate their circuits in trade-off that consists of noise minimization and other design key issues due to the fact that this research shows that noise minimization directly depends on transistor geometry.

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