INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. (2015)
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.2178

Efficient power pad assignment for multi-voltage SoC and its application in floorplanning

Zhufei Chu, Yinshui Xia*,†, Lunyao Wang and Jian Wang

School of Information Science and Engineering, Ningbo University, Ningbo 315211, China

SUMMARY

Multi-voltage techniques are being developed to improve power savings by providing lower supply voltages for noncritical blocks under the performance constraint. However, the resulted lower voltage drop noise margin brings serious obstacles in power/ground (P/G) network design of the wire-bonding package. For voltage drop optimization, both block and power pad positions are important factors that need to be considered. Traditional multi-voltage floorplanning methods use rough estimation to evaluate the P/G network resource without considering the locations of power pads. To remedy this deficiency, in this paper, an efficient voltage drops aware power pad assignment (PPA) method is proposed, and it is further integrated into a floorplanning algorithm. We first present a fast PPA method for each power domain by the spring model. Then, to evaluate voltage drops during floorplanning iterations, the weighted distance from the blocks to the power pads is adopted as an optimization objective instead of time-consuming matrix computation. Experimental results on Gigascale System Research Center (GSRC) benchmark circuits indicate that the proposed method generates an optimized placement of power pads and floorplanning of blocks with high efficiency. Copyright © 2015 John Wiley & Sons, Ltd.

Received 7 May 2015; Revised 30 August 2015; Accepted 19 October 2015

KEY WORDS: voltage drops; floorplanning; multi-voltage; power pad assignment; system-on-a-chip (SoC); physical design

1. INTRODUCTION

With the increasing function-rich of system-on-a-chip (SoC) based consumer electronics, the tremendous demands on energy savings make low power design become an urgent issue. The lower supply voltage leads to less dynamic and static power dissipation in general, but it also results in the performance degradation. To optimize power effectively under the performance constraint, multi-voltage techniques assign high voltages to critical blocks for correct functionality and performance, while low voltages to noncritical ones for power savings [1]. Blocks with the same supply voltage and adjacent physical locations are grouped into one voltage island (VI) to mitigate power/ground (P/G) network design complexity [2, 3]. In terms of P/G network structure, each island has its independent power supply network while the blocks working under chip-level voltage are powered by a global power network [4].

As technology advances to nanoscale regime, voltage (IR) drop can no longer be ignored. Especially, it raises much more attentions since a nonlinear increase in the currents drawn from the P/G networks [5]. Several techniques are proposed to make the P/G network fulfill the voltage drop constraints, such as P/G network topology optimization [6, 7], wire sizing [8–11], and

*Correspondence to: Yinshui Xia, School of Information Science and Engineering, Ningbo University, Ningbo 315211, China.
†E-mail: xiayinshui@nbu.edu.cn

Copyright © 2015 John Wiley & Sons, Ltd.

decoupling capacitors configuration to alleviate the power delivery noise [12, 13]. However, those techniques are implemented only when the floorplan or placement is ready. With exploding design complexity, it is necessary to consider voltage drop issues in the early design cycle [14–17]. Once the voltage drops aware floorplan is obtained, the detailed P/G network design can be performed in the subsequent placement and routing stages that consider Steiner tree construction and electromigration issues [18, 19].

It is reported that 5% of voltage decrease may cause the circuit performance slowdown up to 15% or more [20]. Hence, designers typically limit the voltage drops within 10% of the supply voltage to guarantee faultless operation [21]. Lower supply voltage indicates that lower noise margins or smaller voltage drops are permitted on the P/G network [22]. For instance, 1.5-V supply voltages permit 150-mV voltage drop while 1.0-V supply voltages only allow 100-mV voltage drop. Compared with single-voltage SoC, the voltage drop constraints present more challenges for the P/G network design of the multi-voltage SoC. First, from a low-power perspective, a VI with a larger area and a lower supply voltage is preferred during the VI generation process. However, the permitted ultra-low voltage drops make the P/G network hard to design. Second, power pads are located at the periphery of the chip for wire-bonding package. Locations of power pads affect both the timing and voltage drops [23]. Although multiple power pads for each VI can leverage the voltage drops, it may not be practical because the power pads must compete with other signal I/Os under the limited pad resource. Thus, it is vital to consider voltage drops in P/G network design for multi-voltage SoC.

1.1. Related work

Considerable literature works addressed the P/G network synthesis problem for single voltage [24–30]. For power pad assignment (PPA) in wire-bonging packages, Sato *et al*. [29] proposed the successive pad assignment (SPA) method of power pad locations optimization by the incremental matrix inversion (IMI) to reduce computational complexity. Dubey [30] presented a cost function to evaluate different pad configurations to optimize the placement of P/G pads. Zhao *et al.* [31] put forward a mixed-integer linear programming (MILP) approach to achieve optimal placement of power pads and pins. However, these approaches are unsuitable for PPA and floorplanning co-optimization because of the computational complexity. In terms of flip-chip packages, algorithms were also proposed to optimize the placement of C4 pads [27, 28].

In contrast, there are few existing works to address the multi-voltage P/G network synthesis problem [4,32]. To evaluate the P/G network resource of VI generation in multi-voltage SoC floorplanning, many researchers [33, 34] adopt the model defined by Lee *et al*. [3], which is $\sum_{i=1}^{k} u_i$, where k is the number of VIs while u_i is the half perimeter wirelength of the bounding box of the ith island. The model is a rough estimation which lacks P/G network details such as power pad locations and P/G network topology. Zhou *et al*. considered the power delivery problem in VI designs during the floorplanning process to reduce the design iterations [4]. They proved that it is unnecessary to find an optimal pitch parameter for P/G network during floorplanning stage. Instead, they proposed a voltage drops aware floorplanning method with a fixed topology P/G network to estimate voltage drops. However, the authors only considered the global P/G network for blocks working under chip-level voltage, and the power pads are fixed at the chip corners. To minimize total power stripe area, Lee *et al*. proposed an optimization technique for multiple power domains based on simulated annealing (SA) [32]. The P/G network area optimization is carried out in the post-floorplanning stage with manually generated VIs and power pads.

The voltage drops are mainly determined by the load current and effective resistance of the block. The effective resistance is proportional to the distance from the power pad to the block. Hence, both block and power pad positions are important factors that need to be considered for voltage drop optimization. In previous multi-voltage works, the problems of voltage assignment, VI generation, and floorplanning are simultaneously solved. Apart from the issues above, in our work, we also need to solve PPA and P/G network analysis, which is much more complicated. To the best of our knowledge, it is the first study on the PPA for multi-voltage chips.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

1.2. Contributions of the proposed approach

We summarize our contributions as follows.

(1) For a floorplan candidate, after voltage assignment and VI generation stages, we present a fast voltage drops aware PPA method by spring model. Compared with the greedy method, we can obtain near-optimal solutions with much lower computational cost. The method is applicable to be integrated into floorplanning algorithms.
(2) For P/G network analysis, according to the recently proposed closed-form expressions for voltage drops [35, 36], we explore the relationships among the significant parameters that affect the voltage drops. Instead of time-consuming matrix computation to obtain voltage drops, a weighted distance from the blocks to the power pads is incorporated into the cost function to guide the floorplanning for voltage drop optimization.
(3) For the proposed floorplanning algorithm, we solve voltage assignment, VI generation, PPA, P/G network analysis, and floorplanning concurrently. Because the mentioned problems are tightly interrelated, simultaneously solving the problems is essential to produce a reliable and low power multi-voltage SoC chip.

A preliminary conference version of our research was published in [37]. It only presented the basic idea of using the spring-based model to determine optimized power pad locations for VIs. The main drawback of that paper lies in its experimental parts. It constrained each VI with only one power pad, which is far from practices. In addition, comparisons with the state-of-the-art techniques are also missing. Hence, it did not provide enough evidence to demonstrate its effectiveness in entire multi-voltage floorplanning flow. In this paper, we extend our work and formulate each VI with a user-defined number of power pads. Extensive comparison tests are performed to validate the effectiveness of both PPA and floorplanning.

1.3. Organization of this paper

The remainder of the paper is organized as follows. The motivational example and problem formulation are demonstrated in Section 2. Preliminaries are given in Section 3. In Section 4, the PPA method by spring model is proposed. The floorplanning algorithm with a weighted voltage drops aware cost function is detailed in Section 5. The experimental results are displayed and discussed in Section 6, followed by the conclusions in Section 7.

2. MOTIVATIONS AND PROBLEM FORMULATION

2.1. Motivational example

Because the P/G network of multi-voltage SoC contains a global network for the blocks working under chip-level voltage and an independent one for each VI, the locations of power pads would affect the voltage drop directly. As shown in Figure 1, a floorplan of multi-voltage SoC with two VIs is demonstrated. For single voltage SoCs, the power pads are always fixed in the four corners or centers of the chip boundaries (shown as the dashed squares in the Figure 1). If we choose the power pads among those eight candidates for each VI, the voltage drops may not be the optimized and extra P/G network resource may be consumed. Moreover, to facilitate low power, a VI working under a lower voltage but with a larger area is preferred to be generated. For example, the VI working under 1.0 V has a larger area than the one working under 1.3 V in Figure 1. Thus, the noise margin of voltage drops becomes smaller for such kind of VIs. However, the voltage drops can be improved by PPA carefully. It seems that the power pads p_1, p_2, and p_3 shown in Figure 1 can give overall consideration to the blocks within each power domain, which is expected to optimize the voltage drops.

2.2. Problem formulation

A set of n soft blocks with area $A_1, A_2, A_3, \cdots A_n$ and the lower and upper aspect ratios bounds $[l_i, u_i]$, $i \in [1, n]$ are given; a set of I/O pads, $P = \{p_0, p_1, p_2, \cdots p_k\}$, which are placed along the boundaries of

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

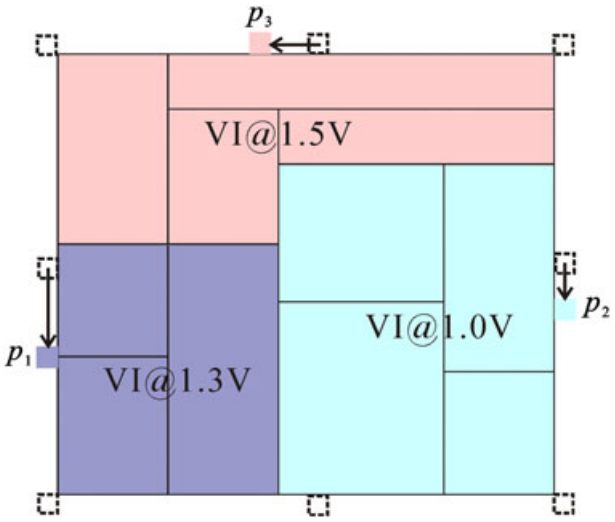

Figure 1. A floorplan of multi-voltage SoC with two VIs and its power pads.

the floorplan region and a set of connecting nets are also provided. For each block, the legal discrete voltage levels are also known. The power consumption of the ith block is $A_i v_j^2$, where v_j, $j \in [1, m]$, is current working voltage selected from the legal voltage levels. It is assumed that the block working under the legal voltage levels can satisfy the timing constraint. Here, we do not consider timing explicitly in our formulation, which is the same as previous works [33, 34]. An example of problem inputs is shown in Figure 2, where the output of the problem is the floorplan of all blocks and the positions of power pads.

3. PRELIMINARIES

3.1. P/G network structure

The mesh-based P/G network has a uniform structure which can be constructed before the placement/floorplanning stage. Thus, it is more flexible for voltage violation estimation compared with tree-based P/G network. A general mesh-based P/G network structure is shown in Figure 3. The P/G network at the top level mainly consists of a core ring and power trunks, which lies over

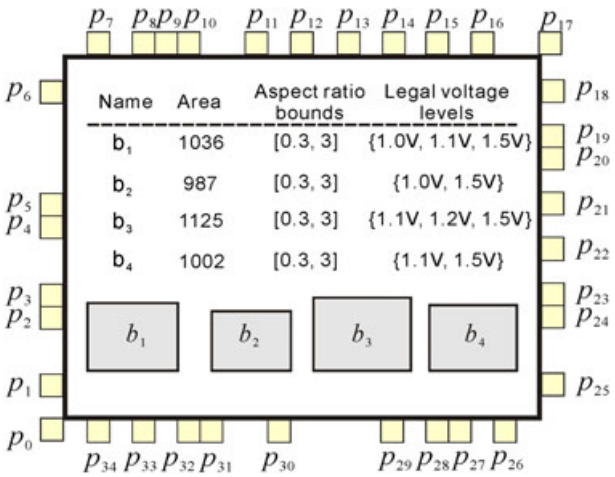

Figure 2. An example of problem inputs.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

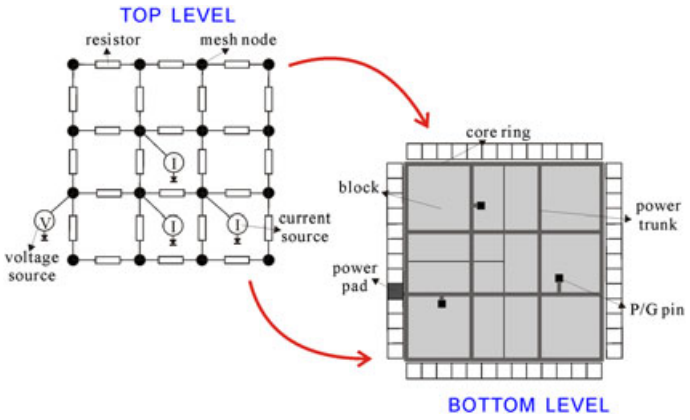

Figure 3. The mesh-based P/G network structure and its equivalent circuit model.

the blocks at the bottom level. The supply voltages are delivered to the blocks by connecting the P/G pin and the power mesh. Because of the resistance of the power trunks and the load currents of the blocks, the voltage obtained from the power pad cannot be completely delivered. Such voltage reduction is called as the voltage drops.

The structure is modeled as a resistive P/G network for static analysis. Although transient analysis which considers resistance, capacitance, and inductance (RCL) simultaneously is more accurate, the analysis is computationally expensive and unnecessary during floorplanning. The static resistive P/G network is sufficient to evaluate the voltage violations. In its equivalent circuit model, the blocks are modeled as the current sources. The sources are connected to the nearest mesh nodes. The supply voltages from the power pads are modeled as the voltage sources. According to the modified nodal analysis (MNA) [38], the static analysis of a P/G network is formulated as follows:

$$\mathbf{GV} = \mathbf{I} \tag{1-a}$$

$$\mathbf{V} = \mathbf{G}^{-1}\mathbf{I} \tag{1-b}$$

where $\mathbf{G}$ is the conductance matrix of the resistors, $\mathbf{V}$ is the vector of mesh node voltages, while $\mathbf{I}$ is the vector of current sources. Assume that the P/G network has m mesh nodes and p voltage sources, then the dimension of the matrix $\mathbf{G}$ is $(m+p)\times(m+p)$, and $\mathbf{V}$ and $\mathbf{I}$ are $(m+p)\times 1$. The matrix inversion computation is time consuming. Because the matrix $\mathbf{G}$ is a sparse positive definite matrix, we adopt the conjugate gradient method, which is based on iterative method, to solve this problem. Apart from voltage drop constraints, the minimum P/G trunk width constraint and the electromigration constraint should also be satisfied.

3.2. *Current source modeling*

To explore the current behavior of each block is an essential step for voltage drop analysis. Because the current may vary during the simulation time, the current sources of these blocks are also time-variant ones. The extreme accuracy is unnecessary and impossible in the limited time. Using the peak current of each block for static voltage drops estimation can obtain an upper bound of actual drop [20]. The current upper bounds can guarantee the circuit operates correctly even under the worst-case scenarios. Consequently, the peak current modeling is widely used in the literature [39–44] for voltage drop optimization.

Because we consider soft blocks which do not have the exact placement of the standard cells at the floorplanning stage, our current model uses the peak current function, which is based on worst-case scenarios and takes account of area, switching activity, and current density simultaneously, to determine the load current. The peak current function is formulated as follows:

$$f(i) = I^{i}_{peak} = A_i \times S_i \times J_i \tag{2}$$

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

where A_i, S_i, and J_i are the area, switching activity, and current density of block i, respectively. The switching activity can be generated randomly or by exploring the extensive microarchitectural profiling [45]. Generally, we randomly divide the circuit into three partitions in which the blocks are assigned high switching activity, medium switching activity, or low switching activity. For the current density of each block, it can be a uniform or non-uniform distribution.

4. PPA FOR EACH POWER DOMAIN

To solve the problem defined in Section 2.2, we first propose a PPA method to optimize the voltage drops. For a floorplan candidate, each power domain has its independent power pads. The PPA is implemented after voltage assignment stage. Once the VIs are generated, the power pads are determined by PPA. Then, a fixed P/G mesh network whose metal pitches/widths are fixed is constructed for P/G network analysis. Given a floorplan which contains K VIs and a set of I/O pads (power pad candidates) which are placed along the boundaries of the floorplan region, the problem in this section is to assign the required number of power pads (the number of power pads is user defined) for each VI with the objective of minimizing voltage drops. Note that different VIs cannot share the same power pad. We first demonstrate how to determine the only-one power pad for the given VI in Section 4.1. Then we generalize the method to solve multiple pads problem by floorplan partitioning in Section 4.3.

4.1. Basic algorithms

P/G mesh network construction is determined by power pad locations, metal pitches, and widths. Given the fixed metal pitches/widths, different power pad locations lead to different P/G mesh structures. For each power pad candidate, we construct a P/G mesh network using fixed metal pitches/widths to evaluate the current floorplan. Then the one which obtains the minimum number of voltage violations or minimum voltage drop is the optimal PPA solution. If the dimension of the conductance matrix is $(m+p)^2$, then the time complexity of the conjugate gradient method is $O((m+p)^2)$. Assume that the number of power pad candidates is q, the required pads' number for i th VI is n_i, then the basic algorithm runs in $\sum_{\text{all } K \text{ VIs}} O\left((m+p)^2 C_q^{n_i}\right)$ times for K VIs.

Another algorithm proposed by Dubey [30] adopts a cost function to optimize power pads' placement by evaluating different pad configurations. The objective is to minimize the total distance from the block to 'the most effective power pad', which has the minimum distance to the block compared with other power pads. Therefore, for each block, the algorithm should sort the distance sourced from different power pads to find 'the most effective power pad'. If the number of blocks in the i th VI is l_i, then Dubey's algorithm runs in $\sum_{all\ K\ VIs} O\left(l_i {n_i}^2 \mathrm{C}_q^{n_i}\right)$ times for K VIs.

4.2. PPA by spring model to determine single pad

The basic algorithms are computationally expensive. They are unsuitable to be incorporated into floorplanning algorithms. To realize fast PPA algorithm, an efficient and effective voltage drop estimation method should be exploited. As this paper focuses on the resistive voltage drops analysis in a uniform mesh structure, the voltage drops between the power pad and an arbitrary current load are mainly caused by the *effective resistance*. As shown in Figure 4, there are one voltage supply at the power pad and one current load, which are denoted as V_{pad} and I_{load}, respectively. The voltage at N_l is $V_{pad} - R_{sl} \times I_{load}$. The corresponding voltage drop at N_l is

$$V_{drop}^{N_l} = I_{load} \times R_{sl} \tag{3}$$

where R_{sl} is the effective resistance between nodes N_s and N_l.

According to (3), the voltage drop between the power pad and the current load is dependent upon the effective resistance between these two nodes, while the effective resistance is directly proportional to the corresponding Euclidean distance. Inspired by this phenomenon, we propose a spring model based

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

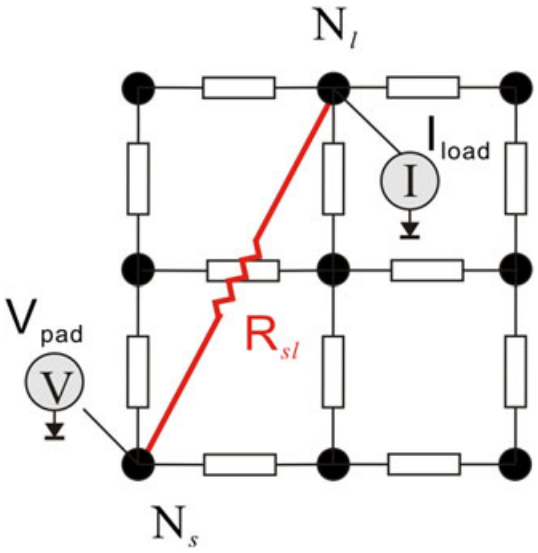

Figure 4. The node voltage computation when there are one power pad and one load current source.

on the physical analogy of Hooke's law. The power pads and the current loads connected by power mesh network can be viewed as exerting attractive spring forces on one another. The spring system-based approach is suitable for wirelength optimization and computational complexity reduction. It has been successfully applied in force driven placement and pin assignment [46]. Given the spring constant k and the offset x, according to the Hook's law, the force exerted by the spring is

$$F = kx. \tag{4}$$

By comparing (3) and (4), it is found that the spring force has good features to the 'analogy' of the voltage drops. The main reasons are described as follows.

(1) On k versus I_{load}, they are both the main contributors of the spring force and the voltage drops, respectively.
(2) On x versus R_{sl}, the effective resistance R_{sl} is directly proportional to the Euclidean distance between the two nodes, which is similar to the spring offset x.

Therefore, the spring model is suitable for the voltage drop estimation.

Next, we construct a spring system to determine the PPA solution. There are generally two basic rules for PPA. First, locations of power pads should be given full considerations of all blocks in the VI. Second, in case of fast voltage drops, the power-hungry blocks are preferred to be placed near the power pad [43, 44].

Assume that the center of each block in the VI connects one end of a spring while the other ends of all springs are connected together. The springs, which have zero-length, construct a spring system. Under the force exerted by the springs, the spring system can reach the equilibrium configuration. Take a floorplan shown in Figure 5 as an example, there are three blocks b_1, b_2, and b_3 and hence three springs. One end of each spring is connected to the center of each block, and the other ends of springs are connected together.

Next, the spring constants are assigned, which is important for the resulted spring system. Based on the rule that power-hungry blocks are better placed near the power pad, the high absorbed current blocks are identified and assigned with higher spring constant. Specifically, the peak current of each block is first calculated. Then the peak current values are sorted in descending order. If the block b_{min} obtains the minimum peak current c_{min}, then the spring constant k_i can be defined as follows:

$$k_i = \alpha \times \frac{c_i}{c_{min}} \tag{5}$$

where α is a user specified constant and c_i is the peak current of block b_i.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

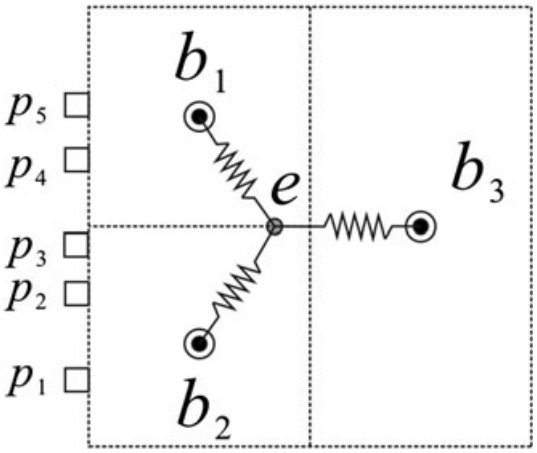

Figure 5. A spring system.

When the spring system reaches its equilibrium configuration, we call the node e which is connected by all springs as the *force equilibrium node*. If the spring constants of all springs are equal, it can be easily obtained that the total quadratic distance from the force equilibrium node to the center of each block is the minimum. Compared with equal spring constant setting, our model makes the force equilibrium node move to the direction of the blocks with higher absorbed current, which gives full consideration for all blocks. Thereby, the force equilibrium node is a good choice for the PPA.

In a flip-chip package, we may assign the power pad in the location of the force equilibrium node. However, in a wire-bonding package, we must select one from the power pad candidates who are placed along the boundaries of the floorplan region. In that situation, we need to find a pad that makes the force equilibrium node get the minimum offset. When the spring system reaches force equilibrium, the energy of the spring system is zero. If the offset from the power pad to the force equilibrium node is d, then the smaller d leads the smaller energy. Hence, we choose the power pad which has the minimum distance (offset) to force equilibrium node as the power pad solution.

To summarize, we first assign spring constants according to the peak current of each block. Then, the force equilibrium node is determined. Finally, the distance from the power pad candidates to the force equilibrium node is calculated. Hence, if the number of I/O pads is q and the number of blocks in i th VI is l_i, the proposed algorithm runs in $\sum_{\text{all } K \text{ VIs}} O(n_i(2l_i + q))$ times, which will get a significant time improvement compared with the basic algorithms.

4.3. Generalization to determine multi-pads

Because the PPA method described in Section 4.2 can only produce one optimized power pad, we need to partition one VI into several sub-VIs to determine multi-pads. For each sub-VI, we perform our proposed PPA method to generate an optimized placement of power pads. The number of sub-VIs is equal to the user defined number of power pads.

Because of the principle of spatial locality, the interactions between the power pads and the current loads are more prominent among components in close proximity [47]. This makes the sub-VI partitioning possible to determine more than one power pad for a whole VI. Because each sub-VI has a power pad, by merging the sub-VIs, the whole VI has its required number of power pads. This is similar to a large power grid design method which partitions the power grid into several smaller parts where each partition is analyzed separately.

Because the power density of the VI is the main factor to influence the voltage drops, the partitioning step mainly considers the constraints of power density and locations of VIs. Several cases are possible in order to partition VIs. For example, a VI with larger power density can be partitioned into the required number of parts with similar power density. Alternatively, a VI with non-contiguous regions can be partitioned into several parts according to their physical locations.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Specifically, by considering the physical locations and the power density of VIs simultaneously, we use a two-stage algorithm shown in Figure 6 to partition the VIs into the required parts. First, we identify the VIs and record the central coordinates of all blocks as data points (line 1). The blocks are then clustered into required parts based on K-means clustering algorithm (lines 2–8). K-means is a popular clustering algorithm in reality because of their simplicity and effectiveness, whose objective is to partition the original data points into several groups so that the data points within the same cluster are compact while those in different clusters are well separated [48, 49]. Because the block coordinates are used as data points, the adjacent blocks tend to cluster together. The K-means algorithm can roughly produce clusters at the same size as the number of data points. However, the power density of clusters may have a great difference. Therefore, in the second stage, power density aware post refinement method is used to fine-tuning the data points in different clusters until all clusters have similar power density (lines 9–13).

5. VOLTAGE DROPS AWARE FLOORPLANNING

We have presented a fast voltage drops aware PPA method in Section 4, where the floorplan and blocks are fixed. In fact, as we mentioned previously, the positions of both blocks and power pads are important factors for voltage drop optimization. Thus, the two factors should not be considered separately. In this section, we further give a voltage drops aware floorplanning method to optimize the positions of both blocks and power pads simultaneously.

5.1. Floorplanning implementation details

SA algorithm is the most popular method of solving floorplanning problems. Based on SA algorithm, various approaches are proposed to improve the algorithm efficiency [50–54]. However, the main drawback is that these techniques do not have a good scalability. Because slicing trees are the traditional representations for the floorplan, SA needs to search numerous slicing trees by perturbing. Therefore, the large circuits always generate non-linear increased solution space, which consumes much more time. Recently, a fast, high-quality, scalable, and nonstochastic fixed-outline floorplanning algorithm named *DeFer* was proposed [55], which generalizes the notion of slicing tree based on the principle of deferred decision making (DDM). Although it was originally designed for fixed-outline floorplanning, DeFer has a good flexibility to handle other floorplanning problems. In this paper, we adopt DeFer as the floorplanner to validate our PPA and MSV floorplaning problem.

To clarify the algorithm, some techniques used in DeFer are reviewed. For traditional slicing tree, the parent node of two children nodes is always labeled as 'H' or 'V' to indicate the nodes be compacted horizontally or vertically. Besides, the order of two children nodes guides the relative

Algorithm 1: Floorplan Partition Algorithm

input : The voltage of VI *vol*, the number of required parts *nParts*
output: The required *nParts* clusters

/* The first stage */
1 For all blocks, if the working voltage of block equals to *vol*, record the central coordinates of the block into a data array;
2 Randomly generate *nParts* centroids;
3 **repeat**
4 Calculate the Euclidean distance from all data points to centroids;
5 Produce new clusters;
6 Calculate new centroids;
7 Evaluate the sum of squared errors of current clusters and compare it with the previous one;
8 **until** *The solution converges*;
/* The second stage */
9 Sort the centroids by descending size of their associated clusters in an array;
10 **repeat**
11 For clusters i ($1 \leq i \leq nParts - 1$), push the data points in cluster i with minimal distance to any other centroid j ($i < j \leq nParts$) off to j;
12 Calculate new centroids;
13 **until** *all clusters have similar power density*;

Figure 6. Pseudo code of the K-means based floorplan partition algorithm.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

positions such as top-down or left-right in the layout. In contrast, the generalized slicing tree proposed in DeFer labels all the parent nodes as '+', which indicates the orientation and order of two children nodes are not determined in this step. As shown in Figures 7(a) and (b), each parent node in the slicing tree incorporates 16 possible slicing layouts generated by two children nodes. All the possible layouts are recorded in the shape curves of parent nodes. By adding and merging the shape curves of child nodes, the final shape curve can be obtained in the root node (shown in Figure 7(c)). Thus we can obtain the points which meet the fixed-outline constraint in the curve. The orientations of all nodes can be determined by back-tracing these valid nodes from top-down. Finally, by swapping and mirroring the order of child nodes to optimize wirelength, the orders of all nodes are determined. As shown in Figure 7(d), the swapping operation switches the left and right subfloorplans with the relative positions among the blocks are unchanged. In contrast, the mirroring operation first figures out the symmetrical axis of the outline of their parent floorplan, and then attempts to mirror them based on this axis.

5.2. *Algorithm overview*

The pseudo code of the algorithm is shown in Figure 8. Given a slicing tree representation of a floorplan with initial cost *init_cost*, we can perform *voltage partitioning* to obtain K VIs based on the dynamic programming method [33,56] (line 3). Then, the VIs in the floorplan are identified, and the power pads are assigned to each VI using our method shown in Section 4 (line 4). According to the locations of power pads, a P/G network with fixed pitch and width is constructed for each power domain. By attaching a current source to the power mesh node, the node voltage can be obtained by the conjugate gradient method. Then, the total number of voltage violations is obtained (line 5). The current cost *curr_cost* is calculated by evaluating the weighted cost function (line 6). If $curr\_cost >= init\_cost$, which means the solution has no improvement, the swapping or mirroring operation that makes the blocks moved will be undone (line 7); otherwise the value of *init_cost* will be updated (line 9). The algorithm will be terminated until all parent nodes are traversed.

Because we do PPA for VIs one by one, we set up flags for all power pad candidates to avoid multiple VIs competing for the same power pad. The initial flag values of all candidates are set to FALSE. Once the power pad is determined by a specific VI, then the pad corresponding flag is set to TRUE. For the next VI, the method will explore the remaining power pad candidates whose flags are FALSE.

5.3. *Cost function*

During floorplanning, the weighted cost function that considers the total cost of the power, wirelength, and the number of voltage violations is used to evaluate the quality of the floorplan. The cost function is

$$cost = \alpha \times power + \beta \times wireLength + \gamma \times numVio \tag{6}$$

where *power*, *wireLength*, and *numVio* are the power of the K VIs, the total wirelength, and the number of violations of the P/G network for all power domains, respectively. The values of power, total wirelength, and number of violation nodes are not in the same order of magnitude. We first

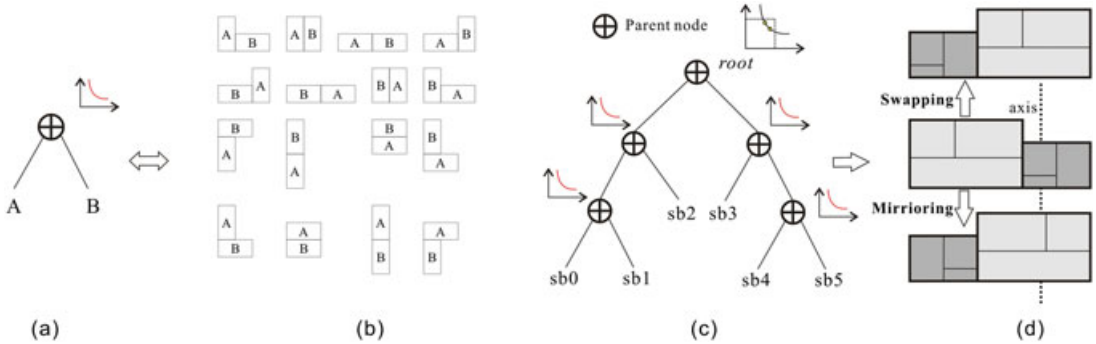

Figure 7. (a) Generalized slicing tree; (b) the corresponding sixteen possible layouts; (c) floorplan representation; (d) swapping and mirroring operations.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Algorithm 2: vDrop_Floorplanning Algorithm

input : A floorplan obtained by an area-oriented fixed-outline floorplanner
output: An optimized floorplan with the objective of power, wirelength, and voltage violations minimized

```
1  init_cost ← ∞;
2  repeat
3      Do the voltage partitioning to generate the desired K VIs;
4      Identify the VIs, partition the VIs into required parts and do PPA;
5      Analyse the P/G network to estimate voltage violations;
6      Calculate the weighted cost function to obtain the current cost curr_cost;
7      if curr_cost ≥ init_cost then Undo the block move;
8      else
9          curr_cost ← init_cost
10     end
11 until The greedy swapping and mirroring are not finished for all parent nodes;
```

Figure 8. Pseudo code for the proposed voltage drops aware floorplanning algorithm.

obtain their initial values at the beginning of the algorithm, then the parameters α, β, and γ are set as the weights to make the three terms similar in weighting. The cost function can be also extended to consider other optimization objectives such as leakage power and temperature [57, 58].

In literature, either the number of total voltage violations or maximum voltage drop is used as one optimization term in the objective function. The evaluation is straightforward and effective. However, the evaluation is computationally expensive because we must calculate the node voltages of the whole P/G network, and then the number of total voltage violations and the values of maximum voltage drop are obtained. It inevitably introduces too much CPU time for the matrix inversion in (1). To further speed up the algorithm, we propose an approximation method to estimate the voltage drops without detailed computing, which trades off accuracy and time.

According to the linear circuit theory and the closed-form expression of voltage drops, it is known that effective resistance is proportional to the distance from blocks to power pads, and blocks which have a higher load current are preferred to be placed near the power pad. Thus, we can use the weighted distance from blocks to power pads as the evaluation criterion for voltage drops. The lower weighted distance leads to fewer voltage violations. We replace the third term in (6) with

$$\sum_{allVIs}\sum_{i}[k_i \times dist(b_i, pad)] \tag{7}$$

where k_i (defined in (5)) is the weight of block i, $dist(b_i, pad)$ is the Manhattan distance from block b_i to the power pad pad. Hence, the modified cost function is

$$\begin{aligned} cost = {} & \alpha \times power + \beta \times wirelength \\ & + \gamma \times \sum_{allVIs}\sum_{i}[k_i \times dist(b_i, pad)]. \end{aligned} \tag{8}$$

Note that the parameters α, β, and γ are also adjusted at the beginning of the algorithm to make three terms similar in weighting.

6. EXPERIMENTAL RESULTS

The proposed voltage drops aware PPA and floorplanning methodology is implemented in C language. Experiments are performed on Gigascale Systems Research Center (GSRC) benchmark circuits. All experiments are carried out on 2.70-GHz Intel Pentium (R) Dual-Core CPU E5400 and 2-GB RAM. The pitch and width of the P/G mesh are 40 mm and 4 mm, respectively. The resistivity of the metal layers is 0.095 Ω per square, while the current density is a uniform distribution 10 A/mm^2. The legal voltage levels and power consumption are provided by the authors of [33], and it is randomly generated from the voltage set 1.0 V, 1.1 V, 1.2 V, 1.3 V, and 1.5 V (chip-level voltage). To evaluate the proposed method in the most rigorous condition, we constrain that each VI only has a single power pad in Sections 6.1. Finally, we give our comparison results of multi-pads in Section 6.4.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

6.1. Experiments on the voltage drops aware floorplanning

Table I shows the comparison results between our approach and a state-of-the-art floorplanner, *DeFer*, which only considers area and wirelength optimization. For fair comparison, DeFer first obtains the final floorplan solution, and then the power pads are assigned by our proposed PPA method.

In Table I, '#VI' stands for the number of VIs; 'Voltages' lists the operating voltage of each VI; 'Thre (%)' indicates the predefined percentage of the voltage drops threshold; 'maxD' is the maximum voltage drop in the P/G network; '#vio' stands for the number of violation nodes (the voltage drop is larger than the predefined voltage drop threshold) and the total nodes; 'WL' and 'Time' stand for the total wirelength and run time, respectively.

Note that the thresholds of circuits are derived by evaluating the different test cases. The standard setting of the threshold is 10%. However, as mentioned in Section 1, to save power, the generated VIs may contain one with a larger area and a lower voltage level, which makes that lower noise margins or smaller voltage drops are permitted on the P/G network. For instance, circuits n10 and n30 have such a kind of VI. Hence, instead of 10% threshold, we increase it to 12% and 13%, respectively, to guarantee the satisfaction of the voltage drop constraints.

From Table I, the results of the proposed method show that the maximum voltage drop in the P/G network is reduced 5.0%, and the voltages of all the mesh nodes can satisfy the voltage drops threshold. The wirelength increases 2.4%, which is an acceptable tradeoff. This is mainly because our proposed method forces blocks with higher load current placed near the power pads. As a result, it seeks the compromise of the wirelength for voltage drop reduction. Besides, it is reasonable that our method runs much slower than the traditional one because our floorplanner performs P/G network analysis, such as conductance matrix construction and time-consuming matrix inversion computation, for every floorplan candidate during floorplanning iterations.

6.2. Experiments on the PPA method

To the best of our knowledge, there is no previous work to address the PPA for multi-voltage chips. The closest approach to our problem is [4], which targets the power delivery problem in VI designs, and considers voltage drops during the floorplanning process to reduce design iterations. However, they assume that the power pads are fixed at the corners of the chip boundary. Moreover, the working voltage of each block is also fixed. To compare our approach with [4], we constrain the power pads being fixed at the four corners and centers of the chip boundary (eight power pad candidates). We also use the same cost function for floorplanning. Although [4] adopts the SA scheme, which is different from our DeFer-based approach, the advantages of our approach on solution quality and CPU time were demonstrated in our previous work [56]. The results obtained by the two methods are listed in Table II.

Generally, our method can generate 5.8% smaller voltage drops and competitive wirelength results versus fixed power pad method. The main reason for such an improvement is our method can give full considerations on all blocks in the VI. In contrast, fixed power pad locations limited the P/G network performance. Moreover, the voltage drops are further optimized by using the cost function, which guides the blocks with higher load current being placed near the power pad. Note that the difference

Table I. Experimental results on voltage drop aware floorplanning.

				Voltage drop aware floorplanning				Traditional floorplanning[55]			
Circuit	#VI	Voltages (V)	Thre (%)	maxD (mV)	#vio	WL	Time (s)	maxD (mV)	#vio	WL	Time (s)
n10	2	1.3,1.5	13	171	0/227	13 609	9.07	176	14/227	13 542	0.48
n30	3	1.0,1.1,1.5	12	91	0/280	42 290	22.48	100	18/215	38 998	0.4
n50	3	1.0,1.1,1.2	10	120	0/270	77 864	104.94	131	72/230	75 238	1.08
n100	3	1.0,1.1,1.5	10	101	0/332	156 070	241.5	103	54/320	149 972	1.22
n200	3	1.0,1.2,1.5	10	99	0/281	274 996	555.05	103	27/301	272 200	1.67
n300	3	1.0,1.1,1.5	10	142	0/495	472 717	1819.51	147	61/465	462 687	3.19
Avg.				1.00		1.00		1.05		0.976	

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Table II. Experimental results on PPA method.

	Our method			Fixed power pad method [4]		
Circuit	maxD (mV)	#vio	WL	maxD (mV)	#vio	WL
n10	171	0/227	13 609	173	123/225	13 888
n30	91	0/280	42 290	102	11/265	38 774
n50	120	0/270	77 864	129	105/247	77 492
n100	101	0/332	156 070	104	146/315	156 070
n200	99	0/281	274 996	103	114/284	273 133
n300	142	0/495	472 717	155	278/385	472 037
Avg.	1.00		1.00	1.058		0.994

of the two methods mainly lies in the number and positions of power pad candidates. The constraints on voltage drops and the optimization objectives are all the same. Hence, the wirelengths of the two methods are not qualitatively different.

Because one of the main contributions in [4] is the proof of unnecessary finding an optimal pitch parameter for P/G network during floorplanning stage, we also compare the voltage drops under different pitches, such as 40 mm (results in Table II), 50 mm, and 60 mm. Larger pitch leads to fewer nodes of power mesh, and hence less CPU time to solve the conductance matrix. However, the resulted voltage drops are also degraded. The data plotted in Figure 9 show that the voltage drops are monotonously increased as the pitch grows. Hence, different from [4], despite the pitch parameter, the power pad locations should be also considered by floorplanning for multi-voltage SoC designs.

6.3. *Experiments on the cost function*

The experimental results obtained by different cost functions are presented in Table III. Generally, by using (8), there is 2.1% voltage drops degradation compared with using (6). However, the CPU time is significantly improved. Because no detailed matrix computation is needed during floorplanning iterations, it is reasonable for CPU time improvement at the expense of accuracy. Compared with traditional floorplanning results shown in Table I, the performance of the voltage drop is optimized by $(5.0-2.1)\%=2.9\%$. This indicates that our proposed voltage drops approximation method captures the key feature of the voltage drops.

6.4. *Experiments on the multiple pads*

Finally, we compare our method with the basic algorithm described in Section 4.1 and previous work [30] which also consider power pads placement for wire-bonding packages. For fair comparison, we

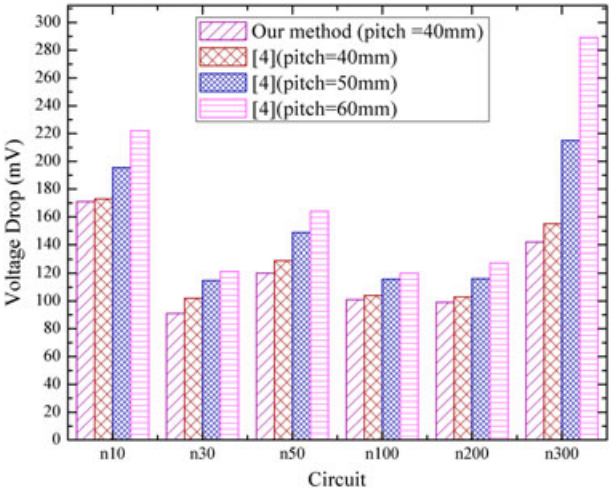

Figure 9. The voltage drops comparison for different pitches.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Table III. Experimental results on different cost function.

	Using (6) as cost function				Using (8) as cost function			
Circuit	maxD (mV)	#vio	WL	Time (s)	maxD (mV)	#vio	WL	Time (s)
n10	171	0/227	13 609	9.07	172	7/227	13 554	0.54
n30	91	0/280	42 290	22.48	97	13/215	41 105	0.45
n50	120	0/270	77 864	104.94	122	16/241	76 278	1.34
n100	101	0/332	156 070	241.5	101	6/308	156 824	1.96
n200	99	0/281	274 996	555.05	101	19/301	277 172	4.46
n300	142	0/495	472 717	1819.51	146	20/435	476 642	7.65
Avg.	1.00		1.00		1.021		1.004	

first obtain the final floorplan solution, and then the power pads are assigned by different methods. The required number of power pads for each VI depends upon the power density or area. Hence, assume that p_i is the power density percentage that the i th VI occupies, we set the number of power pads for each VI by equation (9). Users can modify (9) to obtain the required number of power pads.

$$\text{Number of power pads} = \begin{cases} 1 & \text{if } p_i < 20\% \\ 2 & \text{if } 20\% \le p_i < 60\% \\ 3 & \text{else} \end{cases} \tag{9}$$

Previous work [30] proposed a cost function to optimize the voltage drops by evaluating different power pad configurations. Therefore, such power pad configurations must be generated. To explore the relationship between performance and CPU time, we randomly generated $10^1 \sim 10^6$ power pad configurations. The CPU time includes the floorplanning and PPA time. In terms of performance, as shown in Figure 10(a), the maximum voltage drop generally decreases as the number of power pad configurations increases. However, Figure 10(b) indicates that the CPU time grows quickly as configurations increase. To balance performance and CPU time, we select 10^4 pad configurations to record results.

The comparison results are shown in Table IV. Because we generate the same floorplans and VIs, the wirelengths of all benchmark circuits are the same. For multiple pads for a VI, the floorplan will be partitioned into required parts based on power density and physical locations, and then required number of power pads are generated (Section 4.3). In terms of maximum voltage drop, our method results in 16.9% improvement versus [30], but obtains 14% extra voltage drops compared with the basic algorithm. However, because of the computational complexity of both the basic algorithm and [30], our approach is much faster than both. The basic algorithm exhausts all possible combinations of power pads to find the one with the minimum voltage drop, while [30] has to generate a sufficient

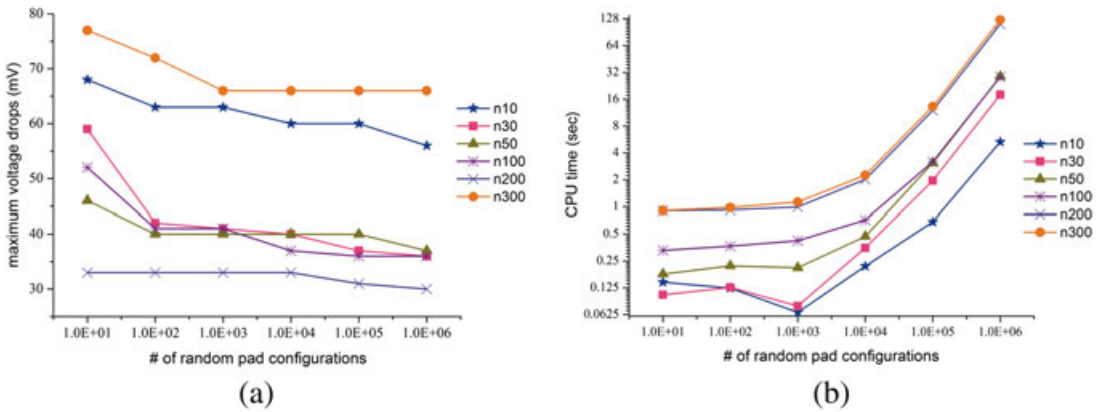

Figure 10. The comparison results: (a) maximum voltage drops; (b) CPU time.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

Table IV. Experimental results on multiple pads.

Circuit	maxD (mV)			#vio			Time			WL	# of total power pads
	Basic	[30]	Ours	Basic	[30]	Ours	Basic	[30]	Ours		
n10	36	60	52	0/227	0/214	0/214	7m22s	0.218 s	0.039 s	14 823	4
n30	32	40	34	0/263	0/198	0/215	98m17s	0.350 s	0.083 s	41 407	6
n50	31	40	35	0/231	0/215	0/267	54m32s	0.470 s	0.126 s	73 482	5
n100	29	37	36	0/261	0/235	0/252	18m15s	0.716 s	0.175 s	143 903	5
n200	27	33	31	0/217	0/244	0/256	90m41s	2.018 s	0.465 s	288 214	6
n300	48	66	48	0/435	0/375	0/405	111m44s	2.256 s	0.504 s	465 742	5
Avg	0.860	1.169	1.000					4.330	1.000		

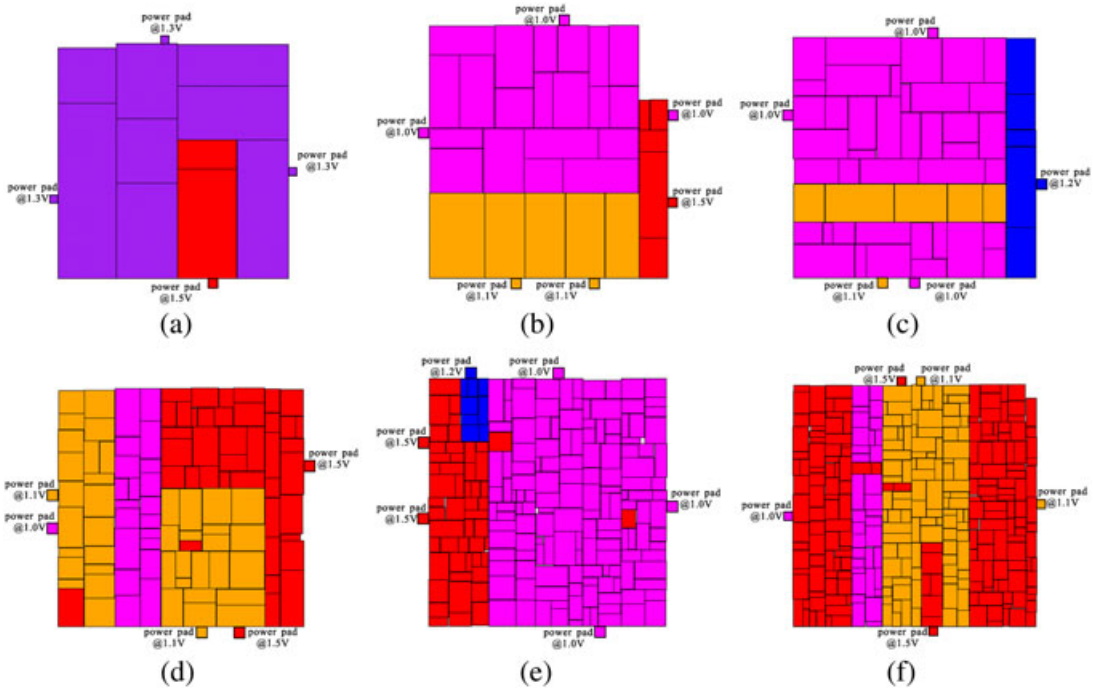

Figure 11. The floorplan results: (a) n10; (b) n30; (c) n50; (d) n100; (e) n200; (f) n300.

number of power pad configurations during one iteration. Therefore, it is believed that the basic algorithm and the method in [30] are unsuitable to be used during floorplanning. The floorplan and power pad results of circuits n10, n30, n50, n100, n200, and n300 are shown in Figure 11, in which the VIs and corresponding power pads are identified by different colors.

7. CONCLUSIONS

In this paper, a voltage drops aware power pad and floorplan method is proposed for multi-voltage SoC designs. Unlike conventional approaches without considering PPA during floorplanning, this work addresses the problem by combining PPA into floorplaning framework to find a globally optimal placement of power pads and blocks. To make our work computationally affordable, the core part of this work is the proposed spring-based fast and accurate PPA method. In particular, we also propose a new cost function to optimize both the total wirelength and the total weighted distance from power pads to blocks. Experimental results show that the proposed approach can achieve better P/G network performance and optimized placement of power pads and blocks.

Copyright © 2015 John Wiley & Sons, Ltd.

DOI: 10.1002/cta

ACKNOWLEDGEMENTS

This work was supported by the National Natural Science Foundation of China under Grant Nos. 61131001, 61501268, and 61571248, Zhejiang Provincial Natural Science Foundation under Grant No. LQ15F040001, Ningbo City Natural Science Foundation under Grant No. 2015A610112, and K.C. Wong Magna Fund in Ningbo University.

REFERENCES

1. Lackey DE, Zuchowski PS, Bednar TR, Stout DW, Gould SW, Cohn JM. Managing power and performance for system-on-chip designs using voltage islands. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2002; 195–202. DOI: 10.1109/ICCAD.2002.1167534
2. Wu H, Liu IM, Wong MDF, Wang Y. Post-placement voltage island generation under performance requirement. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2005; 309–316. DOI: 10.1109/ICCAD.2005.1560085
3. Lee WP, Liu HY, Chang YW. Voltage island aware floorplanning for power and timing optimization. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2006; 389–394. DOI: 10.1109/ICCAD.2006.320063
4. Zhou Q, Shi J, Liu B, Cai Y. Floorplanning considering IR drop in multiple supply voltages island designs. *IEEE Transactions On Very Large Scale Integration (VLSI) Systems* 2011; **19**(4):638–646. doi:10.1109/TVLSI.2009.2037428.
5. Singh J, Sapatnekar SS. Congestion-aware topology optimization of structured power/ground networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2005; **24**(5):683–695. doi:10.1109/tcad.2005.846369.
6. Mitsuhashi T, Kuh ES. Power and ground network topology optimization for cell based VLSIs. In Proceedings of ACM/IEEE Design Automation Conference, 1992;524–529. DOI: 10.1109/DAC.1992.227748
7. Singh J, Sapatnekar SS. Topology optimization of structured power/ground networks. In Proceedings of International Symposium on Physical design, 2004;116–123. DOI: 10.1145/981066.981093
8. Wang T-Y, Chen C-P. Optimization of the power/ground network wire-sizing and spacing based on sequential network simplex algorithm. In Proceedings of International Symposium on Quality Electronic Design, 2002;157–162. DOI: 10.1109/ISQED.2002.996721
9. Tan S-D, Shi C-J. Efficient very large scale integration power/ground network sizing based on equivalent circuit modeling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2003; **22**(3):277–284. doi:10.1109/TCAD.2002.807883.
10. Tan SX-D, Shi C-JR, Lee J-C. Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2003; **22**(12):1678–1684. doi:10.1109/TCAD.2003.819429.
11. Su H, Gala KH, Sapatnekar SS. Analysis and optimization of structured power/ground networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2003; **22**(11):1533–1544. doi:10.1109/TCAD.2003.818372.
12. Zhao S, Roy K, Koh C-K. Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2002; **21**(1):81–92. doi:10.1109/43.974140.
13. Fischer T, Desai J, Doyle B, Naffziger S, Patella B. A 90-nm variable frequency clock system for a power-managed itanium architecture processor. *IEEE Journal of Solid-State Circuits* 2006; **41**(1):218–228. doi:10.1109/JSSC.2005.859879.
14. Zhang L, Zhang Y, Jiang Y, Shi CJR. Symmetry-aware placement algorithm using transitive closure graph representation for analog integrated circuits. *International Journal of Circuit Theory And Applications* 2010; **38**(3):221–241. doi:10.1002/cta.551.
15. Zhang L, Raut R, Jiang Y, Kleine U, Kim Y. A hybrid evolutionary analogue module placement algorithm for integrated circuit layout designs. *International Journal of Circuit Theory And Applications* 2005; **33**(6):487–501. doi:10.1002/cta.332.
16. Hoo C-S, Jeevan K, Ramiah H. Cost reduction in bottom-up hierarchical-based VLSI floorplanning designs. *International Journal of Circuit Theory And Applications* 2015; **43**(3):286–306. doi:10.1002/cta.1939.
17. Anand S, Saravanasankar S, Subbaraj P. A multiobjective optimization tool for Very Large Scale Integrated nonslicing floorplanning. *International Journal of Circuit Theory And Applications* 2013; **41**(9):904–923. doi:10.1002/cta.829.
18. Martins R, Lourenço N, Canelas A, Horta N. Electromigration-aware analog Router with multilayer multiport terminal structures. *Integration, the VLSI Journal* 2014; **47**(4):532–547. doi:10.1016/j.vlsi.2014.02.003.
19. Yan J-T, Chen Z-W. Obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance. In Proceedings ofDesign, Automation & Test in Europe Conference & Exhibition (DATE), 2011;1–6.
20. Yim J-S, Bae S-O, Kyung C-M. Floorplan-based planning methodology for power and clock distribution in ASICs. In Proceedings of ACM/IEEE Design Automation Conference, 1999; 766–771. DOI: 10.1109/DAC.1999.782120
21. Dharchoudhury A, Panda R, Blaauw D, Vaidyanathan R, Tutuianu B, Bearden D. Design and analysis of power distribution networks in PowerPC microprocessors. In Proceedings of ACM/IEEE Design Automation Conference, 1998;738–743.

Copyright © 2015 John Wiley & Sons, Ltd.

22. Zhu QK. *Power Distribution Network Design for VLSI*. Wiley-Interscience: New York, 2004.
23. Haghdad K, Anis M. Power supply pads assignment for maximum timing yield. *IEEE Transactions on Circuits and Systems II: Express Briefs* 2011; **58**(10):697–701. doi:10.1109/TCSII.2011.2164143.
24. Chen H, Cheng C-K, Kahng AB, Wang Q, Mori M. Optimal planning for mesh-based power distribution. In Proceedings of Asia and South Pacific Design Automation Conference, 2004;444–449. DOI: 10.1109/ASPDAC.2004.1337616
25. Singh J, Sapatnekar SS. A fast algorithm for power grid design. In Proceedings of the International Symposium on Physical Design 2005; 70–77. DOI: 10.1145/1055137.1055153
26. Wang K, Marek-Sadowska M. On-chip power-supply network optimization using multigrid-based technique. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2005; **24**(3):407–417. doi:10.1109/TCAD.2004.842802.
27. Wang K, Meyer BH, Zhang R, Stan M, Skadron K. Walking pads: managing C4 placement for transient voltage noise minimization. In Proceedings of ACM/EDAC/IEEE Design Automation Conference, 2014;1–6. DOI: 10.1145/2593069.2593243
28. Zhong Y, Wong MD. Fast placement optimization of power supply pads. In Proceedings of Asia and South Pacific Design Automation Conference, 2007;763–767. DOI: 10.1109/ASPDAC.2007.358081
29. Sato T, Hashimoto M, Onodera H. Successive pad assignment algorithm to optimize number and location of power supply pad using incremental matrix inversion. In Proceedings of Asia and South Pacific Design Automation Conference, 2005;723–728. DOI: 10.1109/ASPDAC.2005.1466443
30. Dubey A. P/G pad placement optimization: problem formulation for best IR drop. In Proceedings of International Symposium on Quality of Electronic Design, 2005;340–345. DOI: 10.1109/ISQED.2005.89
31. Zhao M, Fu Y, Zolotov V, Sundareswaran S, Panda R. Optimal placement of power-supply pads and pins. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2006; **25**(1):144–154. doi:10.1109/TCAD.2005.852459.
32. Lee CJ, Liu SSY, Huang CC, Chen HM, Lin CT, Lee CH. Hierarchical power network synthesis for multiple power domain designs. In Proceedings of International Symposium on Quality Electronic Design, 2012;477–482. DOI: 10.1109/ISQED.2012.6187536
33. Ma Q, Young EFY. Multivoltage floorplan design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2010; **29**(4):607–617. doi:10.1109/TCAD.2010.2042895.
34. Lin JM, Hung ZX. SKB-tree: a fixed-outline driven representation for modern floorplanning problems. *IEEE Transactions On Very Large Scale Integration (VLSI) Systems* 2012; **20**(3):473–484. doi:10.1109/TVLSI.2011.2104983.
35. Köse S, Friedman EG. Efficient algorithms for fast IR drop analysis exploiting locality. *Integration, the VLSI Journal* 2012; **45**(2):149–161. doi:10.1016/j.vlsi.2011.09.003.
36. Rius J. IR-drop in on-chip power distribution networks of ICs with nonuniform power consumption. *IEEE Transactions On Very Large Scale Integration (VLSI) Systems* 2013; **21**(3):512–522. doi:10.1109/tvlsi.2012.2188918.
37. Chu Z, Xia Y, Wang L, Wang J. Voltage drop aware power pad assignment and floorplanning for multi-voltage soc designs. In Proceedings of International Conference on Computer-Aided Design and Computer Graphics, 2013; 87–94. DOI: 10.1109/CADGraphics.2013.19
38. Chung-Wen H, Ruehli A, Brennan P. The modified nodal approach to network analysis. *IEEE Transactions on Circuits and Systems* 1975; **22**(6):504–509. doi:10.1109/tcs.1975.1084079.
39. Cai Y, Liu B, Shi J, Zhou Q, Hong X. Power delivery aware floorplanning for voltage island designs. In Proceedings of International Symposium on Quality Electronic Design, 2007;350–355. DOI: 10.1109/ISQED.2007.121
40. Chi J-C, Huang TH, Chi MC. An IR drop-driven placer for standard cells in a SOC design. In Proceedings of IEEE International SOC Conference, 2005;29–32. DOI: 10.1109/SOCC.2005.1554448
41. Wu S-W, Chang Y-W. Efficient power/ground network analysis for power integrity-driven design methodology. In Proceedings of ACM/IEEE Design Automation Conference, 2004;177–180.DOI: 10.1145/996566.996617
42. Kahng AB, Liu B, Wang Q. Supply voltage degradation aware analytical placement. In Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2005;437–443. DOI: 10.1109/ICCD.2005.101
43. Liu C-W, Chang Y-W. Power/ground network and floorplan cosynthesis for fast design convergence. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2007; **26**(4):693–704. doi:10.1109/TCAD.2007.892336.
44. Chuang YL, Lee PW, Chang YW. Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2011; **30**(11):1649–1662. doi:10.1109/TCAD.2011.2163071.
45. Padmawar M, Roy S, Chakraborty K. Integrated circuit-architectural framework for PSN aware floorplanning in microprocessors. In Proceedings of International Symposium on Quality Electronic Design, 2011;1–7. DOI: 10.1109/ISQED.2011.5770727
46. Hauck S, Borriello G. Pin assignment for multi-FPGA systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 1997; **16**(9):956–964. doi:10.1109/43.658564.
47. Chiprout E. Fast flip-chip power grid analysis via locality and grid shells. In Proceedings of IEEE/ACM International Conference on *Computer-Aided Design*, 2004;485–488. DOI: 10.1109/ICCAD.2004.1382626
48. Hartigan JA, Wong MA. Algorithm AS 136: a k-means clustering algorithm. *Applied Statistics* 1979; **28**(1):100–108.
49. Nie F, Xu D, Li X. Initialization independent clustering with actively self-training method. *IEEE Transactions on Systems, Man, and Cybernetics. Part B, Cybernetics* 2012; **42**(1):17–27. doi:10.1109/TSMCB.2011.2161607.

Copyright © 2015 John Wiley & Sons, Ltd.

50. He O, Dong S, Bian J, Goto S, Cheng C-K. A novel fixed-outline floorplanner with zero deadspace for hierarchical design. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, 2008;16–23. DOI: 10.1109/ICCAD.2008.4681546
51. Chen S, Yoshimura T. Fixed-outline floorplanning: enumerating block positions and a new objective function for calculating area costs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2008; **27**(5):858–871. doi:10.1109/TCAD.2008.917968.
52. Chen T-C, Chang Y-W. Modern floorplanning based on B*-tree and fast simulated annealing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2006; **25**(4):637–650. doi:10.1109/TCAD.2006.870076.
53. Roy JA, Adya SN, Papa DA, Markov IL. Min-cut floorplacement. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2006; **25**(7):1313–1326. doi:10.1109/TCAD.2005.855969.
54. Adya SN, Markov IL. Fixed-outline floorplanning: enabling hierarchical design. *IEEE Transactions On Very Large Scale Integration (VLSI) Systems* 2003; **11**(6):1120–1135. doi:10.1109/TVLSI.2003.817546.
55. Yan JZ, Chu C. DeFer: deferred decision making enabled fixed-outline floorplanning algorithm. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2010; **29**(3):367–381. doi:10.1109/tcad.2010.2041850.
56. Chu Z, Xia Y, Wang L, Wang J. Efficient nonrectangular shaped voltage island aware floorplanning with nonrandomized searching engine. *Microelectronics Journal* 2014; **45**(4):382–393. doi:10.1016/j.mejo.2014.01.006.
57. Haghdad K, Jaffari J, Anis M. Power grid analysis and verification considering temperature variations. *Microelectronics Journal* 2012; **43**(3):189–197. doi:10.1016/j.mejo.2011.12.008.
58. Haghdad K, Anis M, Ismail Y. Floorplanning for low power IC design considering temperature variations. *Microelectronics Journal* 2011; **42**(1):89–95. doi:10.1016/j.mejo.2010.08.022.

Copyright © 2015 John Wiley & Sons, Ltd.