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## **Integrated DWDM Silicon Photonic Transceiver with Self-Adaptive CMOS Circuits for Chip-to-Chip Optical Interconnects**

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Abstract: (250-word limit)

The rapid scaling of microprocessors has shifted the critical bottleneck of high-performance computing systems from the computational units to the communication infrastructure. By taking advantage of the parallelism and capacity of dense wavelength-division-multiplexed (DWDM) technology, optical interconnects using nanophotonics offer a high-bandwidth, low-latency, and energy-efficient solution within a small footprint, when compared with their electrical counterparts.

In this paper, we report our progress on developing a silicon photonic transceiver with hybrid photonic/electronics integration, incorporating CMOS circuits with a photonics substrate to form a DWDM optical link targeting high-performance computing applications. We have demonstrated a transmitter incorporating wire-bonded pre-emphasis drivers and carrier-injection-based microring modulators operating at 5 Gbps, for an energy-efficiency of 808 fJ/bit. Both thermal and bias-tuning schemes are utilized to lock the resonance of the microrings to the input channel wavelengths and compensate for environmental fluctuations. Integrated silicon resistive heaters show a tuning efficiency of 11  $\mu\text{W}/\text{GHz}$  for 5  $\mu\text{m}$  microrings, while bias-tuned feedback compensation demonstrates a maximum wavelength tuning of 0.22 nm at 425  $\mu\text{W}$  power consumption. We also demonstrated a self-adaptive receiver, with an energy efficiency of 275 fJ/bit at 8 Gbps, which reduces the transimpedance amplifier (TIA) power by 14% when the input sensitivity is relaxed by 2 dB.

These components will be brought together into a 16-channel DWDM system by flip-chip bonding a CMOS transceiver chip onto a photonic chip with microring modulators and waveguide germanium photodiodes. The channel grid will be provided by an external quantum-dot-based comb laser at wavelengths near 1.3 $\mu\text{m}$  with 80 GHz channel spacing.