Component-Level Electronic-Assembly Repair (CLEAR) Operational Concept

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Summary

This "Component-Level Electronic-Assembly Repair (CLEAR) Operational Concept" document was developed as a first step in developing the Component-Level Electronic-Assembly Repair (CLEAR) System Architecture (NASA/TM—2011-216956). The CLEAR operational concept defines how the system will be used by the Constellation Program and what needs it meets. The document creates scenarios for major elements of the CLEAR architecture. These scenarios are generic enough to apply to near-Earth, Moon, and Mars missions. The CLEAR operational concept involves basic assumptions about the overall program architecture and interactions with the CLEAR system architecture. The assumptions include spacecraft and operational constraints for near-Earth orbit, Moon, and Mars missions. This document addresses an incremental development strategy where capabilities evolve over time, but it is structured to prevent obsolescence.

The approach minimizes flight hardware by exploiting Internet-like telecommunications that enables CLEAR capabilities to remain on Earth and to be uplinked as needed. To minimize crew time and operational cost, CLEAR exploits offline development and validation to support online teleoperations. Operational concept scenarios are developed for diagnostics, repair, and functional test operations. Many of the supporting functions defined in these operational scenarios are further defined as technologies in NASA/TM—2011-216956.

Contents

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1.0   Introduction

The Component-Level Electronic-Assembly Repair (CLEAR) task is part of the NASA Exploration Technology Development Program (ETDP) Supportability Project. CLEAR's objective is to develop technologies to enable space-flight crews to perform in situ repairs of electronic hardware at the component level (Ref. 1). This document, which is one of many documents produced by the CLEAR task (see Section 2.0), describes an overall operational concept on how to perform component-level repair of electronics within a spacecraft or habitat. The operational concept identifies the capabilities, activities, sequences, and resources, including facilities, software, and staffing. This document sets the top-level objectives and functional requirements for the proposed component-level repair architecture.

The CLEAR task responds to the general need to reduce the upmass of spare hardware and to empower the space-flight crew to respond to problems without depending on a robust and timely logistics system. The CLEAR task has chosen to enable component-level repair of electronics without expanding crew size or dramatically expanding flight crew training. This task has adopted a strategy to exploit teleoperations as a means of augmenting the flight crew with ground-based support on an as-needed basis. Previous documents (Refs. 1 and 2) describe this strategy. The appendix defines the acronyms and abbreviations used in this document.

2.0 Documents

The following documents contain supplemental information related to the CLEAR task.

2.1 Reference Documents

Document number	Document title
CLEAR–DOC–005	Component-Level Electronic-Assembly Repair (CLEAR) Analysis of the Problem Reporting and Corrective Action (PRACA) Database of the International Space Station On-Orbit Electrical Systems
CLEAR–DOC–006	Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs
CLEAR–DOC–008	Component-Level Electronic-Assembly Repair (CLEAR) System Architecture

2.2 Applicable Documents

Document number	Document title
CLEAR–ANA–001	Component-Level Electronic-Assembly Repair (CLEAR) Life-Cycle Cost Impacts of Different Approaches for In Situ Maintenance of Electronics Hardware
CLEAR–ANA–002	Component-Level Electronic-Assembly Repair (CLEAR) Noncontact Coupling Techniques for Performing Signature Analysis
CLEAR–DOC–001	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) Flight System Requirements Document
CLEAR–DOC–002	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) Concept and Hardware Summary
CLEAR–DOC–003	Component-Level Electronic-Assembly Repair (CLEAR) Recommendations for the Design of Electronic Assemblies for NASA's Exploration Program
CLEAR–DOC–004	Component-Level Electronic-Assembly Repair (CLEAR) Trade Study: Current Technologies and Instruments for Electronic Fault Diagnosis and Repair
CLEAR–DOC–005	Component-Level Electronic-Assembly Repair (CLEAR) Analysis of the Problem Reporting and Corrective Action (PRACA) Database of the International Space Station On-Orbit Electrical Systems
CLEAR–DOC–006	Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs
CLEAR–DOC–008	Component-Level Electronic-Assembly Repair (CLEAR) System Architecture
CLEAR–DOC–009	Component-Level Electronic-Assembly Repair (CLEAR) Recommendations for Enabling Manual Component-Level Electronic Repair for Future Space Missions
CLEAR–RPT–001	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) System Requirements Review (SRR) Panel Report
CLEAR–RPT–002	Component-Level Electronic-Assembly Repair (CLEAR) Soldering in Reduced Gravity Experiment (SoRGE) Mission Test Report
CLEAR–RPT–003	Component-Level Electronic-Assembly Repair (CLEAR) Spacecraft Circuit Diagnostics by Analog and Complex Signature Analysis
CLEAR–RPT–004	Component-Level Electronic-Assembly Repair (CLEAR) Synthetic Instrument Capabilities Assessment and Test Report

3.0   Background

The International Space Station (ISS) is providing the United States with the first major experience with a permanent orbiting facility that requires on-orbit servicing. The ISS program recognized in early studies that servicing systems could become the predominant activity of flight crews instead of their intended scientific missions (Ref. 3). Thus, the design of ISS involved modularized hardware that could be replaced quickly and easily at the box level by crewmembers or robotics. These modules, or orbital replaceable units (ORUs), can be swapped out and returned to Earth for servicing without extensive on-orbit crew involvement. The penalty for this approach is the need to transport new replacement spares to space and return faulty ORUs to Earth for rework and eventual return to space. The economics of this approach depends on a robust, readily available, and low-cost space transportation system.

Since the *Space Shuttle Columbia* accident, it has become evident that the Space Transportation System (STS) cannot provide the availability that was envisioned, and persistent flight safety problems have resulted in NASA plans to halt STS flights in 2010. Although a new crew exploration vehicle, *Orion*, will be coming on line in a few years, it is not a cargo vehicle. International partners and commercial sectors have or are developing cargo vehicles that will allow some upmass capability to ISS; however, virtually no downmass will be available once the STS flights stop. The Exploration Program faces similar, but increasing, logistic challenges as crews move further from Earth.

A solution to this dramatically reduced logistic support is to provide in situ repair capability at the component level. The mass of individual electronic components is a small fraction of that of a complete electronic ORU. Typically, the metal enclosure is the greatest single mass component of an electronic ORU for the space environment. In some instances, the enclosure may represent 60 percent of the ORU weight. In contrast, the mass fraction of a single electronic component will usually range from one-hundredth to one-thousandth of the weight of the total ORU. Component-level replacement is a logistically attractive option in comparison to the processing and relaunch costs related to ORU replacement, particularly, if one considers that a faulty electronic ORU is composed primarily of good components.

The ability to replace parts at the component level must be flanked by the ability to accurately diagnose and isolate a problem prior to the repair and to functionally test after the repair. In addition to the crew time required to repair the ORU, time is required for the diagnostic evaluations needed to isolate the faulty component and for postrepair functional tests to assure that the repair is successful and the unit is safe to return to the system.

A maintenance strategy for space electronics must take measures to limit the impact on crew time, which was why the ORU strategy was adopted. Like payload upmass, crew time is a limited resource that should be reserved to accomplish the intended mission.

The Constellation Program (CxP) is developing a new set of vehicles suited for a much broader range of missions. *Orion* can support low-Earth-orbit missions and lunar missions with some extensibility to Mars. The Apollo-like *Orion* is very compact and has very few in-flight servicing options as an independent vehicle. In its early missions, *Orion* will dock with the ISS as part of its crew transportation role. The berthing of *Orion* will let ISS serve as a possible on-orbit repair depot.

The Lunar Surface Systems and the Lunar Lander (Altair), which are currently in the definition phase, will have much different logistics requirements. Missions will be optimized to return only the crews and 100 kg of lunar samples. There will be virtually no accommodations for returning faulty hardware. The constraints on lunar missions are driving the lunar architecture toward greater independence, with in situ capabilities and less dependence on external logistics.

4.0 Assumptions

4.1 Near-Earth Mission Assumptions

The following near-Earth mission assumptions were adopted for this operational concept:

- Crew transportation to the ISS will be one of *Orion*'s primary missions.
- In situ repairs onboard *Orion*, as an independent vehicle, will be limited to emergency repairs.
- ISS will be outfitted to provide a limited electronics repair depot for *Orion*.
- A repair capability on ISS could also provide repair for ISS needs.

4.2 Lunar Mission Assumptions

The following lunar mission assumptions were adopted for this operational concept:

- Repairs in transit between the Earth and Moon will be extremely rare and used only for emergencies.
- On the lunar surface, a lunar lander may have additional spares and repair capability, but repairs will not be routine.
- For the lunar surface systems, the Lunar Habitat or Lunar Outpost will serve as a long-term or permanent facility where the hardware will be stressed and experience high levels of wear and tear as part of exploration and surface operations. Thus, maintenance and repair will be part of normal operations.
- All hardware delivery will be one way. No hardware will be returned to Earth for servicing.
- Faulty or damaged hardware will be replaced with logistics spares when available. Repairs will be performed in situ if no spares are available.
- When the capability exists, faulty units removed from a system will be repaired at the intermediate and component level to return the hardware to serviceable condition and then placed in spare inventory.
- After performing their initial purpose, spent flight systems that are serviceable may be scavenged at the system, ORU, and shop replaceable unit (SRU) levels (recovered, reconfigured, and reused).
- ORU- and SRU-level hardware that is not considered to be repairable will be scavenged for good components.

Recovery and reconfiguration of electronics, including scavenging components, would dramatically extend the useful life and value of electronics that would otherwise be discarded. These reworked packages could begin to build the needed lunar infrastructure, including power, communications, and in situ resource utilization.

4.3 Mars Mission Assumptions

The following Mars mission assumptions were adopted for this operational concept:

- For Mars missions, the capability to perform in situ repair in flight will be enabling.
- The extreme distances and mission duration will negate the abort-to-Earth option as an effective response to major system failures.

- There will be no effective rescue mission capability for timely recovery of the Mars crew or vehicle.
- There will be no external logistics supply beyond onboard provisions and potential prepositioned facilities.
- During Mars missions, the crew will have to scavenge components and fabricate solutions from materials and resources available.

The innate complexity of a Mars vehicle, the very long mission, and exposure to uncertain environments pose a high risk of a damage or system failure and extreme consequences. Flight crews will need to achieve an unprecedented level of resource independence and to be able to effectively respond to any problem and exploit any opportunity. For Mars missions, the crew should be able to fabricate solutions exploiting any available resource including constructing hardware from in situ materials and scavenged flight hardware.

4.4   Launch and Environment Constraints

Spacecraft payload is limited primarily by the physical mass and volume. The launch vehicle applies 3g to 5g acceleration loads during ascent. Furthermore, launch also applies shock, dynamic vibration, and acoustic loading that can be very destructive. Hardening the design for dynamic loading adds mass.

A typical ORU spare has many internal interfaces between the subassemblies and components that are sensitive to the dynamic loads of launch and that must remain intact and fully functional when delivered. The packaging and mounting hardware required to assure safe delivery of an ORU to orbit compound the initial launch mass.

Power and thermal dissipation in a vacuum environment have an impact on mass properties. They drive the design of the enclosure because of thermal dissipation needs that, in turn, drive package mass both at the circuit card level and the ORU chassis level. Vacuum-rated electronics rely on heat conduction to dissipate heat. In many ORUs, the enclosure is pressurized to enhance heat transfer and mitigate the effects of outgas and off-gas processes. This, in turn, drives up the wall thickness and weight of the enclosure. At the circuit-card level, conductive heat transfer is usually achieved by adding extra thick conductive laminations or adding metal plates directly to the circuit.

The weight breakdown of an actual ISS ORU is illustrated in Figure 1. The ORU enclosure must handle all the combined heat loads as well as structural loads and, thus, is the heaviest component. Internal power supplies are the main source of heat, and they tend to be the heaviest subassembly. Circuit-card assemblies (CCAs) are a smaller fraction, but the weight penalty for conductive power dissipation and structural stiffening results in a mass that may be double that of an equivalent air-cooled commercial off-the-shelf circuit card.

In comparison, individual electronic components such as discrete devices and integrated circuits are monolithic. That is, they are a simple single mass with few interfaces. Small electronic components often weigh a few grams and require little more than a padded envelope and loose stowage. The mass of an individual component often represents only one-hundredth to one-thousandth of the weight of the ORU. In other words, component-level replacement eliminates the complexity and weight penalties associated with safely launching a fully integrated ORU. This frees up payload capacity for the primary mission payloads.
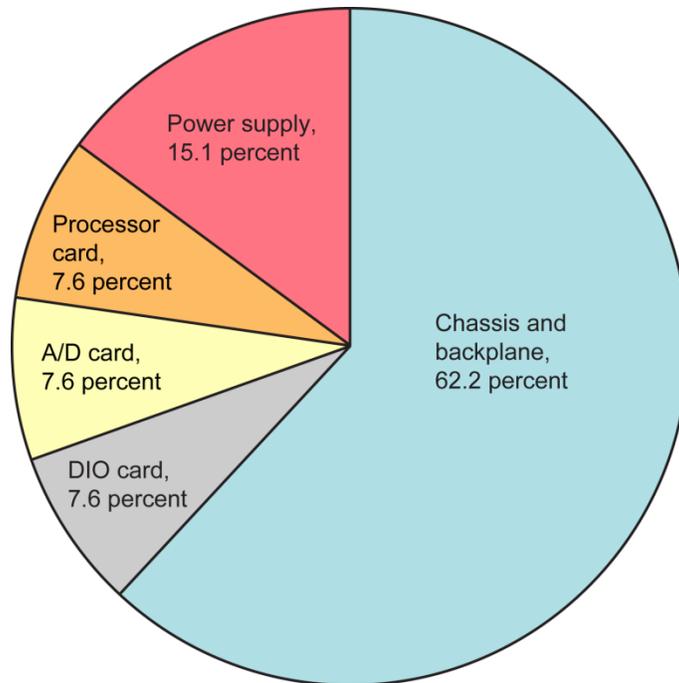
Figure 1.—Mass and volume breakdown of a typical orbital replacement unit (ORU); from "Component-Level Electronic-Assembly Repair (CLEAR) Life-Cycle Cost Impacts of Different Approaches for In Situ Maintenance of Electronics Hardware" (CLEAR–ANA–001). A/D, analog to digital; DIO, digital input/output.

4.5   Crew Constraints

Like payload capacity, flight crew time is a valuable and constrained resource. There are many aspects of flight and preflight training that compete for the crew's attention. Repair and related diagnostic and test activity require a skill set beyond normal flight crew training. Crew members are exposed to rudimentary repair training and cannot be considered to be skilled technicians. Repair, particularly soldering, requires innate dexterity and eye-hand coordination that can only be acquired through practice. Furthermore, these skills require practice in order to maintain proficiency.

Training flight crews as technicians consumes a resource that was originally intended to support mission objectives. As noted earlier, the ORU logistics strategy was intended to reduce the demands on crew availability. Component-level repair must not significantly diminish the time efficiency provided by ORU design. Therefore, manual repair operations need to be limited to tasks for which manual methods provide the best results.

Most producers, even for low-volume production, rely on automated equipment in fabrication. Generally, a repair or rework process will provide good quality results if it employs the setup and process parameters used in production. The secondary benefit of automation is the dramatic reduction of the crew time required to perform component replacements.

Automation depends on prior setup, programming, and tuning of the process. Tuning requires a number of test executions. CLEAR will avoid tying up crew time by doing these tasks remotely through ground-based engineering. The need for remote access and feedback implies significant teleoperations support for certain phases. This is defined in more detail in a later section.

4.6   Command, Control, Communications, and Information Constraints

Command, control, communications, and information (C3I) is the telecommunications infrastructure that supports spacecraft and payloads. The technology developed by CLEAR is expected to be applied first on ISS, but its intended role will be for lunar operations and beyond. The teleoperational environment is expected to evolve over this development lifespan.

The NASA CxP is planning to evolve the communications infrastructure from its present configuration to a more Internet-like network (Ref. 4). The C3I infrastructure will become more flexible and use strategies that will provide greater utilization of bandwidth and greater resistance to signal interruptions.

For near-Earth applications, interruption (or loss-of-signal) events are quite frequent because of the problem of tracking a spacecraft at a low altitude and the 90-min orbit. Lunar operations will be affected by the signal delay. There is considerable uncertainty regarding the communication data rates for lunar operations.

Because they are occasional operations, repairs are likely to operate like many current ISS payloads (i.e., with a high degree of teleoperations) both in low Earth orbit and on the Moon. This will allow for the utilization of communications channels provided for science payloads which simplify development and avoid the need for dedicated secure links.

5.0   Incremental System Development

The CLEAR task recommends an incremental approach to developing the technology and in situ repair capability for NASA. This section describes objectives, rationale, advantages, and architecture needs that warrant incremental development. The CLEAR task proposes that an in situ repair capability be developed as a series of technology packages for ground testing and/or flight aboard ISS, but this capability will ultimately be extensible to lunar applications.

5.1   CLEAR Task Development Objectives

With the assumptions just described, the CLEAR task established the following objectives as requirements for its architecture:

(1) A capability to diagnose an electronics assembly and identify the faulty component(s) with equipment that fits within the mass-volume constraints of spacecraft
(2) A capability to repair electronics in situ with processes and materials that are safe and compatible with a spacecraft environment
(3) A capability to evaluate the repaired circuit as safe to return to service
(4) A capability to equip the flight crew with knowledge and skills to diagnose faults and perform repairs without expanding crew size

5.2   NASA System Engineering Approach

The CLEAR task is part of a technology development program. However, it also represents a permanent capability that will impact the overall life-cycle cost of CxP.

The task will approach the problem of electronics repair as a complete operational system rather than as isolated repair capabilities. Therefore, electronics repair will generally comprise initial diagnostic activities, physical repair, and postrepair functional tests.

CLEAR has adopted the system engineering approach outlined in the NASA System Engineering Handbook (Ref. 5). The CLEAR task is a relatively small part of the overall program, but CLEAR intends to employ the practices outlined in the handbook.

5.3   Incremental Development Approach Rationale

The CLEAR task objectives imply providing a NASA depot-level capability squeezed into the constraints of a spacecraft in a remote environment with no direct precedence. There is an array of technologies and techniques to consider, and an innovative approach is needed to render them compact, lightweight, and compatible with space. Some requirements can be addressed by analysis and tradeoff studies. Innovative, but untested, techniques will require analysis, lab work, and low-gravity tests to validate them for space.

With no accurate way to predict which circuits will need repair, there is a tendency to cover every possible repair option. This would result in a project with huge development ramp-up and coordination costs, as well as a long requirements-definition phase and development contracts. Program managers will attempt to contain cost by pushing an aggressive schedule and selecting low-risk off-the-shelf technology. The resulting product could be a collection of technologies that is a poor match with the operational environment and poorly understood by its users. If users find it to be unwieldy, it will provide very limited utility.

Only operational experience will reveal the failures and the diagnostic, repair, and test needs. Experience also will provide the opportunity for an appropriate mix of crew, robotics, and teleoperations capabilities to evolve. Incremental development will accommodate the development of techniques with varied levels of complexity. It will allow the CLEAR task to capture "low-hanging fruit" with early flight

experience, such as manual soldering methods from Station Development Test Objectives (SDTOs) aboard ISS. More challenging and complex repair methods that involve automated or robotic solutions will have a longer time to evolve.

5.4   Advantages of Incremental Development

Incremental development has the following advantages:

- The project could scale activity to the current development budget, particularly if the initial budget did not fully appreciate the scope.
- Key technologies could be demonstrated, and lessons learned from actual flight experience could be accommodated.
- A series of successes would build program confidence and allow time for technology adoption.
- The flexibility to accommodate external program changes and shifting program objectives would be maintained.
- CxP would evaluate the effectiveness of repair technologies and adjust its logistic and supportability strategies.

5.5   Incremental Development System Architecture

5.5.1   Architecture Backbone

A system engineering approach that focuses on CxP objectives is needed to assure that the end product meets the program needs. Semiautomated repair, diagnostic operations, repair, and functional test will depend on ground support and teleoperations. These tasks will be more complex than simply building an isolated apparatus.

The overall CLEAR architecture is intended to be developed as a series of technology packages. The last package must be compatible with the first package. The initial flight package must include teleoperations and the data backbone architecture of the system. This requires that decisions for this data backbone must be made at an early stage of development.

Because of the long development cycle and the continuous advances in data system technology, CLEAR must anticipate obsolescence. Therefore, the CLEAR architecture must select technologies innately resistant to obsolescence to ensure long-term viability and minimize life-cycle cost.

CLEAR will employ two approaches to combat obsolescence:

(1) A local area network will be the data backbone of the system.
(2) An evolving technology called synthetic instrument (SI) will be exploited.

5.5.2   Development Within an Existing Operational Framework

As with ISS, CxP will have constraints for payload, crew time training, and C3I bandwidth. Therefore, teleoperations capability will be developed to fit within existing capabilities. To prevent adding operational burden to the program, the CLEAR task will use the telecommunications channels used to support payloads. This will prevent competition between CLEAR and flight operations for high-priority command and control channels. As described in Section 6.0, control of CLEAR hardware for diagnostic, repair, and test functions will be developed and validated offline.

5.5.3   Evolution of Electronics Technology

Despite the growth of electronics capability and integrated circuit density within the last three decades, there is real evidence that the pace of electronics technology advance has slowed. For example the Pentium microprocessor clock speeds went from 60 MHz when introduced in 1993 to 3.8 GHz in 2004—a 63-fold increase in speed. However, with processor thermal loads running over 100 W, the

processor speeds have barely advanced since then. The ever-decreasing feature size that drove integration levels and the operating clock speed growth has slowed dramatically. Devices with smaller feature size are much more susceptible to space radiation and thus require additional measures to assure reliable operations. Based on these patterns, the growth in the scale and performance of electronics will advance at a much slower pace in the next decade.

Electronics packaging will continue to advance, and packaging has a major impact on repair. For the foreseeable future, the ball grid array (BGA) and land grid array (LGA) will be the packages of choice for high-density electronics. Space systems commonly use hybrid packages composed of metal and ceramic materials. With their proven history of reliability, hybrid packages are very suited to the space environment. Furthermore, they are an economical way of constructing complex circuits in low production volume. We expect to see hybrid packaging continue to be used in the foreseeable future.

6.0 CLEAR Teleoperational Concept of Operation

6.1 Component-Level Electronics Repair Concept

This section is intended to define the general concept of operation to accomplish the repair goals. The CLEAR operational concept will be consistent with CxP operational concepts for near Earth, Moon, and Mars. The CLEAR operational concept has been used to define the CLEAR architecture in "Component-Level Electronic-Assembly Repair (CLEAR) System Architecture" (CLEAR–DOC–008).

For the CLEAR task, the repair process is composed of three primary activities: diagnostic operations, repair, and functional test (Figure 2). Although these activities may employ the same resources and equipment, they have distinctly different objectives and, in turn, drive different requirements.

(1) *Diagnostic Activities*.—"Diagnose" is from the Greek, meaning "to seek deeper or more perfect knowledge." Diagnosis involves examination, observing symptoms, and measuring fundamental parameters to, first, characterize the fault, and second, determine the root cause of a malfunction or fault. It may involve a passive circuit in a power-off condition or an active circuit in a power-on condition. Furthermore, there may be a series of probing measurements intended to locate a problem area followed by refined probing to isolate the problem. For diagnostic operations, the emphasis is on measurements that help isolate a specific cause among many possible causes.

(2) *Repair Activities*.—Repair is broadly defined as a physical replacement, rework, or remanufacture of a faulty or failed circuit element and restoring full function. Most often it involves replacement of faulty components or the rework of interconnecting hardware such as solder joints, connectors, or the underlying substrate. In most cases, a failed component is replaced. It is rare that the component itself is amenable to repair (e.g., transformers). Thus for clarity, the CLEAR task actually replaces parts at the component level.

(3) *Functional Test Activities*.—Functional test is intended to verify that a circuit functions properly in accordance with functional requirements for that system. Direct electrical measurements are made to determine if the unit is meeting its design specifications. Verifying function implies operating and observing the circuit as it performs its function in its operational environment. Functional testing often follows the assembly sequence where functional tests are performed at the lowest to the highest levels of assembly. Functional tests include built-in tests (BITs) for both software and hardware, physical parameter measurement, and recording observed behavior in nominal and off-nominal operations. Ultimately, a circuit must be tested as part of the actual system (or simulated system).

6.2 CLEAR Teleoperations Approach

Teleoperation refers to remote control of equipment or machinery through telecommunications links. For CLEAR, both the repair apparatus and the diagnostic and test instruments will be teleoperated. Depending on the needs, the equipment may or may not require human intervention. Generally, it is assumed that the ORU assembly will be broken down manually by the crew. This includes manual removal of ORU subassemblies, typically CCAs, and breaking the mechanical and electrical interconnections.

CLEAR equipment is intended to support diagnostics, component replacement, and functional testing. For semiautomated operations, the goal is to limit crew time consumption as much as possible. The bulk of the human activity will be performed by ground-based engineering crews working largely offline. The supporting crew may be formed from hardware vendors, system managers, integrators, and engineering and technical staff of NASA repair depots.
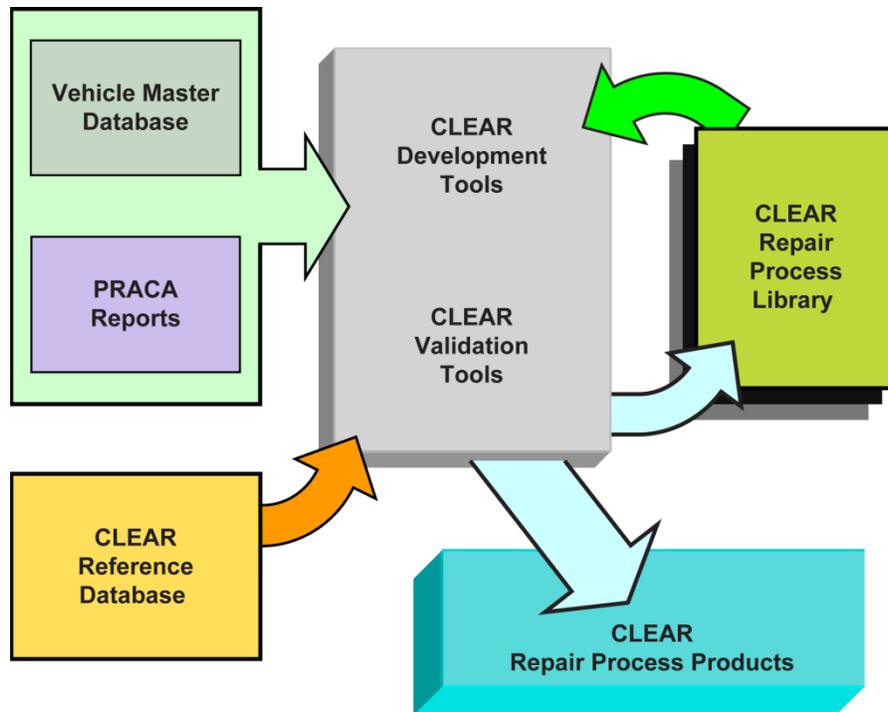
Figure 2.—CLEAR diagnostic, repair, and test application development. PRACA, Problem Reporting and Corrective Action.

Repair operations are expected to be infrequent; the cost of keeping a "standing army" of teleoperators on standby would defeat the benefits of teleoperations. The CLEAR task proposes that support teams be built on an as-needed basis similar to current ISS operations. Such a team, referred to here as the CLEAR Teleoperations Engineering Support Team (CLEAR TEST) will provide the following:

- Specific ORU hardware and software knowledge
- Diagnostic and test expertise
- Materials and process expertise
- CLEAR hardware programming, verification, and validation support
- Vehicle Master Database (VMDB) and CLEAR process library configuration management
- Hardware and spares tracking
- Coordination of flight crew operations
- Coordination of teleoperation and execution of CLEAR diagnostic, repair, and functional test operations

Many of these roles can be provided by existing staff currently performing flight operations, payload operations, and logistics. Such roles are performed today for the ISS by the Logistics and Maintenance group, the Operational Support Office, and the various repair depots that currently perform diagnostic, repair, and test activities for the ISS. The NASA Shuttle Logistics Depot and NASA Spacecraft Services Depot indicated that the majority of ORU repair activity is performed on units that were found to be faulty during ground processing prior to flight. The depots reported that only a fraction of the ORUs repaired are returned flight units that failed on orbit. Thus, the NASA depots also will have the most recent hands-on experience. In most cases, the original vendor will provide the most indepth understanding of the electronics ORU at the component level and, thus, will be needed to support the development of component-level repair processes.

The practice with high-volume consumer electronics is to discard faulty circuits (because the labor involved is simply too expensive relative to the value of the circuit) and simply replace them with new units. In contrast, space-flight circuits are very valuable and are produced in very low volume; therefore, component-level repairs on ORU circuits are practical. NASA depots employ both manual and semi-automated rework stations for removal and replacement of discrete components, complex integrated circuits (ICs), and hybrid circuits.

6.2.1 Orbital Replaceable Unit Design Database

Teleoperations for CLEAR will need to have access to a very complete design and test knowledge database. Because repair is highly dependent on the materials and processes used in fabrication, it is essential that the database contain detailed fabrication information. For printed circuit boards, the laminate material selection, laminate schedule, and thickness of conductor layers—along with other special features such as bonded thermal conduction plates, component staking, and conformal coatings— all impact the preparation and execution of a repair. Detailed process parameters, like a solder reflow heating profile, are essential to a successful repair.

A design drawing and document database is needed to provide the as-built configuration of the hardware and must be kept under configuration management. A study performed in January 2008 (and documented in the "Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs" (CLEAR–DOC–006) gathered detailed information found in the ISS VMDB. There was considerable variation in the completeness of the database from vendor to vendor. A VMDB has valuable information regarding fabrication, functional requirements, and test specifications, but it must be emphasized that it needs to be complete. Also, future design databases for CxP must make detailed materials and process information readily accessible to CLEAR TEST.

6.2.2 CLEAR Process Library

A complete design database is necessary, but not sufficient, to serve all the information needs for the CLEAR task. A distinctly new data library is also required.

Design databases may provide extensive information on acceptance test parameters and functional tests, but they do not generally contain information on specific repairs or diagnostic procedures and techniques. Diagnostic and repair procedures are usually generated on an as-needed basis. Because of in situ constraints and the unique environment, much of the diagnostic, repair, and test procedures will need to be developed from scratch. Repairs are commonly documented on Problem Reporting and Corrective Action (PRACA) reports. PRACA reports may be supported by multiple detailed failure analysis and problems studies. A CLEAR process library will need to be developed to augment the existing the PRACA system, specifically to store repair information composed of diagnostic routines, repair processes, materials, and functional test parameters and procedures.

6.2.3 CLEAR Offline Programming and Validation

CLEAR is expected to be teleoperations and software intensive for both diagnostic and repair operations. Each repair will have unique hardware and software setup needs. Planning and subsequent programming of robotic and instrument equipment must not consume limited crew time or tie up communications bandwidth. Ground-based engineers will conduct programming to set up equipment to minimize crew time. Therefore, CLEAR development tools also will be made available to engineers to develop diagnostic, repair, and test programs offline.

The resulting diagnostic and repair programs will become part of the CLEAR process library. Should a similar fault reappear, a great deal of effort will already have been captured. Over time, the number of team members required can shrink as the library grows and experience makes the team more effective.

Teleoperations must not operate with unverified programming. Although there would be little risk to the vehicle, unverified setup of the apparatus or test set would pose substantial risk to the repair target and

to the apparatus. There also would be some risk of crew injury should an errant program cause the apparatus to act destructively. Therefore, CLEAR validation tools need to be available to the support engineers to debug and validate processes and programs. These validation tools comprise both simulation tools and hardware test beds.

The CLEAR task will define the programming environment along with simulation and validation practices. Any program software required to perform any aspect of the repair process must first pass through a validation process on either a duplicate set of the actual flight hardware or an accurate simulator.

7.0 Operational Concept for CLEAR Diagnostic Operations

7.1 CLEAR Diagnostic Objectives

The fundamental problem with electronic diagnostics is that an electronic system is composed of many interdependent components that function as a whole. ISS faults have been within individual components that could be isolated if the system could be broken down to the component level. However, this implies dismantling an entire assembly, individually testing each component, and reassembling the assembly once the faulty components are replaced. Since some assembly processes are irreversible, this approach is not even feasible on Earth. Thus, diagnostics must employ indirect methods of isolating the faulty components.

Because no single diagnostic method will reveal all forms of malfunction, the CLEAR task recommends the following steps:

- Visual examination
- Fundamental component property measurement
- Utilization of internal capability, including BIT, loop-back techniques, and Joint Test Action Group (JTAG) boundary scan
- Power-off characterization and signature analysis techniques
- Power-on functional tests
- Emission signatures, including radiofrequency (RF) and thermal emissions

7.2 CLEAR Diagnostic Assumptions

The following steps were assumed in developing the operational concept for CLEAR diagnostic operations:

- Existing system-level diagnostic and health-monitoring systems have identified an ORU-level fault, and subsequent self-tests have isolated the fault to a specific card or SRU level.
- The crew has removed the ORU and has performed disassembly sufficient to remove the errant subassembly or circuit card.
- The crew sets up and connects the unit under test to be probed manually or robotically by CLEAR diagnostic and test hardware.

7.3 CLEAR Diagnostic Technologies

In addition to commonly used methods of measuring electrical parameters, the diagnosis of faulty circuits will employ other techniques, including those discussed in the following sections.

7.3.1 Visual Examination

Visual examination is considered to be the initial screening that can most quickly identify a fault with little or no equipment. Faults like burnt components, broken leads, and broken or missing connector pins can be found without tools or equipment. More subtle flaws require optical lenses and imaging. Broken IC solder joints can be found by viewing magnified images and through simple mechanical probing with a dental tool. A microscope lens and digital camera combination will provide clear images for both the flight crew and CLEAR TEST. The downlinked images will let the ground crew see exactly the same image that the flight crew sees, thus saving the time-consuming process of verbally describing the image. Infrared (IR) imaging also needs to be evaluated and considered as a potential tool.

7.3.2 Analog and Complex Signature Analysis Diagnostics

A power-off technique called analog signature analysis (ASA) developed by Huntron has been used by the U.S. Navy as a simple, but effective, form of diagnostics. The U.S. Navy's Gold Disk program records and distributes "known good board" ASA signature data on specific circuits throughout the Navy. The Gold Disk (a compact disk) in combination with an ASA unit provides a simple-to-use initial screening test that can isolate many simple faults. The approach is limited to the number of accessible circuit nodes. Many complex circuits with multilayer boards and BGA or LGA package ICs have inaccessible nodes. Furthermore, the greater the number of devices on a node, the more difficult it is to isolate the faulty component.

CLEAR is advancing the approach by measuring complex impedance in the frequency domain. The complex signature analysis (CSA) approach exploits network analyzer technology to reveal frequency-dependent behaviors and exploit self-resonant and network-resonant characteristics to isolate faults. It can also reveal the resonant behaviors of devices that are physically isolated from the node. It can even detect breaks in circuit-card vias and traces. Some ICs have structures so deep that they are inaccessible by power-off diagnostics.

7.3.3 Built-In Test

CLEAR will exploit BIT capability whenever feasible. Circuits with microcontrollers will often provide self-diagnostic firmware to test internal registers and verify input/output (I/O) functions. Special interfaces are often needed to access these routines at the card level. There are many ways to implement BITs, but all of them require internal programming code that is especially created to perform testing. The vast majority of the testing involves checking digital memory, internal registers, and I/O ports. The tests are often intended to verify that the states of registers are consistent with the specific configuration. BITs may also test the interface with external devices and confirm that output and input channels are connected to the correct external device. BITs may be used with analog circuits that have a digital interface. Such circuits may have loop-back channels where outputs are temporarily connected to inputs so that the analog signal can be read back and verified. BITs on analog circuits will often automatically check measurements against calibration standards. For high-density ICs, a special Institute of Electrical and Electronics Engineers (IEEE) standard, JTAG 1149.1, is widely used.

7.3.4 Joint Test Action Group Boundary Scan

The IEEE 1149.1 boundary-scan techniques were developed by JTAG as an industry standard to aid manufacturers with challenges in testing ICs that were innately complex and had no direct access for external equipment. JTAG-compliant devices have internal "boundary cells," special registers, and access port pins specifically built in to support boundary scan operations. When activated, scan cells capture I/O signals and send the data out through a test access port to be read and analyzed by external equipment that may be no more than software in a laptop computer.

CLEAR will exploit boundary scan and similar techniques for both diagnostic and test operations. Note that CLEAR can only exploit the JTAG boundary scan if the manufacturer employs the standard. The initial design must incorporate the IEEE 1149.1 standard, and appropriate external software must be provided to enable and execute the boundary scan.

7.4 Diagnostic Teleoperations Scenario

As stated in the assumptions in Section 7.2, vehicle system managers will have determined the system-level faults, identified the affected ORU, removed the ORU from the system, and performed ORU self-tests to help isolate the fault to a specific SRU subassembly (e.g., CCA).

- The crew will have de-integrated the suspect SRU and placed it in the apparatus or connected the appropriate diagnostic interfaces.

- The ground-based engineering support team (CLEAR TEST) will have been assembled to plan the diagnostic operations.
- The team will review and analyze available data from higher level tests, including system tests, ORU BITs, and SRU tests, if available.
- At this point, CLEAR TEST also will review design information from the design database, including test specifications.

To conserve effort, the team will first assume simple causes and define a (or use a predefined) sequence of visual examinations and a simple probing test to further characterize the circuit's condition and malfunction.

- Simple tests can be used to quickly isolate simple causes like blown fuses or bad connections.
- Interaction between the ground and flight crew may be short but frequent in this phase.

If earlier testing has not isolated the cause, then a more rigorous test plan must be developed, and ASA or CSA instruments can be employed in the power-off condition. If an automated probing capability is employed, then a motion control and measurement program will need to be created, if one does not already exist for this application.

- Circuit card computer-aided design (CAD) data (Gerber files) can be used to locate test node coordinates for the motion-control system.
- Existing ASA and CSA characterization data may be pulled from the CLEAR library.
- Motion-control sequences can be programmed by industry standard motion-control codes, often referred to as "G-Codes," which can be used to direct the motion.

If only a few easily located points are needed, an operator may simply slew a probe into position using a manual override feature that is commonly available for computer numerical control (CNC) machines.

- Visual examination by high-resolution video or IR cameras can be controlled manually.
- This manual control may be executed by the flight crew or by CLEAR TEST.
- Special safety provisions must be included, such as automatic collision proximity detection, slow-motion feed rates, operator interlocks, and preset exclusion zones.
- Motion control position data can be captured by setting up the apparatus in a "teaching mode." This method allows a crew member to manually position the apparatus to pick up key registration points, which can then be used to create a simple motion-control program and assure proper machine coordinate scaling and alignment and to establish exclusion zones.

The complex sequence of programmed probing by CLEAR TEST will be validated in a three-dimensional simulator model or on a physical prototype.

- All programming will be performed offline, so no teleoperation or crew time will be consumed.
- This is intended to provide an initial screening for motion control and operation errors that might damage hardware or injure crew.
- The probing sequence will be stored in the CLEAR library and uplinked to the flight crew via the teleoperations link.
- The team also will need to access design and test specifications down to the component level.

For complex components like ICs, the team may be able to determine if special BITs or JTAG boundary scan testing is available that is not normally accessible for SRU and ORU testing.

- The JTAG ports will be accessed by a small custom connector in a manual hookup operation.
- JTAG boundary scan or BITs will require preprogrammed test software.
- CLEAR TEST will create and validate the program offline.
- The JTAG test program will be stored in the CLEAR library and uplinked to the CLEAR diagnostic and test hardware.

Once the prior diagnostic cycles have been completed by the flight crew and CLEAR TEST, there should be sufficient information to determine which components should be replaced. In some cases, however, it may be impossible to isolate a single component, and it may be necessary to perform incremental repairs.

- Faults may be in components that other devices depend on, such as the power supply.
- Faults in one component may cause damage or faults in other devices.
- It may not be safe to power the circuit up until certain faults are eliminated.

A failure modes and effects analysis may be needed to determine if an incremental repair is needed and in what order.

- A repair of a key component may make it possible to diagnose other devices that could not be accessed.
- Rerunning ASA or CSA diagnostics or JTAG scans after an incremental repair may reveal new, undetected conditions.

8.0 Operational Concept for CLEAR Semiautomated Repair

8.1 Semiautomated Repair Objectives

As stated in the assumptions section, component-level repair is aimed at reducing the impact of logistics spares. A semiautomated capability is aimed at the need to perform repairs beyond manual methods, to minimize the impact of repair operations on crew time and training, and to free the crew to focus on the mission objectives.

The robotics apparatus employed in a semiautomated CLEAR approach is intended to duplicate portions of the original manufacturing process. As discussed in CLEAR–DOC–006, solder reflow processes are the dominant method for fabricating CCAs. BGA and LGA have become the packages of choice for high-density electronics. BGA and LGA devices can only be reworked by reflow methods. The semiautomated repair apparatus will include solder reflow technology with the capability to perform solder reflow for BGA and LGA devices.

The actual repair apparatus is expected to perform a number of roles and to accommodate materials and process equipment. The repair apparatus will conform to the following spacecraft constraints.

- Weight will be less than 100 kg.
- Volume will be less than 0.5 m^3 when deployed.
- Power will be less than 1500 W nominally.

These objectives are considered to be reasonable for the interim until CxP architectures evolve with definite requirements.

8.2 CLEAR Repair Assumptions

The concept of operation for the CLEAR repair apparatus is based on the following assumptions:

- Crew will retrieve the ORU and disassemble it sufficiently to remove individual circuit subassemblies.
- CLEAR equipment will make repairs at the circuit-card level by removing and replacing components.
- Interconnecting cables and wires will be disconnected and removed manually.
- The spacecraft or flight facility will provide sufficient workspace volume, power, and lighting to support repair operations.
- CLEAR equipment will contain vapor, liquid, and particles for the repair process within the CLEAR repair apparatus.

8.3 Repair Apparatus Technologies

The functions and related technologies required to provide a semiautomated repair capability that is suitable for teleoperated control are described in Section 8.3.1.

8.3.1 Robotic Functions

An apparatus can be described as being robotic if it is capable of precisely controlled, yet flexible, multiaxis motion. For CLEAR, it is important that semiautomated motion provide sufficient performance to place components with more accuracy than with human crews. The following functions are required for robotic motion control.

Circuit-Card Holder.—This device secures and supports CCAs securely yet provides access to the card components for repair operations and can be reoriented as needed to provide access to all sides. The

holder also may need to support the card during preheat and reflow processing. It also may provide conductive heating and cooling.

    Diagnostic and Test Support Features.—This includes provisions that will support wiring, connectors, jumper wires, and other electrical hookup features that are needed for diagnostic operations and testing.

    Access for Manual Operations.—The repair process requires easy access to the circuit to perform a number of manual repair operations or manual operations in support of automated repairs. For debris or fluid processes requiring containment, a glovebox or similar access accommodation must be provided. For processes not requiring containment, the enclosure must have a simple access method that permits rapid setup and handling of tools and equipment.

    Automated Probing.—For point-to-point probing, as in ASA or CSA diagnostics, the repair apparatus will be able to move probes through a sequence of probe points (or test nodes).

    Process Tool Storage.—Tools will range from simple single-piece hand tools to electrically driven motorized tools. The various tools should be stored in a manner that provides easy, quick access while securing the tools against drifting in low gravity.

    Process Tool Staging.—Staging is the temporary holding or staging point for tools that are immediately required for the process but must not be allowed to drift out of the workspace or into the apparatus machinery. For automated tool changing, the tool staging will provide access for a tool-changing mechanism.

    Process Tool Handling.—The robotic apparatus will be able to handle specific tools or devices used in the repair process. The tools may be loaded manually, but the apparatus must also accommodate an automatic tool-change mechanism. The process tool-handling device will also provide electrical power for motorized tools and possibly pneumatically driven tools such as dispensing syringes.

    Component Staging.—The replacement components may be organized as kits for specific circuits. The components must be placed in a staging area easily accessible for robotic pick and place in both removal and installation. Certain components require a preheating operation and a heated staging tray. Industry uses dispensing tapes, tubes, and trays to handle different types of components in pick-and-place operations. The staging will also need to present the component in a manner that makes it easy for the apparatus to properly place the components in the right orientation.

    Component Handling.—Many repairs can be accomplished by manual parts removal and placement. Large integrated circuits encapsulated in surface mount technology (SMT) BGA or LGA packages have critical alignment and preheating requirements. The robotic component handler must handle hot components and accurately place them (e.g., pick and place). If needed, the handling mechanism may be required to hold a component until the reflow process is complete. If components cannot be preoriented, the handling mechanism will perform orientation and alignment operations, in concert with optical alignment techniques.

    Collision Avoidance.—This is a motion-control issue, where the semiautomated apparatus must move in a manner that avoids collisions or interference between various parts of the apparatus, the repair target, fixtures, and even crew members. In industrial applications, certain interlocks and travel stop switches can be set to prevent travel into certain areas. For CLEAR, there will be many different setup configurations, and each has its own restrictions and collision hazards. Furthermore, different process phases pose different risks; thus, hard stops and limit switches would be constantly reconfigured, creating substantial crew workload and chance for error. CLEAR will deal with this by proper planning, programming, and validation.

    Borrowing techniques from industrial robotics and CNC operations, motion-control programming will include modeling exclusion zones into the overall repair program. CNC and robotics motion planners will model the environment and set the limits on motion travel based on physical constraints of the real system. The planner will determine where features like clamps and fixtures are located and create a three-dimensional envelope around them. Validation software tools will step through the motion-control program and detect where the motion path collides with any point in the exclusion zones. Collisions will

require a readjustment of the motion path and rerun of the validation program until the motion-control program is determined to be free of errors.

8.3.2 Logistics for Repair Materials and Processes

Materials Storage.—Repair processes involve a number of reactive process materials and chemicals. For soldering, industry prefers to use solder powder suspended in a flux paste for automated operations with surface mount and BGA and LGA devices. The reactive flux has a limited shelf life and will become too viscous to dispense. Refrigeration will extend the shelf life of flux and other chemicals. If no materials storage is provided, then CLEAR will require built-in storage. In the absence of refrigeration, CLEAR must assure long shelf life by an alternative means, including reformulated materials.

Materials Staging.—Materials must be packaged in a manner that minimizes crew operations and assures reliable and accurate dispensing. For automated operations, the materials must be presented in a manner that allows easy handling and dispensing. Certain materials also must be conditioned thermally.

Materials Dispensing.—For dispensing materials, other than solder, a number of materials and techniques are available:

- Aerosols can apply coatings, fluxes, and cleaning agents. However, these are discouraged because of waste and the need for masking. They may be suited for properly contained aqueous cleaners.
- Viscous liquids and paste, which may be applied by syringe, are maskless, and are suited for automation.
- Techniques where low-viscosity liquids are microdosed by individual droplets similar to those in inkjet printing are the most accurate techniques, are maskless, and are suited to automation.
- Contact brush techniques are effective but are best suited to manual operations. Brush electroplating is an important technique that is suited to the repair of broken circuit traces, refinishing damaged connections, and repairing broken printed circuit board vias.
- Tapes (primarily manually applied)
  - Dry adhesive-backed tapes can replace conformal coatings.
  - Preimpregnated tapes (prepregs) are widely used in industry for composite fabrication including the majority of printed circuit board laminates (refrigeration may be required).

Solder Dispensing.—Metal solder, either in solid or paste form is a primary repair material. Solid solder wire is suited for simple manual repairs. For automated repairs, a wire feed system similar to a welding wire feed can be employed; however, solder paste is the most widely used form. Solder paste is a solder powder suspended in a viscous liquid flux. Automated dispensing of solder pastes will be accomplished by programming a robot that dispenses discrete doses of paste at preprogrammed locations. Manual dispensing will be performed by using a screen and squeegee technique. Prefabricated solder template (screen) kits may be used to manually deposit patterns of solder paste.

8.3.3 Reflow Process

The primary method of replacing components on soldered printed circuit boards is to use the solder reflow process. There are three primary types of reflow: hot-gas reflow, IR reflow, and vapor-phase reflow. Each has special advantages and varied levels of dependency on gravity.

Reflow is attractive in comparison to other techniques (conductive soldering or wave solder) because it is innately simple, repeatable, and easy to automate.

In manufacturing, the entire circuit card passes through the reflow process, and all components are soldered at once. For repair, only specific devices are to be replaced; thus, the heating must be localized. In production, reflow can be performed in simple convection or IR ovens since the whole circuit is soldered in one operation. For repair or rework, reflow is more difficult to perform because only a small area needs to reflow while the rest of the circuit remains solid.

For repair, reflow is performed twice, once for part removal and a second time to install the new component. If the solder remains liquid too long, brittle intermetallic builds up in the solder joints, reducing their reliability.

In circuit production, the circuit is placed in a heated environment (air or nitrogen), and the temperature is raised in a series of steps. The steps involve ramping the temperature up in a specific temperature-time profile usually followed by a soak period, where the temperatures of all the circuit materials are allowed to normalize. Each soak temperature has a specific function, such as flux activation, stress normalization, and solder melting (reflow). Once reflow occurs, the circuit is allowed to cool or ramp down in temperature. The ramping rates control stresses.

In circuit rework, the entire circuit is preheated to a uniform temperature well below the reflow temperature. This activates the solder flux but does not melt the solder, so no intermetallic compounds are created. By preheating the circuit, the temperature difference between the circuit and the reflow heat is reduced; thus, less heat is conducted away from the heat source. For component removal, the reflow heat is applied until the solder melts and the component is easily lifted. A cooldown cycle is often needed to allow for cleanup of the repair site and dispensing solder pastes as needed prior to installing a new component.

For installing the replacement component, the circuit and the component may be preheated separately. A simple pick-and-place device positions the new device; then localized heating is applied to reflow the solder joints.

Hot gas reflow employs a heated gas that is ducted directly to the repair site to heat the component until solder reflow is complete. Hot gas is used for removal and for installing the new component. Hot gas reflow is difficult to localize without special flow nozzles that focus the heat on a component. Shielding adjacent components from hot gas may require special fabricated shields.

IR heating follows a similar procedure, except radiant energy is used. IR heating can be masked with simple reflective foils; therefore, heating of a specific component zone is easily controlled. IR heating is sensitive to the reflectivity and emissivity of the component package, and special measures may be required for metal packaging, such as hybrid devices. IR can be prone to overheating and damaging components because of the fairly uneven radiation pattern of common IR sources. In production, it is common to have a mixed IR/hot-gas system.

Vapor-phase reflow is unique in that it depends on the thermodynamic properties of the working fluid, and it is used in spacecraft circuit production on Earth. Vapor-phase reflow is actually a multiphase system with a liquid bath that is heated, creating a dense vapor that settles above the bath. The dense vapor transfers heat into the circuit with the added benefit of displacing oxygen and thus minimizing the need for flux to remove and prevent oxidation. The temperature is controlled by the physical boiling point of the fluid. When the circuit exceeds the boiling point, the vapor no longer transfers heat by condensation, and condensed liquid vaporizes, thus cooling the circuit board. The process is virtually the same as a heat pipe that is used for spacecraft thermal control. The main disadvantage of the approach is the problem of handling multiple phases in low gravity in an open system. Furthermore, it is difficult to focus or direct the heating at a specific component.

The repair apparatus will need to be composed of materials that are compatible with the high temperatures of the reflow process or be protected from the high temperatures by hardware.

8.3.4 Deflux and Cleanup Processes

Defluxing or removing residual flux eliminates the problem of flux corroding the circuit after soldering. Some fluxes are formulated to provide more complete vaporization and may be less aggressive, albeit less effective. These, so-called no-clean fluxes are more accurately described as "low-residue fluxes." These are really aimed at high-production, low-cost products where residues do not significantly reduce product life.

Cleaning is essential to high-reliability circuits. Conformal coatings trap fluxes against the board and create long-term problems with corrosion and crystal growth. Thus CLEAR will make provisions to provide postrepair cleaning or develop solutions to eliminate harmful residues.

From a crew and vehicle safety standpoint, aqueous cleaners are preferred. The final rinse process would be accomplished with de-ionized water. Final cleanliness will be checked by measuring the ion content of the rinse runoff. Aqueous cleaning implies liquid handling, containment, and disposal; liquid ion measurement techniques; and an additional drying step.

8.3.5 CLEAR Process Environment Containment

There are a number of reasons that a repair apparatus needs containment. The most common is the need to contain any vapor, liquid, or solid debris that could harm the crew or spacecraft systems. From a repair process perspective, containment can provide a separate and favorable process environment. Many of the materials found in manufacturing and rework processes, such as flux, are needed to combat natural environment effects related to oxidation, humidity, and surface contamination.

If hardware were kept protected from such environments after initial cleaning, it would be possible to eliminate or diminish the need for flux. In an ideal process environment, one could create a flux-free process that would eliminate the majority of the cleaning chemicals. This would reduce consumable payload upmass and storage, eliminate shelf-life issues, simplify the process, and make the process more reliable.

8.3.6 Apparatus and Process Control Software Development

The repair apparatus will perform a number of repair tasks that require some robotic motion. Although it will be possible to manipulate the hardware directly through teleoperations, this will be reserved for simple motions where signal interruptions would not have a significant consequence. Moving robotically mounted cameras would be such an example.

Most operations will require a motion-control program prepared specifically for the individual operation. Thus, each individual component will require distinct parameters and motion-control sequence. CLEAR will adopt techniques that simplify the effort required to program a repair apparatus. Industry has developed automated motion standards that serve as a motion scripting language and that are widely used in automated CNC machining equipment. Referred to as "G-Codes," these simple alphanumeric codes describe points along a machining path and related parameters, including motion speed and tool selection.

G-Code interpreters perform the interpolation required to define a path between the described points. G-Codes break operations down to elemental motion and tool operations. Each tool and operation has unique operating parameters, such as starting coordinates, tool path, axis speed, spindle speed, and direction. The robotic CNC machine has a built in G-Code interpreter that allows an operator to program complex operations as a series of simple motion steps. Once programmed, this code is usually validated by stepping through the operation at low speed or by using a code validation tool that illustrates the machining operation in three dimensions. Once validated, the code can be stored in a library and reused. The CLEAR repair apparatus will operate in a similar manner.

Control G-Codes will be validated offline, and programming will be loaded by communication uplinks. The repair apparatus will be designed to exploit existing robotic control standards and validation tools.

8.4 Repair Teleoperations Scenario

In review of the earlier diagnostic teleoperations, vehicle system managers will have been working the process of determining the system-level faults, identifying the affected ORU, replacing the ORU, and performing ORU self-tests. They also will have isolated the fault to a specific SRU subassembly (e.g., CCA). In parallel, a CLEAR TEST will have been assembled to address the diagnosis, repair, and test of the faulty ORU.

At this point, the CLEAR TEST and flight crew have stepped through the diagnostic process, and the CLEAR process library and development tools have been employed to create semiautomated diagnostic procedures. The validated diagnostic code has been executed on orbit, and the faulty component(s) have

been identified. Now that team members know which components need to be replaced, the process becomes more predictable, and the planning and programming can now employ specific processes that may already be available in the library. Furthermore, the team can start planning the functional testing required to complete the repair.

The repair cycle starts by rechecking the alignment of the circuit. This may be a repeated action, but it is necessary to assure that the circuit is fully aligned for the repair process. Repair will most likely require a combination of operations, including reflow, pick and place, site preparation, solder dispensing, and cleanup.

The registration points may be located by imaging; however, the vertical location of the substrate and components is important, and a touch-off probe may be used to physically gauge the vertical height. Z-axis dimensions must be known for accurate solder dispensing, pick-and-place positioning, and reflow.

Like the diagnostics teleoperations, the repair teleoperations will require significant preparation offline. The VMDB will be used for specific design information about the circuit card and the specific components including information regarding reflow temperature profiles. The CLEAR process library will be searched for similar repairs. The repair operation will be planned and programmed using programming and validation tools.

To avoid potential damage to hardware, designers of the repair apparatus motion-control program will include safety limits and exclusion zones that will constrain motion to a specific three-dimensional operating envelope.

Because components are to be removed and replaced, they will require a dedicated staging area. New components will be organized in a tray that will make it easy to locate and pick the components. A similar tray will be needed to capture the bad components. The placement of specific components in the tray must also be specified in the apparatus control program.

In a low-gravity environment, the absence of buoyancy-driven convection tends to allow hot gas to accumulate around heat sources and the heated target. The CLEAR repair apparatus can exploit that behavior and reduce the heat flux required. A special thermal analysis will be needed to predict the effect and adjust the normal heating schedule to achieve the desired reflow temperature profiles. The CLEAR task proposes a low-gravity thermal analysis and prediction program as a specialized tool in the CLEAR process library.

If an inert atmosphere is required, then an inert purge cycle will be used to remove oxygen from the system. A gaseous nitrogen supply such as that available on the ISS may be used. Alternatively, an oxygen-nitrogen generator may be used to locally filter oxygen out of the enclosure.

The apparatus will perform a preheat cycle on the circuit board to bring the temperature of the whole board up to a preheat temperature that is usually 100 °C below the solder melting point. A localized heater will apply heat via hot gas or IR to complete the solder reflow (melting) process. At this point, the robotic apparatus will remove the device and place it in the designated tray.

Once the components have been removed, the assembly will need to be cooled down. The cooldown will be necessary to prevent the growth of intermetallic crystals that would weaken solder joints. The cooldown also will provide time to clean and prepare the board to receive new components.

Manual cleanup and preparation may be performed by the flight crew since this type of operation is very difficult to program. If needed, the circuit card may be removed from the apparatus for manual cleaning. For many devices, a solder paste will be dispensed on the solder pads and, if needed, an additional staking adhesive may be applied to help retain the component during reflow. This operation may also be performed manually by the flight crew.

The apparatus will once again preheat the circuit card and may also preheat the component at a staging point. The robotic apparatus will pick up the component, align it with the circuit card, and place it in position.

A localized heater will heat the component until the solder paste reflows. In production, the heat application is most often a fixed-time event that has been determined by dry-run tests. However, for CLEAR, a closed-loop temperature control may be more reliable. A simple noncontact temperature sensor may be employed.

The reflow process will be monitored by the flight crew and by CLEAR TEST via high-resolution video. It is possible to detect the reflow visually, particularly with surface-mount devices, where the joints are clearly visible. With BGAs, even though they obscure the view of the solder balls from above, one can view the outer rows via a low-angle side camera. The BGA makes a pronounced settling movement when all the balls have melted, and that can be used as a visual confirmation that the reflow process is complete.

Once reflow is complete, the circuit will again be cooled, cleaned, rinsed to remove residues, and dried. Then it will be ready for postrepair functional tests.

9.0   Operational Concept for CLEAR Functional Test Operations

9.1   Functional Test Capability Objectives

The objective of the functional test is to determine if the repair operations in the previous phase were successful and the circuit is ready to be integrated into the next assembly. This includes a detailed visual examination of the circuit, measurement of fundamental properties, a repeat of characterization measurements (as done in the diagnostic phase), and a series of functional tests.

Functional tests are used to verify that the unit performs its intended functions and meets its functional and interface requirements. Tests are performed at many stages in the original fabrication of the circuit. They are used to screen components and subassemblies prior to assembling them into the next higher level. Likewise, testing at the lowest level possible is essential for successful repairs of higher level assemblies.

9.2   CLEAR Functional Test Assumptions

Circuits launched from Earth must pass through a very stressful dynamic vibration load environment, and thus, a number of tests are intended to verify that the package will survive. However, CLEAR will be repairing ORUs on orbit in a relatively benign environment. For in situ repairs, these severe tests would not add value to hardware already in space and only add risk of damage. The CLEAR approach to testing is to only use test procedures that are relevant for the space environment.

- Repairs are assumed not to invalidate prior testing of devices not directly affected by the repair.
- The postrepair test will be a delta acceptance test or a subset of the acceptance test at the SRU (circuit card) level of assembly.
- Functional test procedures will be tested on the ground to develop and validate test programs.

Functional tests are more challenging than diagnostic operations because of the demand for specialized equipment and the inherent weight penalty they pose. Functional tests need to be performed in their normal operating context. That is, a circuit interacts with the hardware and software around it. In some cases, it is feasible to test the hardware in its parent assembly. However, for many critical systems, this type of test could further damage the system. To fully test outside the system implies special hardware to emulate the external systems or parent assembly interface. The functional test assumptions follow:

- CLEAR will provide functional tests for the SRU or CCA level of assembly.
- The vehicle program will have sufficient equipment or BIT capability to verify that an assembled ORU is fully functional.
- For low-power analog and digital signals, CLEAR expects to be able to emulate many external functions. External loads for systems like electrical power and RF are both governed by the load-handling capacity and may be very heavy in contrast to other interfaces.
- For electrical power loads, CLEAR assumes that the parent assembly can safely dissipate electrical power for functional tests.
- For RF power loads, CLEAR assumes that the parent RF (communications or radar) assembly can safely dissipate power for functional test purposes.
- CLEAR assumes that the program can perform ORU tests (primarily BIT) and system-level tests. CLEAR equipment will be available to augment existing abilities.

9.3 CLEAR Functional Test Types

The following describes the type of functional testing that CLEAR will need to perform:

Visual Examinations.—As used in the diagnostic and repair segments, visual examination by the crew and by imaging cameras will be an important part of the functional tests. Examination will be needed to assess the condition of the repair circuit and look for visual indications that the soldering operations were complete and do not have common flaws like solder bridges. Low-power microscope lenses will be needed for closeup examination. A microscope lens and digital camera combination will provide clear images for both the flight crew and CLEAR TEST.

Power Supplies.—CLEAR will provide external power for the functional tests. The power voltage and current level will be limited because of spacecraft constraints. The power supplies will provide programmable parameters including voltage, current, current limits, over-current alarm, and cutoff settings. The supplies will provide separate power channels. Unusual power needs, such as high voltage or high current, may require special additional hardware.

Stimulus Signals.—CLEAR will provide stimulus signals (analog, digital, and RF) bounded by yet-to-be-determined limits for voltage, current, power, frequency, and channel count. Stimulus signals may include continuous sine, square, and sawtooth waveforms, and noncontinuous single- and multiple-pulse, tone-burst waveforms. Modulation of stimulus may be simple amplitude- and frequency-modulation modes. Complex waveforms that involve multiple modulation modes may be provided by a programmable arbitrary waveform generator(s) for specific applications. RF signals may be generated directly by direct synthesis or by using frequency upconverter techniques.

Signal Measurement.—CLEAR will provide signal measurement (analog, digital, and RF) for the signals most common to spacecraft applications. The equipment will provide mixed-signal (analog and digital) measurement for the baseband frequency range. The signal measurement capability will match or exceed the stimulus signal-generation capability. RF-range signal measurements will handle RF signals directly by measurement or by using downconverter techniques.

Automatic Calibration.—CLEAR will provide automated calibration capability to assure that measurements are accurate. Calibration will use fixed references (usually National Institute of Standards and Technology (NIST) traceable) that compensate for changes or drift in equipment due to equipment temperature, changing scale ranges, variations from channel to channel, and equipment age effects.

9.4 Functional Test Technologies

Like the diagnostic element of the repair process, the functional test element has multiple technology options to select from. The technologies described in Sections 9.4.1 to 9.4.6 are expected to be required to assure that repaired circuit assemblies are suitable to return to service.

9.4.1 Built-In Test

As discussed in CLEAR–DOC–006, BIT substantially reduces the need for external test equipment. As described in Section 7.0, a number of circuit built-in capabilities can reduce the need for external test equipment. BIT, which is primarily internal software code, can exercise certain functions and read back the results by checking the contents of specific registers. If an unexpected value appears, a problem is flagged usually in the form of an error code that can be passed to the system-level health-monitoring system.

As a functional test, a BIT does not necessarily provide sufficient diagnostic information to determine the root cause. BITs are aimed primarily at determining that the circuit is functioning normally. BIT error codes may not define the root cause or suggest corrective action since they may be a result of one of many root causes, in effect, error codes can be considered to be symptom reports.

Often a problem lies in the software and is not an actual hardware issue. Because of this ambiguity, it is ultimately up to the test engineers to determine if the fault poses a problem and to evaluate the consequences. Persistent errors may require additional tests and external equipment to isolate the fault. A BIT

can substantially reduce the need for external equipment, but it cannot isolate all the root causes of a problem.

9.4.2   Joint Test Action Group Boundary Scan Functional Test

As described earlier, IEEE 1149.1, also known as the JTAG boundary scan, is a technique used to test large-scale ICs, such as microprocessors, application-specific integrated circuits (ASICs), and field-programmable gate arrays (FPGAs) installed on the circuit card. It is particularly useful for FPGAs, where the JTAG port also serves as a means of in-circuit programming of the device.

The boundary scan isolates the I/O pins so that the IC can be tested in isolation. Although much of the testing relates to programming, it also can determine if internal gates or registers have failed. Access is accommodated by the JTAG test access port, which provides an interface for an external testing device that is programmed to set up and execute JTAG routines. JTAG boundary scan can reduce the need for external equipment, but as a form of BIT, it cannot isolate all causes of a problem.

9.4.3   External Interface Emulation

Interface emulation is needed to fully test a circuit's interaction with other hardware as part of an overall system. Internal BIT or JTAG tests can locate internal problems; however, many problems are due to interactions with an external system. Testing interactions with external circuits may involve transmitting or receiving signals, supplying or consuming power, and dissipating thermal loads. Testing of external interfaces will reveal problems associated with bad connections or wiring, and problems with communications. External connections introduce power supply or instrument noise, spurious network behavior, marginal signal strength, and other effects that may confuse an otherwise stable circuit.

For circuits that handle significant power dissipation, full-power tests over an operating period are the best way of revealing stability or thermal problems. For RF circuits, power amplifier outputs must be connected to an impedance-matching dissipative load, or RF reflections will damage the circuit.

9.4.4   External Load Equipment

The external loads tend to imply heavy power dissipating devices. Regulated power supplies often require tests that apply rapidly varying loads to test the supply stability. Programmable load simulators used for ISS power system acceptance testing occupy a full instrument rack. For spacecraft, the added weight of large load equipment is prohibitive. The CLEAR task will examine alternative methods of providing test loads, which may include the use of existing onboard systems that can provide electrical loads for tests.

9.4.5   Signal Routing

To cover a large variety of circuits, it is necessary to provide a variety of connector options. There is no "universal connector" scheme that will accommodate all connectors. For safety, the program deliberately mixes connector sizes and keying to prevent the catastrophic consequences of inadvertently connecting the wrong hardware together.

Custom-built test connectors and cable harnesses are normally used in ground-based functional tests as a way to save time in hooking up the equipment. These test cables become a significant portion of the test system weight and consume considerable stowage volume. However, without these cables, the process of connecting instruments to a circuit under test with individual test leads can consume a substantial amount of crew time. Signal routing is one of the most difficult barriers to creating an effective general-purpose instrumentation system.

A signal matrix scheme can reduce the number of unique connections between a circuit card and instrument. In fact, it allows multiple instruments to be connected to the same pin. The matrix serves the same purpose as old instrument patch panels, which used replaceable jumper panels to connect signals with specific configurations. When a wide range of signal types must be accommodated, a wide range of conductor characteristic impedance values also must be considered.

CLEAR is examining signal-switching matrix technologies that can be configured on demand under remote control as an effective replacement for patch panel capability. A switching technology under investigation by the U.S. Air Force for satellites is called the Reconfigurable Manifold. The study considers multiple switching technologies including microelectromechanical systems (MEMS) switching devices. Signal routing is essential for an effective SI approach (described in Section 9.4.6).

9.4.6   Synthetic Instrument

SI is a scheme to create general-purpose automatic test equipment that can accommodate a wide range of test articles and test procedures. Flexibility and programmability are its primary objectives. It also appears to be the best option for achieving a compact, lightweight system that can be remotely configured easily.

Normally, the automatic test equipment comprises a mix of equipment, including emulators of specific external equipment, programmable power supplies, and rack-mounted signal generators, scopes, and analyzers. To distill the hardware into a smaller package, developers need to convert the functions provided by digital controllers, signal analyzers, and signal synthesizers to pure software. Analog front-end hardware, such as an instrument amplifier linked to analog-to-digital converters, and output amplifiers driven by digital-to-analog converters are still needed.

Instead of having software executed on a common microprocessor that executes code in serial fashion, the code can be burned in or programmed into an FPGA to achieve high performance. FPGAs can exploit the higher throughput of parallel channels and pipeline architecture.

9.5   Functional Test Teleoperations Scenario

Teleoperations will need to support both postrepair visual examinations and functional tests. Functional testing will progress from low-level components, to intermediate SRU level, to ORU level, and ultimately, to system level.

The first step will be postrepair visual examination:

- These examinations will look for flaws in the repair and any flaws that were missed in the initial diagnostic operations.
- Detailed high-resolution examination could be performed by CLEAR TEST using camera facilities provided by the apparatus.
- The procedure will provide a digital image record of the repair for future reference.
- At this point, before and after photos could be compared to determine if any collateral damage occurred in processing.
- Imaging cameras could be controlled by a prescripted routine, or CLEAR TEST could control the cameras interactively since there is little risk and communication interruptions have little consequence.

As in earlier sections of the repair process, CLEAR TEST will require access to the design database so that they can prepare a procedure. Because many functional tests may cause damage if they are set up improperly, a dry run on Earth or a similar procedure validation will be required.

There will already be a substantial test history on the circuits based on prior development, qualification, and acceptance test records. CLEAR TEST could select the tests most suitable for verifying the circuit. Functional tests are driven by specific verification requirements, thus testing will be defined formally in test specification documents. Many changes will be made to account for the space environment and spacecraft and operational constraints, but otherwise, the tests required will be well defined.

- CLEAR TEST will formulate the functional tests at the component and SRU level.

- The VMDB, including ORU test specification documents, would be the primary source of test information.
- Existing functional test plans and procedures will aid in planning but will have to be reworked to suit in situ tests.
- Functional test procedures will have to be validated prior to in situ testing.

The flight crew will have to select and hook up the appropriate connections to set up the tests and to provide power. Multiple cross checks and validations will be needed to assure that a safe and effective test is executed. Note that a separate test setup may be required for each functional test at each level.

- ASA and CSA tests support both component and SRU-level testing and should precede SRU-level functional tests.
- The probe routines used for ASA and CSA routines must be repeated to provide characterization data and to document the repair.
- Inspection will be needed to ensure that the circuit is properly hooked up, equipment is properly configured, and limits are set (particularly power supplies).
- Crew equipment setup must be validated by the CLEAR team prior to power up.
- Power will be applied with a validated safe power-up sequence.
- Specific programs for configuring the test equipment, including programs for creating synthetic instruments, will be uploaded; and pretest validation checks and calibration routines will be performed.

Component-level tests will vary in complexity, and testing should involve the replaced components and any other components that interface with the device.

- Fundamental measurements will suffice for discrete components.
- ICs will execute BIT and/or JTAG test schemes.

SRU functional testing strategy is very dependent on the system architecture and how functions are allocated among the hardware modules. Furthermore, SRUs will have a functional hierarchy within the ORU. For example, within the ORU certain SRUs will dominate the structure, such as the motherboard and its relation to the subordinate daughterboards. The motherboard can be expected to have substantial BITs that thoroughly examine its functional readiness. Because daughterboards are simply extensions of the motherboard and cannot function independently, they have no independent test capability. For ORUs that use a common backplane bus, the motherboards and daughterboards have the same physical form factor and connectors, but the functional hierarchy remains.

- SRU testing will be a combination of internal BITs and externally driven functional tests.
- BITs will be supported by CLEAR and are expected to involve a simple interface with an external BIT controller that will initiate the test and record output data.
- If BITs are not provided, the functional tests using external equipment will be required.

Depending on the architecture, SRU-level functional tests may require substantial emulation of circuit interfaces by the CLEAR equipment.

- Installation and power up must not pose any risk of harm.
- Interfaces to circuits outside the ORU may require emulation by CLEAR.
- Internal interfaces will be handled by the ORU.
- The ORU will require power and cooling support.

To limit the in situ crew time consumption, CLEAR TEST will determine the functions that may have been affected by the repair and the functional tests that are required.

10.0 Concluding Remarks

This document is intended to identify the operations and necessary functions required (and the potential technology options) to accomplish component-level electronic assembly repair as part of an overall supportability plan for the Constellation Program (CxP). This "Component-Level Electronic-Assembly Repair (CLEAR) Operational Concept" is based on earlier studies of International Space Station systems, an understanding of the current state of CxP architecture (2008), and the common weight, volume, crew limitations, and operational constraints of space flight. This document described the capabilities needed and the technology options to achieve these capabilities. To create a context for the capabilities, the document stepped through operational scenarios for diagnostic, repair, and functional test operations.

This document is closely related to "Component-Level Electronic-Assembly Repair (CLEAR) System Architecture" (CLEAR–DOC–008), which organizes the functions identified here into a hierarchy and establishes the relationships between the diagnostic, repair, and test subsystems.

Appendix.—Acronyms and Abbreviations

A/D	analog to digital
ASA	analog signature analysis
ASIC	application-specific integrated circuit
BGA	ball grid array
BIT	built-in test
C3I	command, control, communications, and information
CAD	computer-aided design
CCA	circuit-card assembly
CLEAR	Component-Level Electronic-Assembly Repair
CLEAR TEST	CLEAR Teleoperations Engineering Support Team
CNC	computer numerical control
CRE–1	Component Repair Experiment 1
CSA	complex signature analysis
CxP	Constellation Program
DIO	digital input/output
ETDP	NASA Exploration Technology Development Program
FPGA	field-programmable gate array
G-Codes	industry-standard motion-control codes
I/O	input/output
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IR	infrared
ISS	International Space Station
JTAG	Joint Test Action Group
LGA	land grid array
MEMS	microelectromechanical system
NIST	National Institute of Standards and Technology
ORU	orbital replaceable unit
PRACA	Problem Reporting and Corrective Action
prepreg	preimpregnated tape
RF	radiofrequency
SDTO	Station Development Test Objective
SI	synthetic instrument
SMT	surface mount technology
SoRGE	Soldering in Reduced Gravity Experiment
SRU	shop replaceable unit
STS	Space Transportation System
VMDB	Vehicle Master Database

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14. ABSTRACT
This "Component-Level Electronic-Assembly Repair (CLEAR) Operational Concept" document was developed as a first step in developing the Component-Level Electronic-Assembly Repair (CLEAR) System Architecture (NASA/TM-2011-216956). The CLEAR operational concept defines how the system will be used by the Constellation Program and what needs it meets. The document creates scenarios for major elements of the CLEAR architecture. These scenarios are generic enough to apply to near-Earth, Moon, and Mars missions. The CLEAR operational concept involves basic assumptions about the overall program architecture and interactions with the CLEAR system architecture. The assumptions include spacecraft and operational constraints for near-Earth orbit, Moon, and Mars missions. This document addresses an incremental development strategy where capabilities evolve over time, but it is structured to prevent obsolescence. The approach minimizes flight hardware by exploiting Internet-like telecommunications that enables CLEAR capabilities to remain on Earth and to be uplinked as needed. To minimize crew time and operational cost, CLEAR exploits offline development and validation to support online teleoperations. Operational concept scenarios are developed for diagnostics, repair, and functional test operations. Many of the supporting functions defined in these operational scenarios are further defined as technologies in NASA/TM-2011-216956.

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