A 160×120 Light-Adaptive CMOS Vision Chip for Edge Detection Based on a Retinal Structure Using a Saturating Resistive Network

Jae-Sung Kong, Sang-Heon Kim, Dong-Kyu Sung, and Jang-Kyoo Shin

We designed and fabricated a vision chip for edge detection with a 160×120 pixel array by using 0.35 μm standard complementary metal-oxide-semiconductor (CMOS) technology. The designed vision chip is based on a retinal structure with a resistive network to improve the speed of operation. To improve the quality of final edge images, we applied a saturating resistive circuit to the resistive network. The light-adaptation mechanism of the edge detection circuit was quantitatively analyzed using a simple model of the saturating resistive element. To verify improvement, we compared the simulation results of the proposed circuit to the results of previous circuits.

Keywords: Vision chip, edge detection, retinal structure, saturating resistive network, light adaptation.

I. Introduction

Vision systems, which have image sensors and subsequent processing units for specific purposes, do not use raw images from image sensors such as charge-coupled devices (CCD) or CMOS image sensors (CIS) [1], [2]. Indeed, they use filtered images to improve performance and reduce error rates. In particular, Laplacian filtering, which outputs high signal at the edge of an image, is used in many image processing fields such as pattern recognition and the treatment of noisy images (such as medical images, silhouettes, and infrared red images) [3]-[5]. Until now, computer vision systems, which use CCD cameras for capturing incident images and general purpose computers for acquisition of useful data from captured images, have been used in many applications. However, the systems are limited in terms of size, power consumption, and speed when used in real applications because they consist of two separate modules for image capturing and processing which do not interact. Recently, bio-inspired vision chips have been developed to overcome these problems [6]-[9]. The vision chips, which mimic the structure and functions of image capturing and processing in the human retina, offer several advantages including compact size, high speed, low power dissipation, and dense system integration.

CMOS vision chips for edge detection based on the vertebrate retina are currently being developed [1], [2], [6]-[9]. Photoreceptors, horizontal cells, and bipolar cells in the human retina are related to extraction of edge information from an incident image [10]. All their operations are done in a parallel manner; thus, the edge information of an input image can be obtained in real-time by integrating all mentioned functions on

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a single chip.

In order to realize bio-inspired vision chips based on CMOS technology, it is necessary to design a proper resistive circuit and network for the function of horizontal cells. Previously, there were several resistive networks with linear or non-linear resistive circuits for edge detection. Their output or diffusion length varied according to the changing background brightness level or the light intensity difference of an input image [7]-[9]. Varying output interrupts the extraction of useful information from an output image. Thus, it is necessary to design a new resistive network for maintaining output and diffusion length in a constant value.

In this paper, we propose a saturating resistive network (SRN) that maintains constant output and a constant diffusion length in edge detection. The light-adaptation mechanism for edge detection was analyzed by using a simple model quantitatively. We embodied the proposed saturating resistive element circuit which consists of 4 MOSFETs and investigated it. The operation of the edge detection circuit consisting of the saturating resistive network was investigated by simulating two-dimensional arrays and comparing them with others that were implemented with a single MOSFET and a conventional resistor. The vision chip with 160×120 pixel array was fabricated via a 0.35 ㎛ standard CMOS process. The operation of light-adaptation and image quality improvement of the fabricated chip was investigated.

II. Theory

1. Edge Detection Mechanism of a Biological Retina

Figure 1 shows the structure of a biological retina, which consists of photoreceptors (rods and cones), horizontal cells, bipolar cells, amacrine cells, and ganglion cells. The information falling on the photoreceptors is not sent directly to the brain through the optic nerves, but is instead first processed in a number of ways by a variety of interactions among neurons within the retina. Photoreceptors, horizontal cells, and bipolar cells are related to edge detection while ganglion cells are related to signal digitization [10].

Figure 2 shows a simple example of edge detection. The x-axis represents the position and the y-axis represents the normalized outputs of the photoreceptors, horizontal cells, and bipolar cells, respectively. If a bright light is projected only on the right-hand side of the photoreceptor array, the output of each photoreceptor sends a high-level signal. On the other hand, when a dim light is projected on the left-hand side of the photoreceptor array, the output of each photoreceptor sends a low-level signal. Horizontal cells receive signals from the photoreceptors and spatially smooth them. Edge signals, resulting from the differences between outputs of photoreceptors and horizontal cells, are yielded through the bipolar cells. The smoothing function, so-called lateral inhibition, is mainly characterized by the resistive properties of the horizontal cells. If the diffusion length, the number of pixels that contribute to the smoothing function is large, many pixels will be needed to represent the edge signal. A large diffusion length is directly related to a decrease of the spatial resolution. The difference between the outputs of the photoreceptors and the horizontal cells is directly related to the output of the bipolar

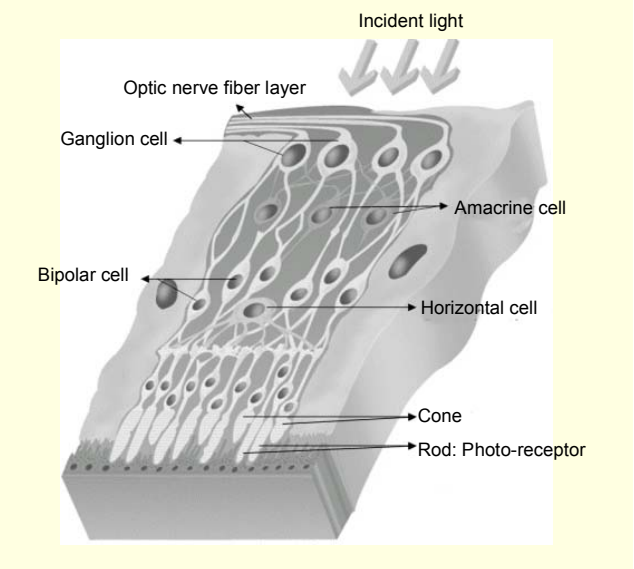

Fig. 1. The structure of a biological retina.

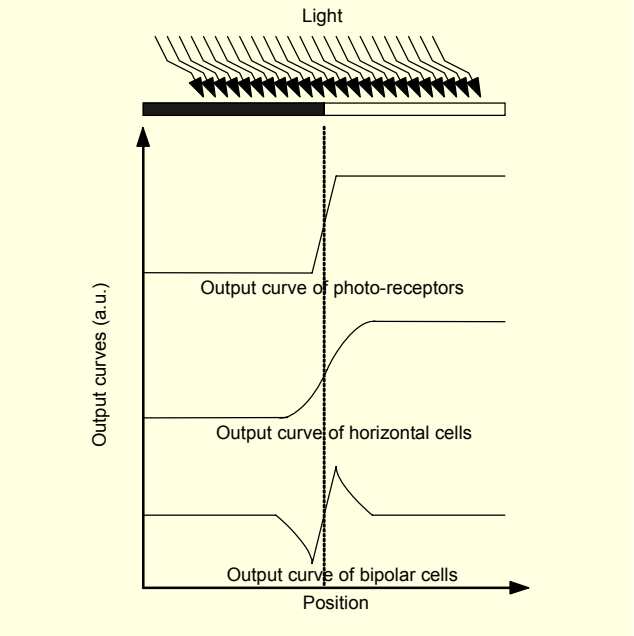

Fig. 2. Simple example of edge detection.

cells. Generally, the gain of the electrical circuit for bipolar cells is constant. In that case, the difference between the outputs of the photoreceptor and the horizontal cell will be the most important factor in deciding the magnitude of an edge.

The major advantage of the retinal structure is the speed of operation for edge detection because all operations which include image capturing, smoothing, and differencing are done in a parallel manner. Another advantage is that each function of the structure is simple enough to realize in an electrical circuit; therefore, the entire system size can be reduced.

2. The Modeling of a Retinal Structure in Electrical Devices

Photoreceptors, horizontal cells, and retinal bipolar cells are the three key elements of a retina embodied in a vision chip for edge detection. First, a raw image is necessary from which to extract edge information. A CCD can be used to sense the incident image in high quality. It requires a special process for fabrication; therefore, it is impossible to embed other circuits for signal processing. This problem of on-chip integration can be solved by using CIS technology. The function of horizontal cells can be embodied by using the resistive network proposed by Mead's research group [2]. All photo-sensors in a bio-inspired vision chip are connected horizontally and vertically through resistive circuits to build the resistive network. The current flows, from a higher-potential area to a lower-potential area, contribute to smoothing. The smoothing is done in a spatially parallel manner; therefore, the mechanism is proper for real-time applications. In this type of vision chip, the characteristic of the resistive network is an important parameter in improving final edge images. We could improve the quality of final edge images by optimizing the resistive network. Detailed explanations will be presented in a later section. The function of the bipolar cells can be embodied by using differential circuits. In addition, noise reduction circuits and addressing circuits are needed for a practical design.

3. Mechanism of Light-Adaptation for Improvement of an Edge Image

The characteristics of a resistive network comprise the key-parameters in improving final edge images. Earlier models of vision chips for edge detection used a single MOSFET or a circuit which has a linear resistive characteristic [7]-[9]. Their results showed that the output or diffusion length was quite varied depending on the illumination. This characteristic is one of the reasons for low quality. This problem can be solved by optimizing the characteristics of the resistive network.

Figure 3 shows an equivalent circuit of a conventional resistive network based on CMOS technology. Source followers, which include the MOSFETs Mp_i, Mp_j, Mpl_i, and

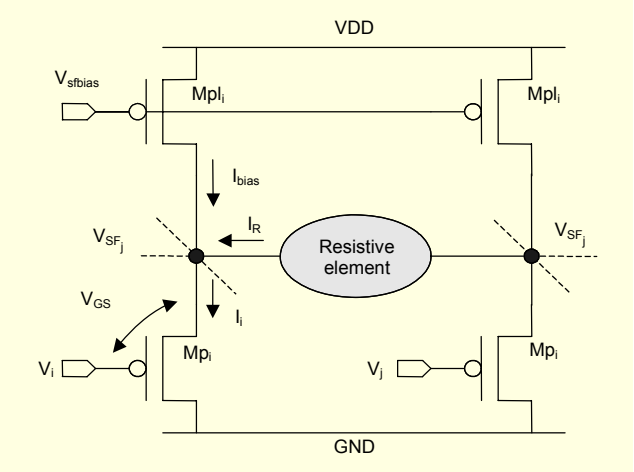

Fig. 3. Equivalent circuit of the resistive network using CMOS technology.

Mpl_j, provide the level-shifted potentials of V_i and V_j, the light-induced voltages. The resistive elements transfer or receive a small portion of the signals from their terminal nodes and generate a spatially smoothed signal. The edge signal can be obtained from the voltage difference of node V_{SF_i} both when the I_R exists and when it does not.

The operation of the circuit was calculated by general MOSFET equations. For ease of calculation, we assumed a one-dimensional resistive network. The second effect due to the diffusion current I_R was ignored. The gate-source potential difference of the Mp_i, V_{GS}, is given by

$$V_{GSwithoutIR} = -\sqrt{\frac{I_{bias}}{\beta}} + V_{th}, \quad (1)$$

$$V_{GSwithIR} = -\sqrt{\frac{I_{bias} + I_R}{\beta}} + V_{th}, \quad (2)$$

where $\beta = \mu_p C_{OX} W/2L$, μ_p is the mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area, W is the gate width, L is the gate length, and V_{th} is the threshold voltage [11]. The gate-source voltage differences of the Mp_i when the I_R exists and when it does not, are represented by $V_{GSwithIR}$ and $V_{GSwithoutIR}$, respectively. The difference between a raw signal ($V_{GSwithoutIR}$) and a smoothed signal ($V_{GSwithIR}$) becomes an edge signal.

Earlier vision chips for edge detection were based on a linear resistive circuit or single MOSFET [7]-[10]. Using (1) and (2), we can determine whether the edge signal varied due to the I_R variation. In Fig. 4, (a) and (b) are examples using a linear resistive circuit. In the case of using a MOSFET, the diffusion current (I_R in Fig. 3) increases in proportion to the square of the gate-source voltage difference; thus, the edge variation becomes larger than that of the linear resistive circuit.

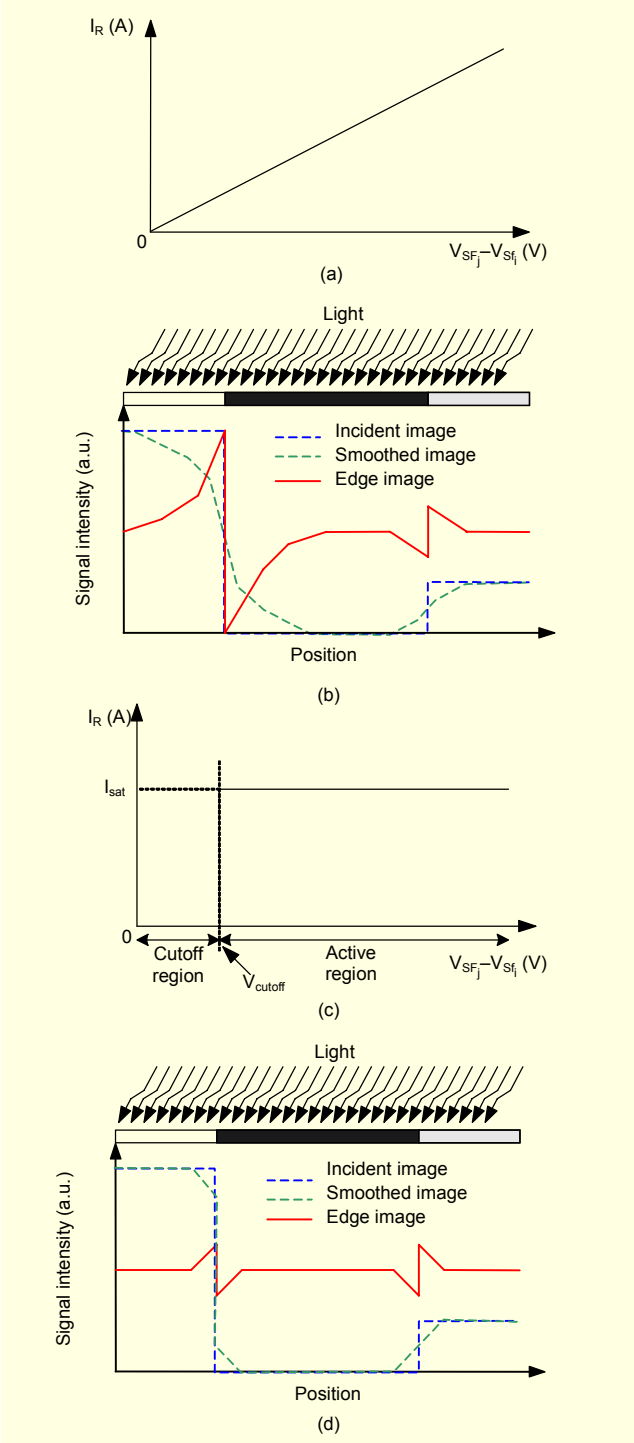

Fig. 4. Mechanism of the light-adaptation: (a) I-V characteristics of a linear resistive element, (b) expected output signals without the light-adaptation, (c) I-V characteristics of the proposed resistive element for light-adaptation, and (d) expected output signals with the light-adaptation.

In general, this circuit loses edge information due to the difficulty of biasing. A detailed explanation with simulation results will be given in the next section.

This output variation problem can be overcome using the saturating resistive element, as shown in Fig. 4(c). In the cut-off region, the edge signal should be 0 because (2) is equal to (1). Otherwise, in the active region, the edge signal becomes a constant value because the I_R becomes a constant value of I_{sat}. The current flow limitation can be used to determine the constant output and constant diffusion length, which is called light-adaptation. The expected signals are shown in Fig. 4(d). On the array, there is a two-step light input. In general, the output and the diffusion length vary according to the pixel-to-pixel potential difference when using a linear resistive element as shown in Fig. 4(b). On the other hand, by using the element shown in Fig. 4(c), the output and the diffusion length are maintained at a constant value. We can control the output swing of the edge signal by changing I_{sat} and V_{cutoff}.

Two simple approaches can be thought to extract the edges from the output of the chip. One, so-called peak-detection, is to detect its peak. However, this approach requires additional signal processing, which increases the cost of system size, power consumption, and time. If this method is used, our approach does not have much advantage compared with the results using other resistive circuits. The other approach is level-detection. Like a digital signal, the edge can be defined as a particular voltage. When results of a linear resistor and a MOSFET are applied in this method, the varied output peak and the varied diffusion length make it hard to define the edge position. Compared with that, our approach shows improvement without cost increment.

III. Circuit Design

1. Saturating Resistive Circuit

It is difficult to realize the proposed resistive element shown in Fig. 4(c) using CMOS technology because of its discrete I-V characteristic. Nonetheless, we realized the light-adaptation using a saturating resistive circuit, which is similar to the proposed saturating resistive element. Figure 5 shows an equivalent circuit schematic of the saturating resistive circuit. The source and drain of the MOSFET MDM are the two terminal nodes for a resistive element. The MOSFETs M1, M2, and Mbias organize a self-biasing circuit for the constant gate-source potential difference of the MDM. The reason for the interconnection between the gate and the body of the MDM is to reduce the body effect. The fixed body potential of the MDM was the most significant parameter of the current variation according to the source potential. The difference in the current level between the simulation and the experimental results does not significantly affect the final output image because the signal level can be controlled by V_{bias} and another

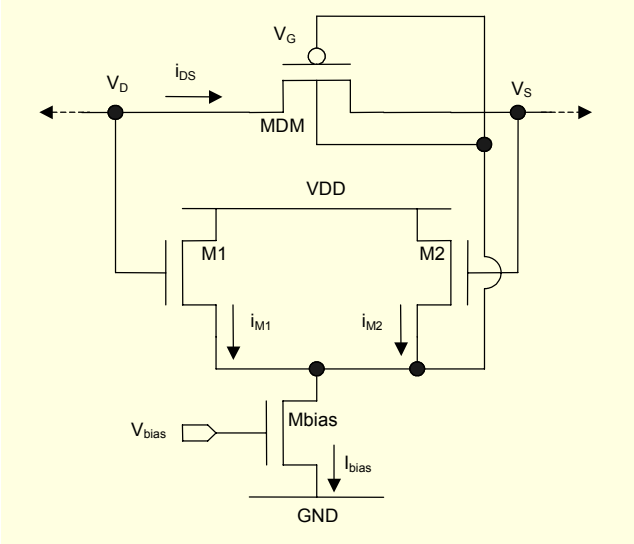

Fig. 5. Schematic of the saturating resistive circuit.

resistance (which is controlled by HSFbias, shown in Fig. 7) in the resistive network can compensate it. The most important parameter for an improved edge image is the shape of the current through the MDM. To take a proper output swing and a diffusion length, the current can be controlled by V_{bias}. To get the proper current flow through the MDM, all MOSFETs should operate in the subthreshold region. The current through the Mbias is given by

$$i_{bias} = I_O \exp(\frac{V_{bias}}{\xi V_T}), \quad (3)$$

where ξ is a non-ideality factor and $V_T = kT/q$ [11]. If V_S is bigger than V_D, i_{M2} will be much larger than i_{M1}, because the current flow through the M1 and the M2 exponentially increases according to the gate-source potential difference. Under this condition, the gate-source potential difference of the MDM can be calculated by

$$V_{GS\min} = -V_{bias}. \quad (4)$$

Otherwise, when the potential V_S and V_D are the same, the current that flows through the M1 and the M2 assumes the same value, that is, $i_{bias}/2 = i_{M1} = i_{M2}$. Therefore, the gate-source potential difference of the MDM, which is the maximum potential difference, is given by

$$V_{GS\max} = -V_{bias} + \xi \cdot V_T \cdot \ln 2. \quad (5)$$

However, in real conditions, V_{GSmin} and V_{GSmax} are smaller than the calculated values because of the body effect at the M1 and the M2.

Figure 6 shows characteristic curves of the saturating

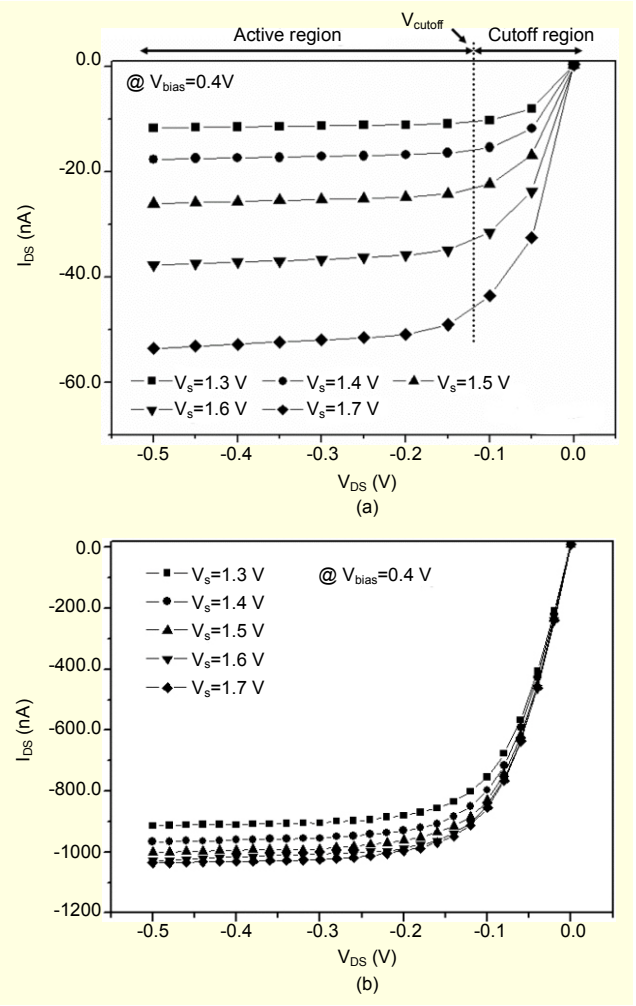

Fig. 6. Characteristics of the saturating resistive circuit: (a) simulated and (b) measured data of I_{DS}-V_{DS} characteristic.

resistive circuit. For the experiments, we fabricated a 5×5 array of saturating resistive circuits according to the previously described CMOS process. Each saturating resistive circuit was 13.5 μm ×17 μm. Figure 6(a) and (b) show our simulation and experimental results. The V_{DS} varied from -0.5 V to -0.12 V in the active region and it varied from -0.12 V to 0 V in the cut off region. The current variations according to the terminal node voltages were approximately 500% in the simulation and approximately 20% in the experiment. The current variation resulted in a varying output swing which is the reason for falling-off of quality in a final edge image. The results show that experimental results are better than the simulation results in terms of higher quality of an edge image. The differences between the simulation and the experimental results are attributable to inaccurate simulation parameters in the subthreshold region and to the inaccurate bias voltage, V_{bias}. Although the simulation and experimental results are different from the proposed saturating resistive element in both

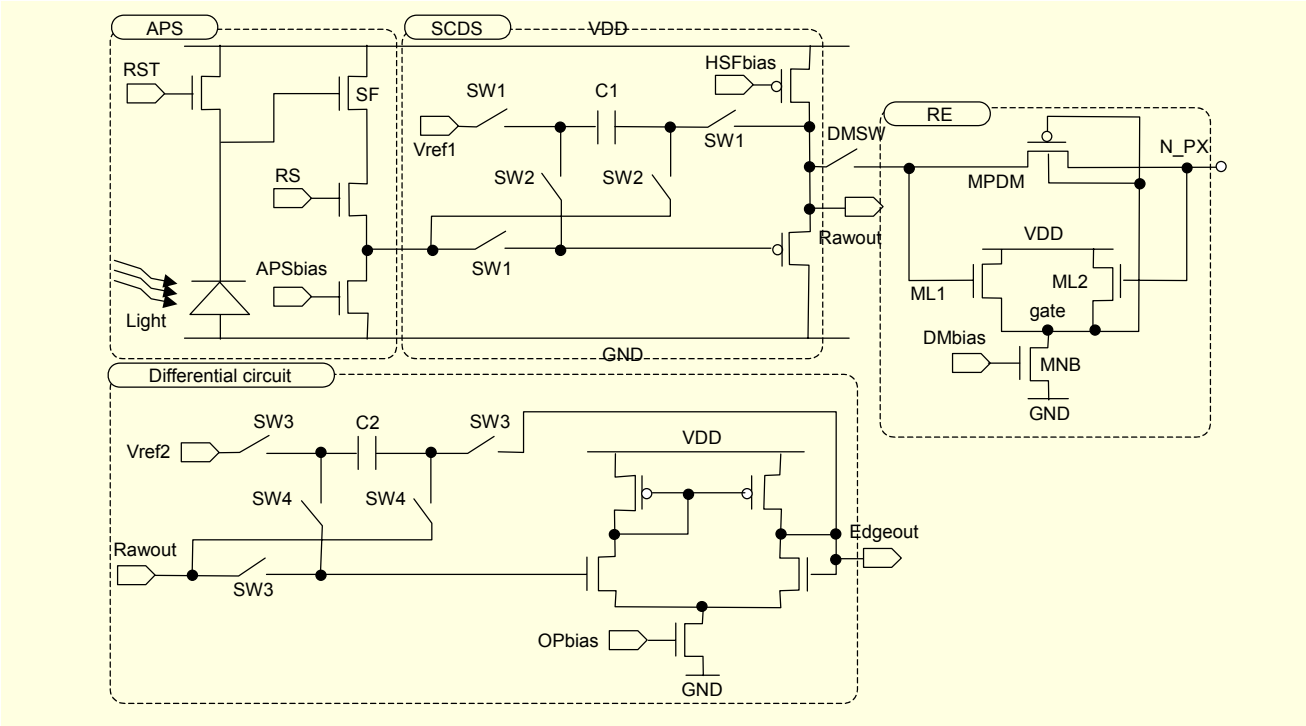

Fig. 7. Schematic of the unit pixel circuit.

magnitude and variation, the shapes are similar to the proposed element. Thus, the proposed circuit can be used for light-adaptation.

2. Unit Circuit

Figure 7 shows a schematic diagram of a designed unit pixel. The circuit contains an active pixel sensor (APS) for image capturing, two simplified correlated-double sampling (SCDS) circuits for reducing fixed pattern noise (FPN) and yielding the difference between raw and smoothed image data, and a saturating resistive circuit which consists of 4 MOSFETs (MDM, ML1, ML2, and MNB). Figure 8 shows a timing diagram to control the proposed circuit. In the Fig. 7, "RE" represents the resistive element.

A three-transistor APS and SCDS were used for image capture and noise reduction, respectively. An APS is an imager in which every pixel includes at least one active transistor. Transistors in the APS may operate as both amplifier and buffer in order to isolate the photo-generated charge from the large capacitance of the common output line. The photodiode capacitance is charged to a reset voltage by turning on the RST. During the integration time, electrons are accumulated in the photodiode capacitance according to the light intensity. After the integration time, the light signal is sampled when the SW1 is turned on. The sampled signal has FPN due to process variation. To reduce the FPN, a correlated-double sampling

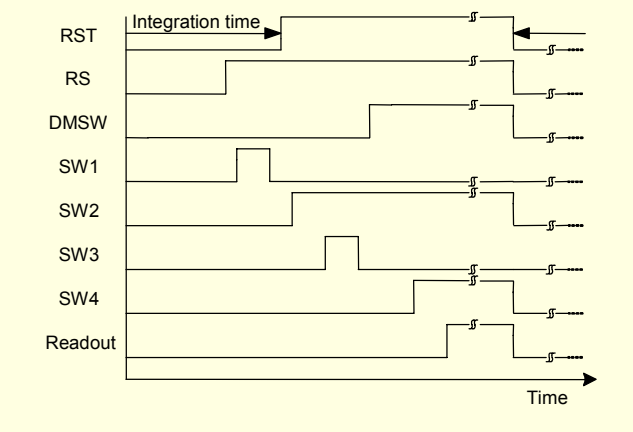

Fig. 8. Timing diagram for control.

(CDS) technique is required.

A noise reduction circuit is also one of the essential circuits for signal processing. To enhance the resolution of a vision chip, the applied CDS should occupy the minimal area. A dominant cause of area consumption of CDS is its capacitors for analog memory. Using SCDS, which was proposed by Kavadias, is very effective for noise reduction [12]. The key advantage of SCDS is that the circuit only requires one capacitor. Therefore, we can easily minimize area consumption. Compared with SCDS, conventional CDSs use 2 capacitors to memorize both the image and reference signals. A detailed operation of SCDS can be found in [12] and [13]. The light signal and reset signal

are sampled when the SW1 and SW2 are turned on, respectively, and then subtracted.

The edge detection circuit uses only one source follower circuit for both raw and smoothed images. Each image can be selected by a switch, DMSW. Because the output node for raw and smoothed images is the same, the FPN can be reduced. The area consumption was also reduced. The differential circuit extracts the edge signal from the raw and smoothed images by switching SW3 and SW4.

IV. Simulation and Experimental Results

1. Simulation

The output swing and diffusion length uniformity are important factors in determining the image quality of an edge image. To verify the improvement of a final edge image using the SRN, we simulated the circuit shown in Fig. 3. For the simulation, we used the simulation program with integrated circuit emphasis (SPICE). Edge images were achieved by differencing the image outputs before and after image smoothing.

Figure 9 shows one-dimensional array simulation results

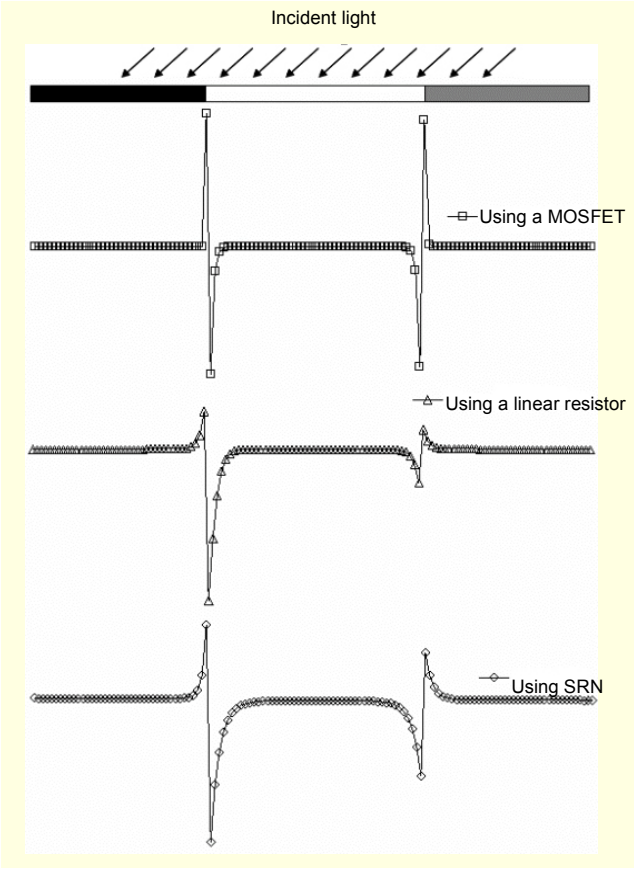

Fig. 9. One-dimensional simulation results.

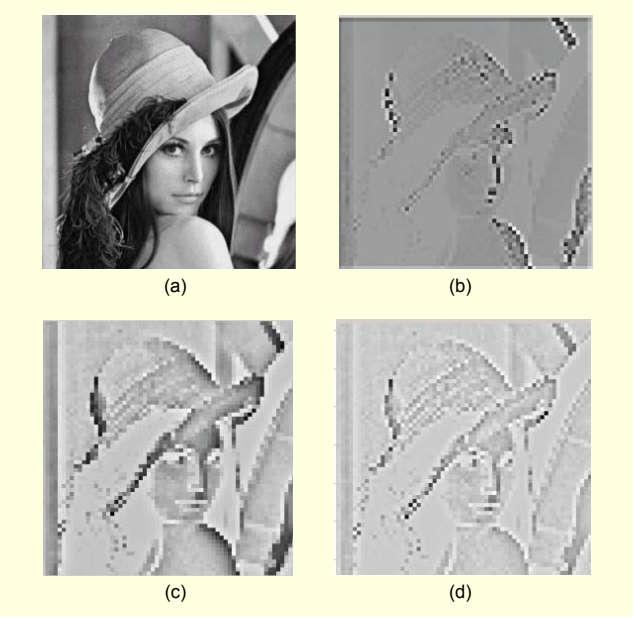

Fig. 10. Two-dimensional simulation results: (a) input image, (b) result using a MOSFET, (c) result using a linear resistor, and (d) result using the proposed resistive circuit.

using various resistive circuits for an incident light having two different contrasts. The result using a MOSFET shows an ideal output, but the output signal is delicately changed with the source potential of the MOSFET. Thus, information from pixels, which does not match with the gate bias voltage, may be lost, as Fig. 10(b) demonstrates. Compared with the result using a linear resistor, we could confirm that the result using SRN shows improvement at the point of output swing uniformity. The reasons for swing variation using SRN may be found in Fig. 6(a). One reason is the saturation current variation; another is that the current linearly increases in the cut off region of the proposed resistive circuit [14].

In Fig. 10, (b), (c), and (d) show the two-dimensional image simulation results from a 64×64 pixel array using a MOSFET, a linear resistor, and a saturating resistive circuit for the resistive element, respectively. The gray scale of these images indicates the output voltage. Black and white mean minimum and maximum voltages, respectively. The result in Fig. 10(b) shows some loss of edge information, because the diffusion current is in proportion to the square of the gate-source voltage difference and each source voltage varied in accordance with the local-light intensity. This means that an individual gate voltage for each unit pixel is required, which is not practical. Compared with the results shown in Fig. 10(b), the edge image shown in Fig. 10(c) is much improved. However, the diffusion current of a conventional resistor is dependent on the pixel-to-pixel voltage difference; therefore, the edge signal varied in accordance with the varied diffusion current. The varied output

signal affects the diffusion length which is directly related to spatial resolution, because the varied signal also affects its neighboring pixels. As shown in Fig. 10(d), we could confirm an output image with a more uniform output swing and diffusion length compared with the image shown in Fig. 10(c).

We confirmed that an improved edge image can be achieved by using the saturating resistive network compared with the other circuits although the proposed saturating resistive circuit does not have the ideal characteristics of the saturating resistive element. The result using a linear resistor for the resistive element circuit was not bad. However, it is not practical to fabricate a linear resistor using the standard CMOS process because of its large size.

2. Experimental Procedures

We fabricated a vision chip with a 160×120 pixel array using a 0.35 ㎛ double-poly four-metal standard CMOS process. The chip size was 5×5 mm^2.

In order to enlarge the resolution, signal processing circuits were separated from the APS array [15]. Conventional vision chips are built using a two-dimensional resistive network for high operation speed and mimicking a more retina-like model. A unit pixel of this kind of chip contains a photodetector, noise suppression circuit, resistive circuit and differential circuit. The noise suppression and differential circuits require capacitors for storage of analog data. Thus, the unit-pixel requires a large area over 100 ×100 $㎛^2$. Due to area consumption, this type of vision chips suffers from a critical lack of resolution. Figure 11(a) shows the structure of a vision chip with a two-dimensional resistive network.

We have tried to solve the problem of low resolution by restructuring circuits for photo-sensing and image processing. Figure 11(b) shows our proposed structure. The signal processing circuit (resistive network) was separated from the image sensor array (APS). Then the signal processing circuit was used in row-parallel. This structure has two advantages and two disadvantages. The advantages are high resolution and low power dissipation. High resolution is caused by the small size of the unit pixel. Lower power dissipation is caused by fewer current paths through the overall chip. The disadvantages are the possibility of data loss and low operation speed. Data loss can appear at either the horizontal or vertical edges depending on the direction of the resistive network. However, the problem can be compensated when the resolution is sufficiently improved. The other disadvantage of low operation speed can be a problem when the illumination condition is dim because of long exposure time. It can be compensated by using a reset control. Figure 12(a) shows the layout.

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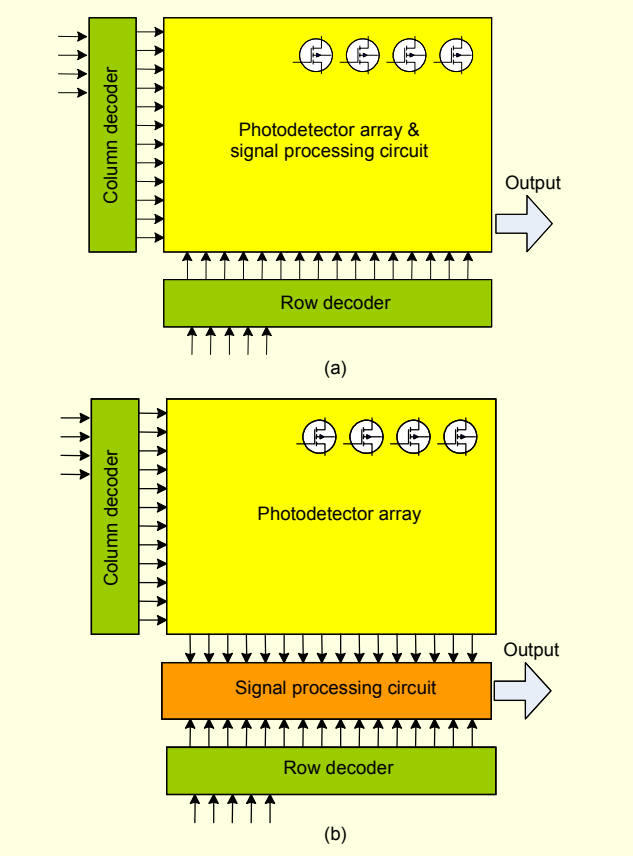
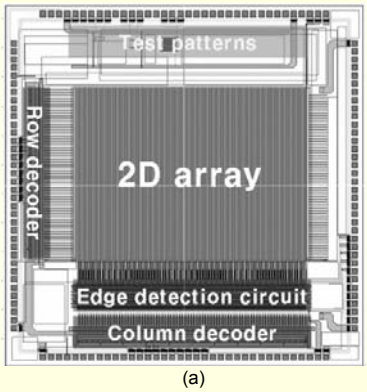


Fig. 11. Two types of circuit arrangement: (a) a vision chip which contains 2-dimentional resistive network and edge detection circuit in a unitpixel and (b) a vision chip which separates a signal processing circuit from a unitpixel.

Instrument Company were used to generate control signals and achieve an output signal. An optical lens (focal length of 16mm, f number of 1.4) was mounted in a C-mount format to project an incident image onto the chip surface. Figure 12(b) and (c) show the printed circuit board with the fabricated chip and the measurement setup, respectively.

Figure 13 shows our experimental results. We investigated the fabricated chip under several illumination conditions. In the results of Fig. 13(a), the voltage at the non-edge region was approximately 1.65 V, and the value did not change according to the illumination. At the edge, the chip outputs approximately 350 mV of peak-to-peak voltage swing and 10 mV of FPN were investigated. In dim illumination conditions, the output peak increased due to the linear characteristics of the designed resistive circuit in the cut-off region. According to the increase in illumination, the output peak was saturated. This point can be thought as V_{cutoff}. The output variation according to the illumination was small, compared with previous results [7]-[10], [13]. Actually, the linear characteristic of the proposed resistive circuit helps the vision chip to operate robustly for real edge of an incident pattern can be easily achieved by using



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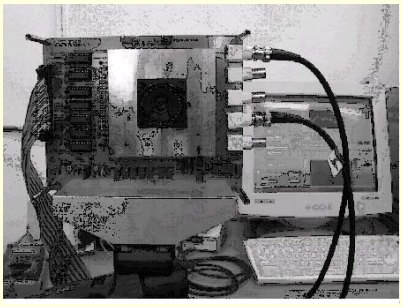

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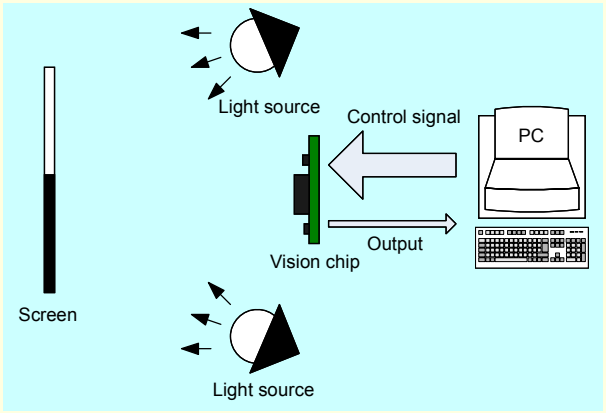
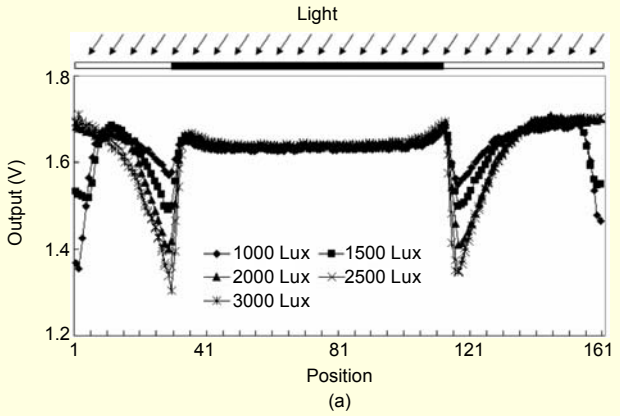


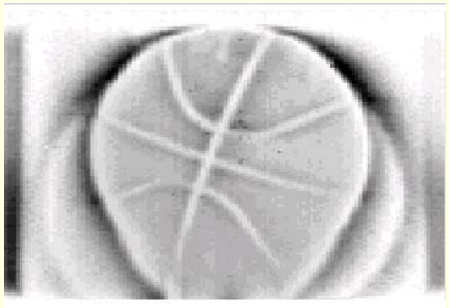
(c)

Fig. 12. Implementation: (a) layout, (b) a picture of the fabricated chip on a PCB, and (c) measurement setup.



(a)

(b)



(c)

Fig. 13. Experimental results: (a) one-dimensional results under various illumination conditions, (b) input image, and (c) output image.

level detection. The values of non-edge and edge voltages were controllable using biases. The output swing and diffusion length were dominantly controlled by DMbias and HSFbias, as shown in Fig. 7.

Although the vision chip worked well, there were a few problems. First, the output image was distorted at the sides of the edge detection circuit. For real applications, this distortion should be carefully considered. Second, both the overshoot voltage and the maximum reference voltage variance according to the brightness were 40 mV. The overshoot voltage might not be detected by using level detection for worse conditions.

Figure 13(b) and (c) are the input and output images, respectively. The gray scale represents the output voltage; black and white represent 1.3 V and 1.7 V, respectively. The analog signal processing of the vision chip is similar to Laplacian filtering. The features of a target object can be easily achieved using our vision chip, and the extracted edge information may be used in various pattern recognitions (such as face, fingerprint, car number, and shapes in general).

V. Conclusion

Bio-inspired vision systems attempt to compute image information. Using a bio-inspired vision system offers several advantages including compact size, high speed, low power

dissipation, and dense system integration. This paper proposed a new approach to light-adaptation and then the mechanism was quantitatively analyzed using a simple model. To achieve light-adaptation, SRN was applied to the vision chip. The characteristics of the proposed edge detection circuit were investigated though simulations and experiments. The results of SRN were compared with other resistive networks consisting of a single MOSFET and a linear resistor. The current results showed that the proposed circuit offers clearer edge images than the others. A vision chip for edge detection with a 160×120 pixel array was fabricated using a 0.35 ㎛ double-poly four-metal standard CMOS process. We investigated light-adaptation using the fabricated chip. From the results of simulations and experiments, we concluded that edge information from an image can be obtained more clearly and effectively by applying SRN to an edge detection vision chip. By employing the proposed vision chip in pattern recognition applications, real-time robust computations with compact hardware can be achieved.

Table 1. Specifications of the fabricated vision chip.

Process	Standard CMOS 0.35 μm double-poly four-metal
Die size	5 × 5 mm^2
Resolution	160 (H) × 120 (V) [pixel] (4:3 ratio)
Unit pixel	20 × 20 μm^2 including metal lines
Supply voltage	3.3 V
Output swing	350 mV peak-to-peak
FPN	10 mV (2.8 % of V_{sat})
Power consumption	Approximately 10 mW (Varies according to the bias conditions)

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