Effects of Interfacial Dielectric Layers on the Electrical Performance of Top-Gate In-Ga-Zn-Oxide Thin-Film Transistors

Woo-Seok Cheong, Jeong-Min Lee, Jong-Ho Lee, Sang-Hee Ko Park, Sung Min Yoon, Chun-Won Byun, Shinhyuk Yang, Sung Mook Chung, Kyoung Ik Cho, and Chi-Sun Hwang

We investigate the effects of interfacial dielectric layers (IDLs) on the electrical properties of top-gate In-Ga-Zn-oxide (IGZO) thin film transistors (TFTs) fabricated at low temperatures below 200°C, using a target composition of In:Ga:Zn = 2:1:2 (atomic ratio). Using four types of TFT structures combined with such dielectric materials as Si_3N_4 and Al_2O_3, the electrical properties are analyzed. After post-annealing at 200°C for 1 hour in an O_2 ambient, the sub-threshold swing is improved in all TFT types, which indicates a reduction of the interfacial trap sites. During negative-bias stress tests on TFTs with a Si_3N_4 IDL, the degradation sources are closely related to unstable bond states, such as Si-based broken bonds and hydrogen-based bonds. From constant-current stress tests of I_d = 3 μA, an IGZO-TFT with heat-treated Si_3N_4 IDL shows a good stability performance, which is attributed to the compensation effect of the original charge-injection and electron-trapping behavior.

Keywords: IGZO, interfacial dielectric layer, electrical stability, thin-film transistor.

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I. Introduction

Thin-film transistors (TFTs) using oxide semiconductors as active layers have shown remarkable performance, including low-temperature processing near room temperature, high transparency for the next version of transparent device applications, and good electrical properties for alternative display backplanes of active-matrix organic light-emitting diodes (AM-OLEDs) and thin-film transistor liquid crystal displays (TFT-LCDs) [1]-[4].

Despite great advances in the fabrication skills for oxide-based TFTs, the lack of explanation for their performance has made it difficult to fully understand their operation or degradation phenomena. For application to industrial products, electrical reliability as well as electrical properties, such as mobility, sub-threshold swing (SS), drain current on/off ratio, and so on, should be guaranteed to the required condition. Therefore, an exact understanding of the degradation behavior of oxide-based TFTs is needed.

The main factors affecting the electrical properties of oxide-TFTs include the active layer, gate insulator, and their interface [5]. Among these, the interface is the most complicated due to two adjacent layers; therefore, it is not easy to extract any physical parameters. Chang and others reported that an $Al_2O_3/HfO_2/Al_2O_3$ multilayer structure as a gate insulator is effective in suppressing the large charge trap density effect due to the HfO_2 dielectric layer [6]. Although the authors used a top-gate TFT structure, there were no chemical effects on the interface or channel because those multi-layers were made by

conventional sputtering methods. On the other hand, Park and others investigated the effects of a TiO_x (high-k) interfacial layer on the device performance of bottom-gate TFTs with a SiN_x gate insulator as a function of TiO_x thickness, where TiO_x formed by atomic layer deposition (ALD) cannot chemically impact the interface or channel [7]. Similarly, Suresh and others reported that an ATO ($AlO_x + TiO_x$) gate insulator deposited by using an ALD gate insulator showed no hysteresis in the transfer plots, while SiN_x formed by plasma enhanced chemical vapor deposition (PECVD) had a large hysteresis in bottom-gate oxide TFTs [8]. Because there are many kinds of gate insulators, processing methods, and possible device structures, it is not easy to fabricate stable oxide-TFTs with excellent electrical properties. However, one possible method is to make an interface without physical collision processes, related with many defect states, and causing severe electrical instability. Moreover, a top-gate TFT structure with chemically processed-dielectric layers will become a preferable scheme [9].

In this work, we investigate the effects of interfacial dielectric layers (IDLs) on the electrical performance of oxide-TFTs fabricated at low temperatures below 200°C. We will investigate both device structures and dielectric materials in order to elucidate the relationship between an interface (between IDL and IGZO) and TFT properties.

II. Experiments

We fabricated top-gate thin-film transistors of the staggered structure type without an additional passivation process for excluding the environmental effects of gases or water vapors [10]. Glass substrates coated by ITO thin films (t = 150 nm) could be obtained via two-step deposition processes to guarantee good surface roughness after ITO-etching, which can be optimized for use in obtaining source/drain electrodes of thin-film transistors [11]. For the low-temperature processing, an IGZO target with a composition ratio of In:Ga:Zn = 2:1:2 (atomic ratio) was chosen, which was made by Advanced Nano Products Corp. (4 inches, 99.99% purity). The channels were formed by the same method as one used in an earlier paper [12], where the gas ratio was 15% O_2 in an Ar and O_2 mixture, and the RF power was 200 W. An Al_2O_3 layer was used as a gate insulator (t =180 nm), which was formed by ALD at 150°C. Between two IDLs, the Al_2O_3 was obtained by ALD at 200°C, while the Si_3N_4, was formed by plasma-enhanced chemical vapor deposition method (PECVD) using SiH_4, N_2 and NH_3 gases at 200°C, 900 mTorr. The thickness of each IDL was 10 nm. The gate electrode was made by Pt (t =100 nm) using both the sputtering method and the image-reversal process of photo-lithography. The basic pattern size was 40 μm (width) × 20 μm (length). The device performance was electrically characterized using an Agilent 4156C semiconductor parameter analyzer.

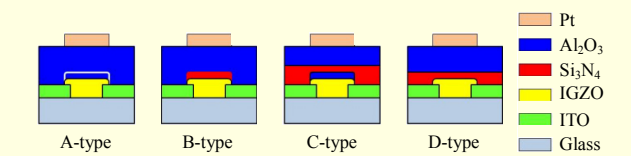

Fig. 1. Schematics of the A-, B-, C-, and D-type IGZO-TFTs.

To elucidate the impact of the IDL on the device performance, four different device structures were manufactured as shown in Fig. 1. In the A- and B-type structures, IDLs were consecutively formed on IGZO channels. After a photo-lithography process they were etched out at the same time using an HF in water solution (1000:4 diluted in water). In the C-type structure, another Si_3N_4 layer was deposited on the patterned channel plus the Al_2O_3 IDL. After that, the Al_2O_3 gate insulator was formed continually. In the D-type structure, the Si_3N_4 IDL was formed on the patterned-IGZO channel, where the surface of the channel was directly exposed to a photo-resist and resist-remover (such as acetone) during the channel patterning process.

III. Results and Discussion

1. Electrical Properties with Various Device Structures

Figures 2(a) to (h) show the electrical transfer plots of the four types of devices mentioned previously. Figures 2(a), (c), (e), and (g) are the electrical transfer plots of A-, B-, C-, and D-type TFT after the fabrication of the devices, while Figs. 2(b), (d), (f), and (h) show the results from the post-annealing at 200°C for 1 hour in an O_2 ambient, respectively. The highest mobility could be obtained by the A-type TFT, while the lowest was obtained by the D-type TFT. During the post-annealing process, there were no major changes in mobility in each type of TFT. Recently, Lim and others reported that the interface roughness between the IGZO channel and the gate insulator affected mobility [13]. On the other hand, there were dramatic decreases in SS: from 0.43 to 0.22 in the A-type TFT, from 1.29 to 0.29 in the B-type TFT, from 0.39 to 0.15 in the C-type TFT, and from 0.66 to 0.29 (V/decade) in the D-type TFT. Jeong and others reported that the SS value is closely related to the density of the trap states near the interface [14]. From this point of view, the post-annealing process could improve the near-interface character by reducing trap states. On the other hand, as shown in Figs. 2(a), (c), and (g), the large changes in the turn-on voltage and the hysteresis with an increasing drain voltage appeared in the Si_3N_4 IDL devices rather than in the Al_2O_3 IDL. The shift of V_{on} during the measurement may be

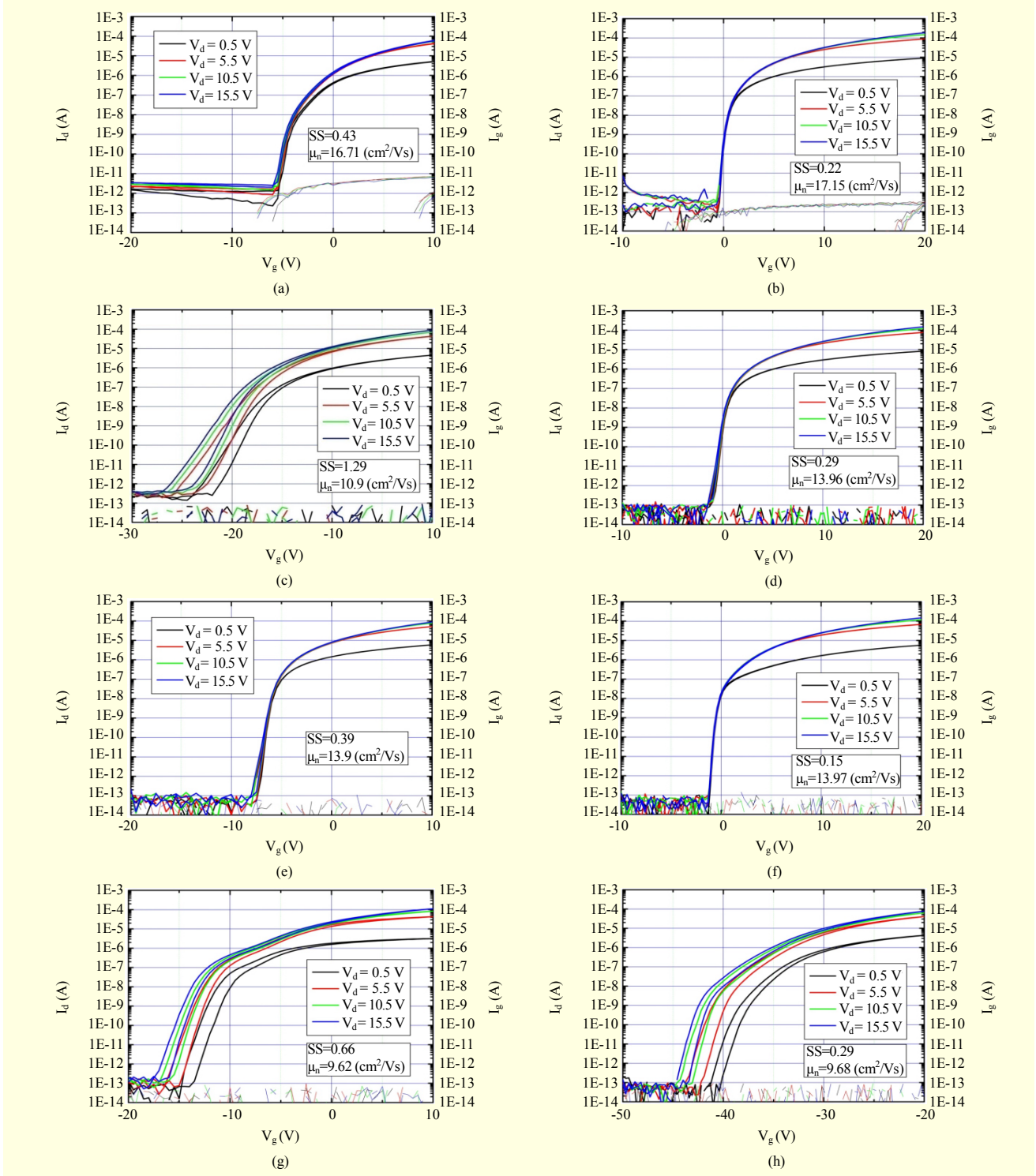

Fig. 2. DC transfer characteristic [log(I_d)-V_g] and gate leakage current [log(I_g)-V_g] curves of IGZO-TFTs, where (a), (c), (e), and (g) show the results of A-, B-, C-, and D-type TFT before annealing, while (b), (d), (f), and (h) show the results after annealing at 200°C for 1 hour in an O_2 ambient, respectively.

attributed to unstable bonding states in the interface between ILD and IGZO, while the clockwise hysteresis resulted from the charge-trapping [5].

Unlike the B-type TFT in Figs. 2(c) and (d), the turn-on voltages of the D-type TFT in Figs. 2(g) and (h) did not converge even after the post-annealing process. To make

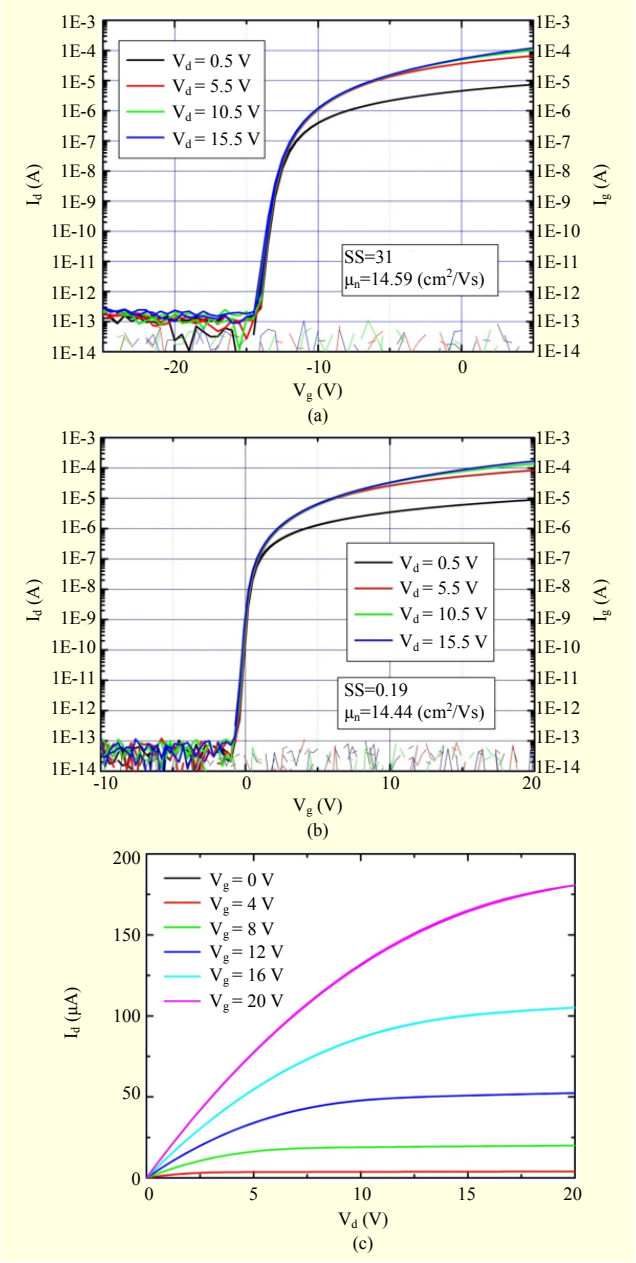

Fig. 3. DC transfer characteristic [log(I_d)-V_g] and gate leakage current [log(I_g)-V_g] curves of the B-type TFT with post-heat-treated Si_3N_4 IDL, where (a) and (b) show the DC transfer characteristic [log(I_d)-V_g] and gate leakage current [log(I_g)-V_g] curves, before annealing and after annealing, respectively, and (c) shows the output curves [I_d-V_d] of (b).

matters worse, the V_{on} of Fig. 2(h) moved to the negative direction, while those of the other three types of devices went to 0 V. This behavior presumably means that Si_3N_4 deposition on the patterned IGZO channel caused permanent damage to the interface, and the post-annealing process worsened it. Because the D-type TFT with the Al_2O_3 IDL made no large differences in electrical properties after the annealing process (not shown in this paper), it is related to the unique phenomenon of Si_3N_4 IDL.

2. Annealing Effect of Si_3N_4 IDL

To estimate the interface states, various annealing tests on the Si_3N_4 IDL in the B-type TFT were carried out. From the first test, the continual annealing at 200°C for 1 hour in an O_2 ambient was processed right after the Si_3N_4 deposition. The results are shown in Fig. 3, where Fig. 3(a) is related to the transfer characteristics of the B-type TFT after fabrication of the device, and Figs. 3(b) and (c) show the transfer and output curves after the post-annealing. Figure 3(c) indicates that they follow the classical MOSFET theory with a saturation region with no contact problems. Compared with Fig. 2(d), the B-type device with heat-treated Si_3N_4 IDL in Fig. 3(b) showed a slightly high mobility and low SS. In Fig. 3(a), the shift of V_{on} with the increasing V_d disappeared, causing a large difference from Fig. 2(c). This means that the interface between the Si_3N_4 IDL and the IGZO channel was remarkably improved.

One reason is the reduced unstable bond states such as Si-based broken bonds and hydrogen-based bonds. The behavior could be clearly evidenced by using a negative bias stress (NBS) test. Moreover, the negative shift under the NBS with time is related to hole-trapping, responding to the hole-trap sites at the interface and near the surface of the IGZO channel. Recently, Shin and others suggested that, under illumination, an enhanced negative shift during an NBS is closely related to the hole-trapping in the interface of the ZnO-TFT [15].

Figures 4(a) and (b) show the results from NBS tests on the same devices in Figs. 2(d) and 3(b), respectively, where the test conditions were V_g= -20 V and V_d=0.5 V. The shift of threshold voltages in Figs. 4(a) and (b) were -2.77 V and -0.58 V, respectively. The B-type TFT with heat-treated Si_3N_4 IDL was more stable than that with non-heat-treated Si_3N_4 IDL, meaning that the defect sources are closely related to the hole-trapping behavior. In other words, in the B-type TFT in Fig. 2(d), the interface between Si_3N_4 IDL and the IGZO channel had more Si-based dangling bonds and broken hydrogen bonds than that in Fig. 3(b) did.

3. Electrical Instability with Time

Except for the D-type TFT, various electrical stress tests on the other types of TFTs were carried out to evaluate which type of TFT is the most appropriate for a low-temperature IGZO-TFT structure below 200°C. Figure 5 shows the results from the constant bias stress (CBS) tests on the A-, B-, and C-types of TFTs mentioned previously, where the B-type TFT used a heat-treated Si_3N_4 IDL as shown in Fig. 3(b). Among the three

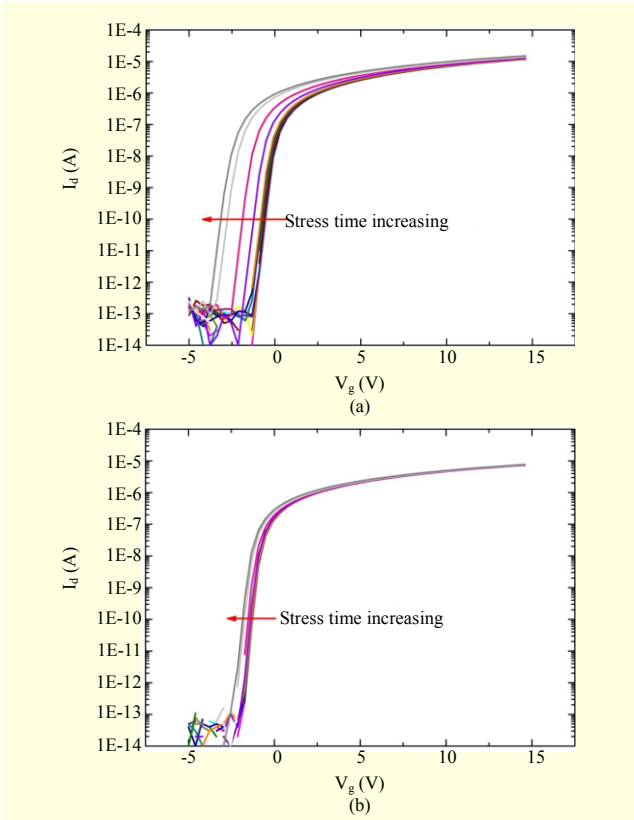

Fig. 4. Shifts of the transfer plots during the NBS test on B-type TFTs, where (a) is related to Fig. 2(d), while (b) is related to Fig. 3(b). The test conditions were V_g= -20 V and V_d=0.5 V.

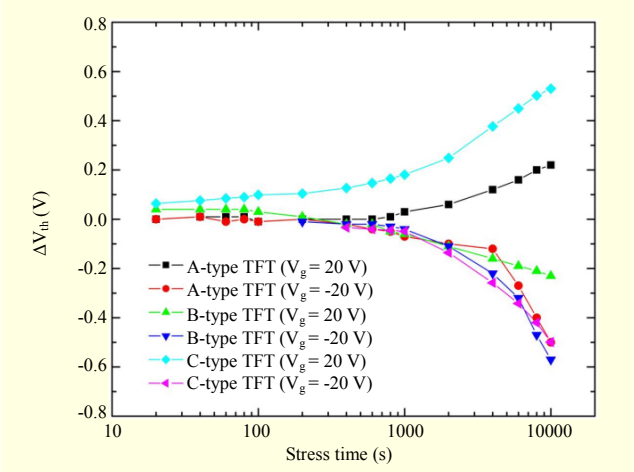

Fig. 5. Results from the CBS tests on A-, B-, and C-type IGZO-TFTs, where the test conditions were V_g=20 V and V_d=0 V for the positive bias test, while those for the negative bias test were V_g = -20 V and V_d = 0 V.

types of TFTs, there was some difference in NBS (V_g= -20 V) with time, namely, a 0.5 V to 0.6 V shift in the threshold voltage (V_{th}) in the negative direction after 10,000 sec.

In a positive bias stress (PBS) (V_g = 20 V), however, there

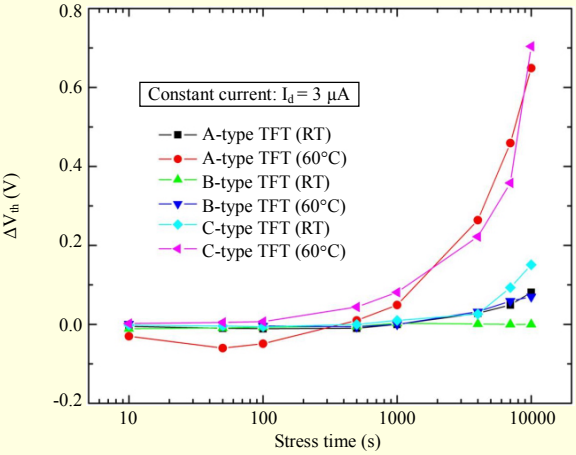

Fig. 6. Results from the CCS tests of I_d = 3 μA on A-, B-, and C-type IGZO-TFTs at room temperature and 60°C.

were large differences. The V_{th} of the C-type TFT showed a 0.54 V shift in the positive direction, while that of the A-type TFT was 0.22 V. It is more interesting that the transfer plot of the B-type TFT moved toward the negative direction even under a PBS test. It is likely due to charge-injection sources more than electron-trapping ones. Some charges may be generated from the imperfect interface between the IGZO surface and Si_3N_4 IDL, while others could be related to H^+ carriers from the Si_3N_4 layer. However, the dominant mechanism will be elucidated by further systematic experiments.

Figure 6 shows the changes of threshold voltages under a constant current stress (CCS) of I_d = 3 μA. The A- and C-type TFTs showed similar results from the CCS with time at both room temperature and 60°C. The insertion of the Si_3N_4 layer (t = 10 nm) between the Al_2O_3 IDL and Al_2O_3 GI did not affect the electrical instability of the IGZO-TFTs. Note that the most stable TFT was the B-type under the CCS even at 60°C .

From the CBS and CCS, the small shift of V_{th} in B-type TFT was commonly related to compensation behavior between electron injection from the imperfect bonding character and electron-trapping. A properly controlled interface between Si_3N_4 and IGZO could maintain the TFT stability.

IV. Conclusion

In this study, the effects of the interface between the IDL and IGZO channel on the electrical properties of IGZO-TFTs were investigated using four types of TFT structures and two types of IDLs (Al_2O_3 and Si_3N_4). The interface was affected by both the IDL process and post-annealing. After post-annealing at 200°C for 1 hour in an O_2 ambient, the sub-threshold swing was greatly improved in most TFTs due to the reduced

interfacial trap sites. From NBS, the degradation sources in the TFT with Si_3N_4 IDL are unstable bond states such as Si-based broken bonds and hydrogen-based bonds. During the CCS (I_d = 3 μA), an IGZO-TFT with heat-treated Si_3N_4 IDL showed good electrical stability, which responded to the compensation behavior of charge-injection and electron-trapping.

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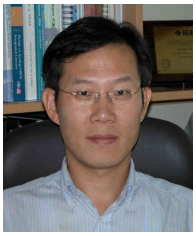

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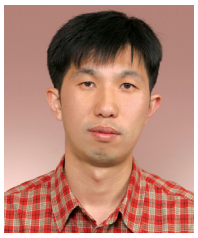

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