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A MONTE-CARLO APPROACH FOR THE ESTIMATION OF AVERAGE TRANSITION PROBABILITIES IN SEQUENTIAL LOGIC CIRCUITS

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This paper presents an efficient and accurate Monte-Carlo approach to the problem of estimating average node switching probabilities in sequential circuits, which are used in average power estimation and reliability analysis of these circuits. Specific error bounds for the proposed estimation method are given at a certain level of confidence. This method is based on the analysis of *paths* in the State Transition Graph (STG) of the circuit and is validated by both theoretical analysis as well as experimental results.

Keywords: Monte-Carlo approach; STG; VLSI circuits; Simulations

INTRODUCTION

There has recently been much interest in the simulation of VLSI circuits for the estimation of their average power dissipation and their susceptibility to cumulative degradation phenomena such as electromigration and hot-carrier degradation. For the simulation of combinational circuits a number of methods have been introduced in the past. Some of them approached the problem at the transistor level and estimated the average current drawn by each individual gate [1,2]. Others proposed a gate level simulation, using the average switching activity in the circuit nodes as a measure of the average power dissipation of the circuit [3–7]. Sequential circuits were considered as a separate problem [8–10] as the combinational

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approaches were not readily extendable. However, the complexity of the derived algorithms was high and no simulation results for large sequential circuits were given. The major obstacle for extending the average power (or current) estimation methods to sequential circuits has been the estimation of the probability that a flip-flop output node will go from the logic "1" state to logic "0" and *vice-versa*. This probability is referred to as the output switching probability of the flip-flop. Once the average switching probability can be estimated properly for every flip-flop in a circuit, the problem of average power dissipation reduces to estimating the average power of a combinational circuit. Consider a sequential circuit with N flip-flops. The circuit has 2^N possible states, which have distinct probabilities of occurring. There are also 2^{2N} possible transitions that may occur in each clock cycle, which also have distinct probabilities of happening. When the circuit moves from one state to the next, the flip-flops may change state and consequently there will be a transition on their output node. A first approach to the problem of computing flip-flop output switching probability in sequential circuits was presented [8], however, it did not take into consideration the correlation between the flip-flop input lines and, thus, the obtained power estimation results were not accurate. A comparison of several methods for estimating the average switching probability of the flip-flop output nodes was presented [9]. The first one was the exact method, through solving the Chapman-Kolmogorov equations for discrete time Markov chains. This involves the solution of a system of 2^N equations, and, as it was reported, this method was limited to circuits with fifteen flip-flops or less. The second method was the "line-probability" method, which included the solution of a system of non-linear equations and the use of OBDDs to estimate required probabilities. The average power estimates that were presented were very close to the ones obtained by the exact Chapman-Kolmogorov methods for the circuits presented. However, by ignoring the correlation between the outputs of the flip-flops some error was introduced, which grew with the size of the circuit. No error values were presented for the larger circuits and no upper bound for the estimation error was given. On a per flip-flop basis, the error in the estimation of the switching activity is much larger and even for small circuits it can reach 100% or more. The per flip-flop estimate is much more important than the overall power

estimate because it identifies the parts of the circuit with high power dissipation and allows for some power reducing intervention. Finally, judging from the presented results, the "line-probability" method was applicable to only small sequential circuits (the maximum gate count of all the examples was 657). However, most circuits of industrial interest are much larger than this. In this paper we describe a computationally efficient method for obtaining the average switching activity for synchronous sequential circuits with high accuracy by using Monte-Carlo simulation at the logic gate level. The accuracy obtained is to within 10% of the actual switching probability value for a particular node at a 95% level of confidence or better. This is achieved by introducing the notion of "paths" in the State Transition Graph (STG) of the circuit, which efficiently scans the sample space that has both the primary inputs and the initial state of the latches as variables. This results in a two step approach, in which the average switching probability being estimated along a single "path" in the first step, and over several "paths" in the second. The validity of this method has been explained theoretically and validated by experimental results. The acceptable error can be set by the user at different values and at different confidence levels, resulting in a different number of required samples in each case. Another significant attribute of this approach is that it can be efficiently applied to even the largest benchmark circuits (ISCAS 89 [11]) and that it can be coupled with any of the existing methods for estimating the average power dissipation of combinational circuits either at the gate or at the transistor level. As an example, the iProbe-c simulator [12] has been used to estimate the average power dissipation of the ISCAS 89 benchmark circuits. The results presented have been geared towards high accuracy rather than speed. Even so, the simulation times are in the 30-minute range for even the largest circuits.

THEORETICAL FOUNDATION

The circuit model that will be used in this paper is the one in Figure 1. There are two distinct blocks, one containing the flip-flops (the "sequential logic" part of the circuit) and the second containing the logic gates that comprise the combinational part of the circuit. The

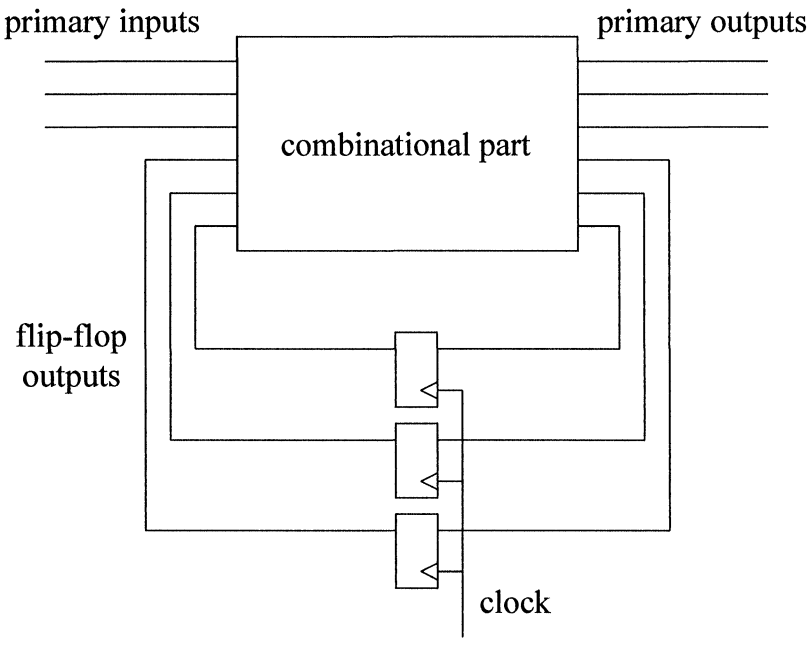

FIGURE 1 The sequential circuit model used.

nodes of interest are the ones termed "flip-flop output nodes" and the analysis will focus on determining the accurate switching probabilities for these nodes. We assume: (a) the circuit can be at any state after power up with equal probability, (b) there are no glitches at the outputs of the latches, and (c) all latches reach a steady state before their next state is allowed to enter into the combinational logic part. All of the above are reasonable expectations from a well-designed sequential circuit. Furthermore, the above assumptions permit the estimation of the power dissipated by the latches separately from the rest of the circuit (the combinational part) and limit the number of times the output of a latch can switch in one clock cycle to at most once. The latter is a critical part of the ensuing study.

Initial State Probability Analysis

A first and intuitive attempt to estimate the average switching probability at the output of the latches would be to set the latches

to some initial value and then to apply a number of random vectors to the circuit's primary inputs and observe the output state of the latches for every clock cycle, counting the number of times the outputs went from logic "1" to logic "0" and *vice-versa* and then dividing that number with the total number of vectors applied, the same way as a combinational circuit might be treated. This is, however, not enough since the results are biased by the initial state of the circuit, before simulation started. This makes the samples correlated and, thus, no inference can be drawn from them. Furthermore, a very small and connected part of the STG is sampled, which can in the general case be not connected. Consequently, further analysis is required. By observing the Boolean expressions for the value of the next state of the latches, it can be deduced that they are a function of not only the primary inputs but of the present state of the flip-flops as well. Therefore, the space that needs to be searched by a random search becomes much larger. However, a Monte-Carlo search is invariant with the size of the input space, meaning that the number of inputs to the scanned function does not affect the number of samples that need to be taken. But even with that taken into consideration, it is still impossible to generate the required input vectors because the probability of the latches being at the present state is not known. Thus, an experiment in which spanning of all variables occurs cannot be created (*i.e.*, assign a random state to the latches and the apply a random input pattern) because it is heavily dependent on the probabilities assigned to each state of the latches. The dependence on the initial state probabilities could be alleviated if it can be proven that the stochastic processes which describe the state of the flip-flops in the time domain are stationary and ergodic. Fortunately, by applying Borovkov's theory of renovating events [13] we can prove that this is true if the latches can be driven to a known state by a sequence of input vectors, which is the definition of initializable circuits [14]. Let us introduce some definitions at this point:

- *Palm probability for discrete-time processes*: In discrete time, the Palm probability is just a conditional probability $E_U^o[Z] = E[Z|U_0 = 1]$.

  For the purposes of this analysis, the Palm probability reduces to the probability of a sequence of input vectors occurring, as the conditional probability is conditioned on the entire sample space.

- *Compatible with the shift*: A stochastic process that is compatible with the shift, is a stationary process.
- *Initializable circuit*: A circuit is initializable if and only if it can be driven to a known state from any initial state, with a finite number of input vectors.
- *Initializing sequence*: A sequence of input vectors that drives a circuit to a known state from every initial state.

Let a system be described by the stochastic recurrence:

$$W_{n+1}^{Y} = h(W_n^{Y}, \xi_n) \qquad n = 0, 1, \ldots \tag{1}$$

where ξ_n is the driving sequence. The theorem [13] we use is the following:

THEOREM *If there exists a sequence of events* $\{A_n\}$ *compatible with the shift and satisfying the condition* $P^o(A_0 > 0)$, *a function* φ *and an integer* m, *such that, on* A_n, $W_n^Y = \varphi(\xi_n, \ldots, \xi_{n+m-1})$, *for all* $Y \in \mathbf{Y}$, *then there exists a stationary sequence* $\{Z \circ \theta^n\}$, *solution of expression* (1), *and such that, for all* $Y \in \mathbf{Y}$, *the sequence converges with strong coupling to* $\{Z \circ \theta^n\}$.

Strong coupling between $\{X_n\}$ and $\{Z \circ \theta^n\}$ implies that $\{X_{n+k}\}_{n \geq 0}$ converges in variation to $\{Z \circ \theta^n\}$. Convergence in variation implies convergence in distribution. For the analysis in this paper, expression (1) is the definition of the next state of a sequential circuit, ξ_n is a stationary and ergodic process as we have assumed that the circuit inputs are driven by random bit patterns, the sequence $\{A_n\}$ is an initialization sequence, which due the random bit pattern applied has a non-zero probability of occurring and drive the circuit to a certain state independent from previous states (*i.e.*, the $W_n^Y = \varphi(\xi_n, \ldots, \xi_{n+m-1})$ condition is satisfied). All the above directly imply that, if the sequential circuit is initializable (*i.e.*, there exists a vector sequence that can drive it to a known state irrespective of the present state), then the random processes describing the state of every node in the circuit, including the states of the latches, converges in distribution to a stationary process. Furthermore, states that are separated by one or more initializing sequences become independent, which means that the node processes are also mean ergodic. Stationarity and ergodicity in combinational circuits is a trivial subproblem of the initializable

sequential circuits. In the case of a non-initializable sequential circuit, no such convergence can be proven in the general case. Consequently, for the initializable circuits, the average switching probability converges to an average value which is independent of the initial state of the circuit and the pathwise average is equal to the time average due to ergodicity. However, the number of samples required is not readily available. By defining the notion of "paths" in the State Transition Graph (STG) of the circuit, a new perspective appears. Instead of running one long simulation with a given initial condition (time average) that may take a long time to converge (dependent on the unknown length of the initialization sequence), we sample through simulations with different initial conditions (pathwise average). As the process is stationary and ergodic, the initial state probability will not bias the estimated average value and, thus, equiprobable initial states can be safely used. In a more mathematical form, suppose that each path is assigned probability $p_{path,i}$ and that the average to which all the paths converge is μ. Then, the average overall the paths would be:

$$\mu_{\text{path,ave}} = \sum_{i=1}^{N} p_{\text{path},i} \times \mu = \mu \tag{2}$$

since

$$\sum_{i=1}^{N} p_{\text{path},i} = 1$$

A path is defined as a sequence of adjoining transitions in the STG. The state from which the first transition in a path originates from is termed the head of the path, while the state at which the last transition arrives to is termed the tail of the path. In the random search that is proposed by this paper the sampling is performed one path at a time. The transition probability samples are the average transition probabilities calculated by the analysis of a "random" path, a path in which the head is randomly selected and so are the vectors applied to the primary inputs. Since we have assumed that the latches can be driven to any state by the proper reset sequence, we assign equal probability to all initial states. A study on the effect of the path head assignment probabilities to the calculated transition probabilities is presented, in which it is shown that

considering all states originally equiprobable is a valid assumption. The transition probability estimation is performed in two steps: (a) estimation of the pathwise transition probabilities, and (b) estimation of the overall transition probabilities.

Step 1 Average along one path A random path is created by first randomly choosing a state as the head of the path and subsequently applying random vectors to the circuit's primary inputs. The transition probabilities observed in this path, call it i, for the output of flip-flop j, are given by the following expressions:

$$plh_{ij} = \frac{\text{Total number of low} - \text{to} - \text{high transitions in path i}}{\text{Total number of clock transitions}}$$

$$phl_{ij} = \frac{\text{Total number of high} - \text{to} - \text{low transitions in path i}}{\text{Total number of clock transitions}}$$

It must also be noted that plh_{ij} and phl_{ij} cannot exceed 0.5. Since the following analysis is valid for both plh_{ij} and phl_{ij}, the symbol p_{ij} will refer to either of the two quantities. The number of vectors needed for achieving a maximum error ε with level of confidence (1-a) is:

$$N \geq \left(\frac{t_{a/2}\sigma}{\eta\varepsilon}\right)^2 \tag{3}$$

where $t_{a/2}$ is the Student-t coefficient for the level of confidence (1-a), σ is the variance of p_{ij} and η its mean. It is useful to make here certain remarks regarding the worst case conditions for N. The random variable p_{ij} follows the Bernoulli distribution. This means that $\eta = p_{ij}$ and $\sigma^2 = p_{ij}(1 - p_{ij})$. Based on this observation it can be deduced that as $\eta \to 0$, N becomes increasingly larger for constant ε. This becomes a problem when η goes below 0.05 since the number of vectors required for adequate approximation becomes prohibitively large. However, a larger amount of error can be tolerated for low transition valued nodes since they contribute little to the overall power dissipation. Furthermore, the error accumulated in this step is compensated for in the second step of the estimation. Another way of expressing the observed transition probability of node j on path i is by the following expression:

$$\eta_{ij,\text{obs}} = \eta_{ij} + E_{ij}(N) \tag{4}$$

where $\eta_{ij,obs}$ is the observed average from the sample, η_{ij} is the true path mean and $E_{ij}(N)$ is the error, which is a random variable with zero mean and variance given as a function of N:

$$\sigma_E = \frac{t_{0.05}\sigma}{4\sqrt{N}} \tag{5}$$

The maximum error observed is for $\sigma = 0.5$ which is the maximum variance that the random variable representing low to high or high to low switching might attain.

Step 2 Average over all paths The second step in the average switching probability estimation algorithm is to average over all paths, with the switching probability estimate of each path being one sample. The setup of the problem seems to be the same as in the first step. However, the samples in the first estimate could only take the values 1 for a transition of the desired variety during that clock cycle and 0 for all other conditions. In this case the random variable can take any real value in the interval [0,0.5]. The approach for estimating the number of paths required for a certain maximum percentile error at a specific level of confidence is the same as in the first step. However, due to the reduction of the range of the random variable ([0,0.5] here *versus* [0,1] in step one), a reduced number of vectors is needed to arrive at the same maximum error at an equal confidence level. The analysis of the mean switching probability is not complete yet. In addition to the error due to the sampling of the switching probabilities of the paths, there is an additional term due to the error in the estimation of the average switching probability for each path (recall Eq. (4)). However, the average switching probability for a node j is given as:

$$p_{j,obs} = \frac{\sum_i p_{ij,obs}}{N} = \frac{\sum_i p_{ij} + E_{ij}}{N} = \frac{\sum_i p_{ij}}{N} + \frac{\sum_i E_{ij}}{N} \tag{6}$$

In the analysis of the pathwise sample we have concentrated just on the first term of the right hand expression in Eq. (6). The second term is the error term that introduces additional error in our calculations. Since this term is a sum of zero-mean normal variables, its contribution to the value of the estimated overall mean switching

probability is zero. However, it contributes an additional absolute error ε_1, which is bound by:

$$\varepsilon_1 = \frac{t_{a/2}\sigma_E}{\sqrt{N}} \tag{7}$$

where σ_E is given by Eq. (5). At this point there is a tradeoff to be made between the speed of the simulation and the accuracy that can be achieved. Table I shows the number of samples required to attain a 10% maximum error at a 95% confidence level. The first column of Table I presents a characteristic sample of average switching probability values that can be encountered in a circuit. The range is from 0.5, which is the maximum switching frequency for a flip-flop output, to 0.01 which, means that the specific node switches once every 100 clock cycles. It is important to stress here that an accurate estimate for the high switching probability nodes is highly desirable, while for nodes with low transition probability a rough estimate should be sufficient since they contribute very little to the overall power dissipation, a notion shared with other work in the area [6]. The second column in the same table contains the number of vectors required to get an estimate of 10% maximum error at 95% confidence level, given that the path samples follow a Bernoulli distribution, which describes the worst case scenario for this analysis. The probability density function is derived by allowing the path mean probabilities to have only two values: zero and 0.5. Thus, the distribution can be created as in following example for a targeted average switching probability of 0.1. In this case 20% of the sample paths are assumed to have switching probabilities of 0.5 and the

TABLE I Required vectors for 10% maximum error at a 95% level of confidence

Transition probability	*Bernoulli distribution*	*Uniform distribution*
0.01	18824	128
0.05	3458	128
0.10	1537	128
0.20	577	128
0.25	384	128
0.30	256	57
0.40	96	8
0.50	1	1

remaining 80% zero switching probability. This kind of distribution, given the continuous nature of the random variable describing the path mean values is highly unlikely to occur. A still conservative, yet more realistic distribution analysis is presented in the third column of Table I. In this case a uniform distribution around the actual mean of the switching probability is assumed for the path samples. This is still very pessimistic, however, the number of the required vectors has been reduced dramatically for the same level of confidence and maximum error. It must be noted that for the actual circuits that were simulated, the distribution of the pathwise switching probabilities was far better than the uniform distribution described here, as the various paths converged towards a common mean, as predicted by the ergodicity of the processes. Table II describes the additional percentile error that is introduced by the path average switching probability error, to the overall switching probability estimate. As can be seen, the additional error is very small and justifies the use of this pathwise approach as convergence to the mean is faster.

Effect of the Assignment Probability of a Path Head to the Estimate

A critical part of the average switching probability analysis of sequential circuits is the assignment of the initial state probabilities, the probabilities by which the heads of the paths are selected. Based on the theoretical results equal probabilities for all the states in the circuit were assumed. However, careful experimental analysis is required to ascertain that this initial selection does not bias the result. In the path

TABLE II Additional error due to the error in the estimate of the pathwise average (length of paths = 400, number of paths = 2000)

Transition probability	*Additional error* (%)
0.01	5.37
0.05	1.07
0.10	0.54
0.20	0.27
0.25	0.21
0.30	0.18
0.40	0.13
0.50	0.11

approach, the initial state of a path, the head, is the only state directly influenced by the state probability assignment, while the rest of the states in the path are influenced by the random vectors applied to the primary inputs of the circuit. Thus, the state of the circuit, after the application of the first random vector, is determined exclusively by the circuit structure. Furthermore, the number of random input vectors in a path is such that any bias induced by the uniform probabilities assumed for path head states is minimized. This is true for all sequential circuits in which the primary inputs can drive the flip-flops to a known state (initializable circuits). However, there are circuits in which the previous statement is not true (non-initializable circuits). In the latter circuits, the uniform probability assumption for the initial states is warranted as the flip-flops can be in any state after power-up. In order to test this approach we simulated all of the ISCAS89 benchmark circuits by the method proposed in this paper, with the probability that a given flip-flop is at logic high value in the head state of a path ranging from 0 to 1 in increments of 0.1. A notion of convergence was also introduced: a switching probability value has "converged" if the difference between the minimum and the maximum values over all the runs was less than a preset threshold t_{conv}. The length of the paths was chosen as 1000, the number of the sampled paths was 1000 as well, and t_{conv} was set to 0.001. Table III shows the number of nodes that converged and did not converge in the ISCAS89 benchmark circuits, along with and indication of whether the circuit is initializable or not according to [14]. It is noteworthy that out of the 28 circuits in Table III (the rest of the circuits were simulated but they were not covered by Wehbeh and Saab [14]), the 25 that converged were also deemed initializable and the three that did not converge were considered non-initializable by Wehbeh and Saab [14], exactly as predicted by the theoretical analysis. A X^2 test shows that there is significant evidence to support that initializable circuits converge (*i.e.*, there is no bias from the uniform selection probability of the initial states) at a confidence level greater than 99.99%. This result conforms with the hypothesis stated in the beginning of this section. In order to explain how the path-averaging method, which is proposed in this paper, can be extended to non-initializable circuits, the circuit of Figure 2 is used.

TABLE III Analysis of the effect of the initial state probability

Ckt name	*Flip-flops*	*Converged*	*Not converged*	*Initializable*
s27	3	3	0	Yes
s208	8	8	0	Yes
s208.1	8	5	3	No
s298	14	14	0	Yes
s344	15	15	0	Yes
s349	15	15	0	Yes
s382	21	21	0	Yes
s386	6	6	0	Yes
s400	21	21	0	Yes
s420	16	16	0	Yes
s420.1	16	5	11	No
s444	21	21	0	Yes
s510	6	6	0	Yes
s526	21	21	0	Yes
s526n	21	21	0	Yes
s641	19	19	0	Yes
s713	19	19	0	Yes
s820	5	5	0	Yes
s832	5	5	0	Yes
s838	32	32	0	Yes
s838.1	32	5	27	No
s953	29	29	0	Yes
s1196	18	18	0	Yes
s1238	18	18	0	Yes
s1423	74	74	0	Yes
s1488	6	6	0	Yes
s1494	6	6	0	Yes
s35932	1728	1728	0	Yes

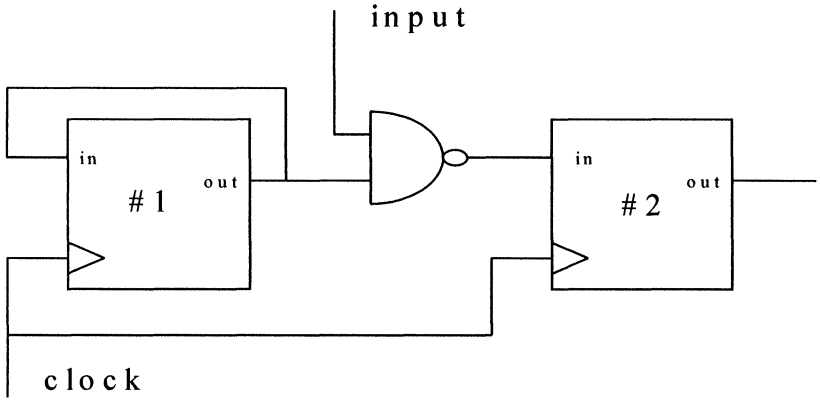

FIGURE 2 Example of a non-initializable circuit.

It is obvious that flip-flop #1 cannot be driven by the primary inputs. In fact, it retains the value it has after power-up throughout the run. Consequently, the switching probability of its output node is zero. If we examine flip-flop #2, we see that if flip-flop #1 is at logic "0", then flip-flop #2 is set at logic "1" and it cannot switch, no matter what the primary input is. If on the other hand, flip-flop #1 is at logic "0", then flip-flop #2 switches in accordance with the primary input. Thus, for the two different initial conditions the output node of flip-flop #2 has a switching probability of zero and 0.5 (which is assumed to be the switching probability of the primary input). As it was assumed, flip-flop #1 is at "0" with probability 0.5 after power-up. This means that the average switching probability at the output of flip-flop #2 is 0.25, since there are only two distinct cases. However, there is a theoretical issue behind this phenomenon. As predicted by the theoretical analysis, the non-initializable circuit of Figure 2 produces non-ergodic processes at the output of flip-flop #2. Thus, we cannot get rid of the initial probability influence and accurately predict the average switching probability based on one single path. Multiple paths are required under the very logical assumption that the circuit can beat any state after power-up with equal probability. Therefore, the path averaging approach can handle non-initializable circuits as well, such as some of the larger ISCAS89 benchmarks (s9234, s13207 *etc.*) Finally, the same argument can be used for circuits with very long initialization sequences that lead to disjoint parts of the STG, and in which convergence is extremely slow.

EXPERIMENTAL RESULTS

The approach described in this paper has been applied to the ISCAS89 benchmark circuits with the path length set to 400 and the path number set to 2000 in order to achieve his accuracy even for very low switching probabilities. With this setup, the switching probability of a node, which has an actual switching probability of 0.01, can be estimated to within 5% at 95% confidence level.

The results of this estimation along with the combinational part of the circuits were then analyzed by the iProbe-c simulator [12] to

estimate the average power dissipation. The runtimes for both the switching probability estimation program and the average power simulator are shown in Table IV. Figure 3 shows a histogram of the average switching probabilities for s1423, a characteristic initializable circuit compared with the histogram of s13207.1, which is not initializable. The power estimates have been omitted since they are implementation dependent.

TABLE IV Simulation times for the sequential and the combinational parts

Ckt name	*Flip-flops*	*Sequential simulation*	*Combinational simulation*
s27	3	38.3	0.1
s208	8	100.8	0.3
s208.1	8	98.4	0.3
s298	14	34.1	0.4
s344	15	93.0	0.7
s349	15	92.7	0.7
s382	21	36.3	0.6
s386	6	72.4	1.1
s400	21	45.5	0.6
s420	16	185.5	0.9
s420.1	16	177.5	0.9
s444	21	37.0	0.7
s510	6	189.8	0.9
s526	21	38.1	0.9
s526n	21	38.2	0.8
s641	19	351.6	3.1
s713	19	350.3	4.1
s820	5	183.9	1.8
s832	5	184.8	1.9
s838	32	345.6	2.9
s838.1	32	345.0	2.8
s953	29	173.5	1.9
s1196	18	160.3	3.8
s1238	18	157.2	4.2
s1423	74	199.3	10.4
s1488	6	107.6	7.1
s1494	6	106.4	7.2
s5378	179	481.3	11.8
s9234	228	456.0	69.0
s9234.1	211	630.9	74.5
s13207	669	775.1	102.5
s13207.1	638	1073.9	109.0
s15850	597	808.5	185.0
s15850.1	534	1261.0	202.4
s35932	1728	1468.5	778.5
s38417	1636	1914.7	854.3
s38584	1452	1383.4	847.4
s38584.1	1426	1656.6	890.8

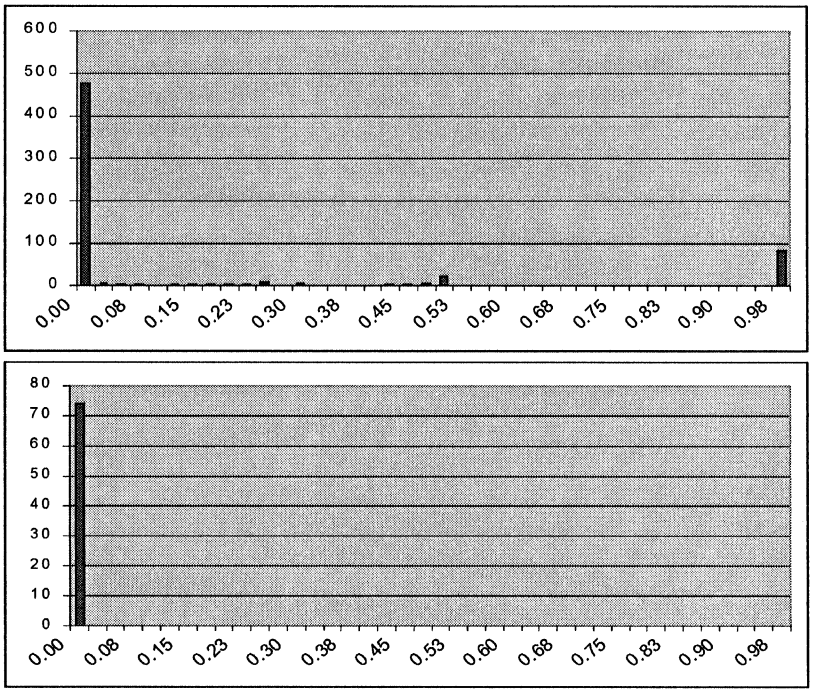

FIGURE 3 The average switching probabilities for s13207.1 (top) and s1423 (bottom).

CONCLUSIONS

In this paper we have presented a method for the accurate estimation of the average switching probability of flip-flop outputs in a general sequential circuit along with its error bounds. The theoretical foundation and the experimental validation have been presented. This approach introduces the notion of paths in the state transition graph of the sequential circuit and employs them in a Monte-Carlo logic simulation approach to estimate the average switching probability. Furthermore, the possible bias on the results by the initial state selection has been alleviated, as shown by theoretical and experimental results, in initializable circuits and special guidelines are set forth for non-initializable ones. It should be noted that this approach achieved high accuracy in relatively little time and with a very small memory overhead.

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