Data Supply Voltage Reduction Scheme for Low-Power AMOLED Displays

Hyoungsik Nam and Hoon Jeong

This paper demonstrates a new driving scheme that allows reducing the supply voltage of data drivers for low-power active matrix organic light-emitting diode (AMOLED) displays. The proposed technique drives down the data voltage range by 50%, which subsequently diminishes in the peak power consumption of data drivers at the full white pattern by 75%. Because the gate voltage of a driving thin film transistor covers the same range as a conventional driving scheme by means of a level-shifting scheme, the low-data supply scheme achieves the equivalent dynamic range of OLED currents. The average power consumption of data drivers is reduced by 60% over 24 test images, and power consumption is kept below 25%.

Keywords: Data supply voltage reduction, low-power, level-shifting, AMOLED.

I. Introduction

Liquid crystal display (LCD) has become the main display technology used in such consumer products as mobile phones, notebook PCs, monitors, and TVs. However, the market share of active matrix organic light-emitting diodes (AMOLEDs) has been significantly on the rise in the arena of small display applications, including mobile phones, and is expected to expand its domain into TV applications on the back of wide color gamut, slim and light design, high contrast ratio, fast response time, and the like [1].

As for AMOLED displays embodied in all consumer electronics, the industry may have to eventually apply low-power technologies to abide with stricter legislation regarding the power consumption of electronic products [2], [3]. So far, several power reduction techniques for AMOLED displays have been put forth, including OLED efficiency enhancement [4], through-current reduction in integrated panel circuitries [5], and the RGBW pixel format [6]. However, reducing the analog supply voltage of data drivers for low-power AMOLED displays has yet to be reported upon. Because the power consumption of data drivers makes a big impact on the high-resolution and high-frame-rate AMOLED displays for TV applications like LCDs [7], a low-power technique for data drivers is indispensable.

II. Data Supply Voltage Reduction Scheme

The AMOLED pixel circuit that has been suffering from the nonuniformity problem should compensate the variation on the threshold voltage of a driving thin-film transistor (TFT). In past research, the nonuniformity compensation has been performed by voltage modulation, current programming, and digital

Manuscript received Mar. 2, 2012; revised June 8, 2012; accepted June 22, 2012.

This research was supported by National Research Foundation of Korea Grant funded by the Korean Government (KRF 2012-0003219).

Hyoungsik Nam (phone: +82 2 961 0925, hyoungsiknam@khu.ac.kr) and Hoon Jeong (hjeong@tftlcd.khu.ac.kr) are with the Department of Information Display and Advanced Display Research Center, Kyung Hee University, Seoul, Rep. of Korea.

http://dx.doi.org/10.4218/etrij.12.0112.0139

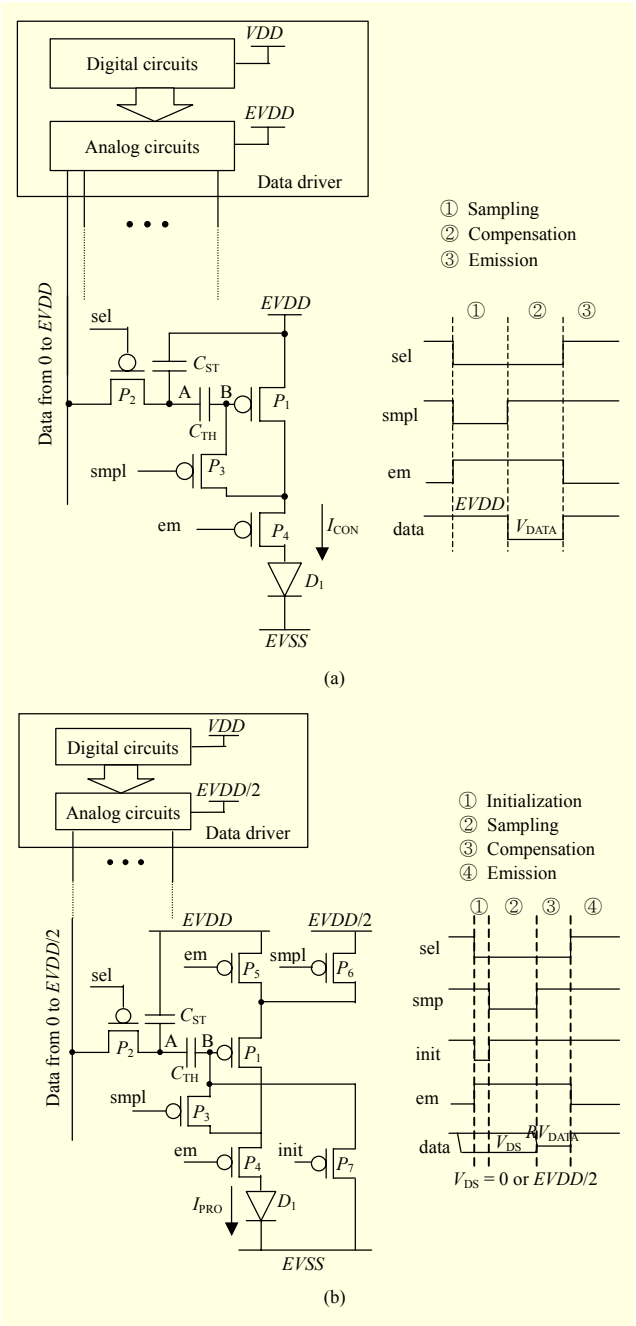

Fig. 1. AMOLED pixel circuits and timing diagrams: (a) conventional circuit with data voltage driven at *EVDD* and (b) proposed circuit with data voltage driven at *EVDD*/2.

driving schemes [8]-[10]. One of the most widely used methods is the voltage modulation circuit depicted in Fig. 1(a) [11]. Only p-channel poly-silicon TFTs have been employed on account of cost and hot carrier issues.

The operation is divided into three periods: sampling, compensation, and emission. Whereas P_1 operates at the saturation region, the other TFTs (P_2, P_3, P_4) are in use at the triode region for switching. During the sampling period, P_2 and P_3 are turned on and P_4 is turned off. Because the current path to an OLED (D_1) is cut off, there is no light output. Node A is charged through the data line at the supply voltage (*EVDD*), and node B, which is the gate terminal of P_1, is settled at $EVDD-|V_{TH1}|$, where V_{TH1} is the threshold voltage of P_1. As a result, the voltage across C_{TH} (V_{AB}) becomes $|V_{TH1}|$. In the compensation period, P_3 is turned off and the target data voltage (V_{DATA}) is applied via the data line to node A. Since node B is floating, the gate voltage of P_1 is set as $V_{DATA}-|V_{TH1}|$. In the emission period, P_2 and P_3 are turned off and P_4 is turned on. The resulting current of D_1 (I_{CON}) is described as (1), which is independent of V_{TH1}:

$$\begin{aligned} I_{CON} &= \frac{\beta_{P1}}{2}\left(EVDD - V_B - |V_{TH1}|\right)^2 \\ &= \frac{\beta_{P1}}{2}\left[EVDD - \left(V_{DATA} - |V_{TH1}|\right) - |V_{TH1}|\right]^2 \\ &= \frac{\beta_{P1}}{2}\left(EVDD - V_{DATA}\right)^2. \end{aligned} \quad (1)$$

Our proposed low-supply scheme modifies the conventional AMOLED pixel circuit of Fig. 1(a) into the circuit of Fig. 1(b) with three additional switching TFTs (P_5, P_6, P_7), which might affect the pixel size and brightness, to reduce the power consumption of data drivers. The operation is divided into four periods: initialization, sampling, compensation, and emission. Particularly, the data signal is provided at the half range from 0 to *EVDD*/2, which leads to a 50% voltage reduction of data drivers' analog supply. As the maximum possible swing magnitude decreases by 50% and the peak power consumption is proportional to its square, a substantial power consumption reduction of 75% can be achieved at the maximum.

The operation is as follows. In the initialization period, node B is connected to *EVSS* through P_7 to ensure that P_1 is turned on at the diode connection at the following sampling period. During the sampling period, the source of P_1 is connected to *EVDD*/2 through P_6 and the voltage of node B (V_B) reaches to $EVDD/2-|V_{TH1}|$. When V_{DS} is defined as the data signal at the sampling period, the voltage across C_{TH} (V_{AB}) is expressed as

$$V_{AB} = V_{DS} - \frac{EVDD}{2} + |V_{TH1}|. \quad (2)$$

In a compensation period, the target data voltage (RV_{DATA}) of the reduced voltage range from 0 to *EVDD*/2 is provided to node A, and V_B is modulated into $RV_{DATA}-V_{AB}$ as (3). Consequently, V_B is obtained by level-shifting RV_{DATA} by $EVDD/2-|V_{TH1}|$ when V_{DS} is 0 and by $-|V_{TH1}|$ when V_{DS} is *EVDD*/2:

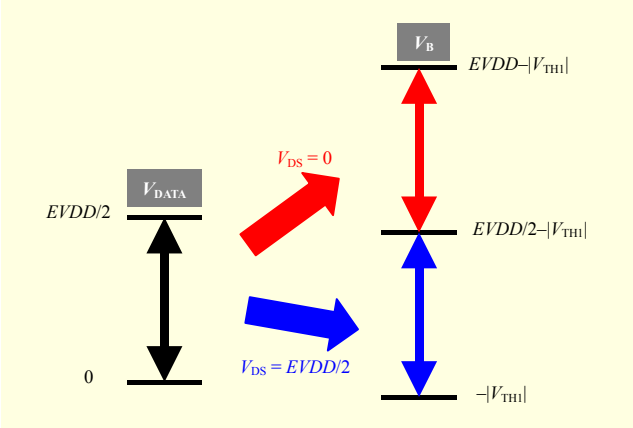

Fig. 2. Level-shifting at V_B according to V_{DS}.

$$V_B = RV_{DATA} - V_{AB} = RV_{DATA} - V_{DS} + EVDD/2 - |V_{TH1}| = \begin{cases} RV_{DATA} - |V_{TH1}| + EVDD/2, & V_{DS} = 0, \\ RV_{DATA} - |V_{TH1}|, & V_{DS} = EVDD/2. \end{cases} \quad (3)$$

The ensuing V_B can cover the full range of $EVDD$ from $-|V_{TH1}|$ to $EVDD-|V_{TH1}|$ by programming V_{DS} with two levels of 0 and $EVDD/2$ even at the half analog supply of $EVDD/2$, as explained in Fig. 2. As a consequence, the uniform OLED current (I_{PRO}) of the equivalent dynamic range is obtained as (4), which is independent of V_{TH1}:

$$I_{PRO} = \frac{\beta_{P1}}{2}\left(EVDD - V_B - |V_{TH1}|\right)^2 = \begin{cases} \frac{\beta_{P1}}{2}\left(EVDD/2 - RV_{DATA}\right)^2, & V_{DS} = 0, \\ \frac{\beta_{P1}}{2}\left(EVDD - RV_{DATA}\right)^2, & V_{DS} = \frac{EVDD}{2}. \end{cases} \quad (4)$$

On the other hand, because the proposed scheme covers two different voltage regions by level-shifting through C_{TH}, any errors on the stored voltage across C_{TH} can degrade the image quality. However, this issue can be resolved by employing separate data mapping tables for two different regions.

III. Simulation Results

1. Circuit Simulation

The proposed low data voltage driving scheme is verified by conducting Simulation Program with Integrated Circuit Emphasis (SPICE) simulation with parameters extracted from fabricated p-channel poly-silicon TFTs. The simulated transfer characteristic of the p-channel TFT is plotted in Fig. 3. The mobility and threshold voltage are 18 cm^2/Vs and –1.6 V, respectively.

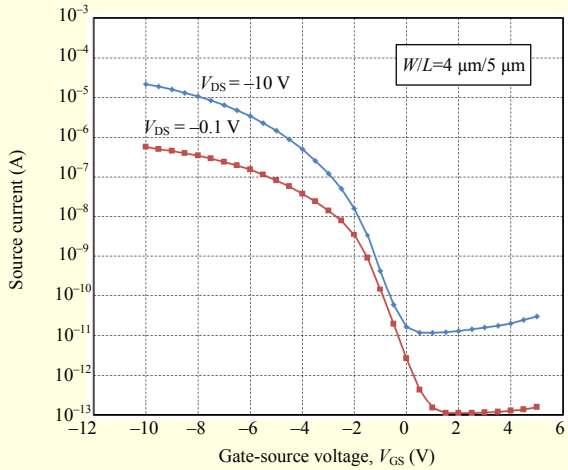

Fig. 3. Simulated transfer characteristic of p-channel TFT.

For the proposed pixel circuit, the size of a driving TFT is 10 μm/5 μm, the size of all the other switching TFTs is 4 μm/5 μm, $EVDD$ is 10 V, $EVSS$ is –5 V, C_{ST} is 0.5 pF, and C_{TH} is 0.5 pF. Figure 4(a) shows the waveforms of control signals, and Figs. 4(b) and 4(c) present the voltage waveforms of nodes A and B in the two cases of V_{DS}=0 V and V_{DS}=$EVDD/2$=5 V. Figure 4(b) shows that when V_{DS} is equal to 0 V, the voltage of node B successfully reaches a higher level than $EVDD/2$ by level-shifting through C_{TH}.

Figure 5 plots the gate voltage of a driving TFT (V_B) regarding V_{DATA} and V_{DS}. Whereas the data voltage has the 5 V range, the range of V_B is doubled to around 10 V, resulting in the equivalent dynamic range of the OLED current.

Finally, Fig. 6 presents the OLED current characteristics of a proposed pixel circuit at the threshold voltage variation of ±0.3 V.

2. Power Evaluation

Because the data lines can be approximated as capacitive loads, the dynamic power consumption of data drivers is expressed by summing the square terms of the output voltage swings [7].

For the conventional scheme of Fig. 1(a), each pixel has two transitions from $EVDD$ to V_{DATA} and from V_{DATA} to $EVDD$. As a result, the dynamic power consumption of conventional data drivers (DP_{CON}) is described as

$$DP_{CON} = k \cdot 2\sum_{i=1}^{3N}\sum_{j=1}^{M}\left(EVDD - V_{DATA}(i,j)\right)^2, \quad (5)$$

where k is the coefficient, $3N$ is the total number of column lines, M is the total number of row lines, and $V_{DATA}(i,j)$ is the target data voltage of an i-th column and j-th row subpixel.

For the proposed scheme, the power can be estimated from

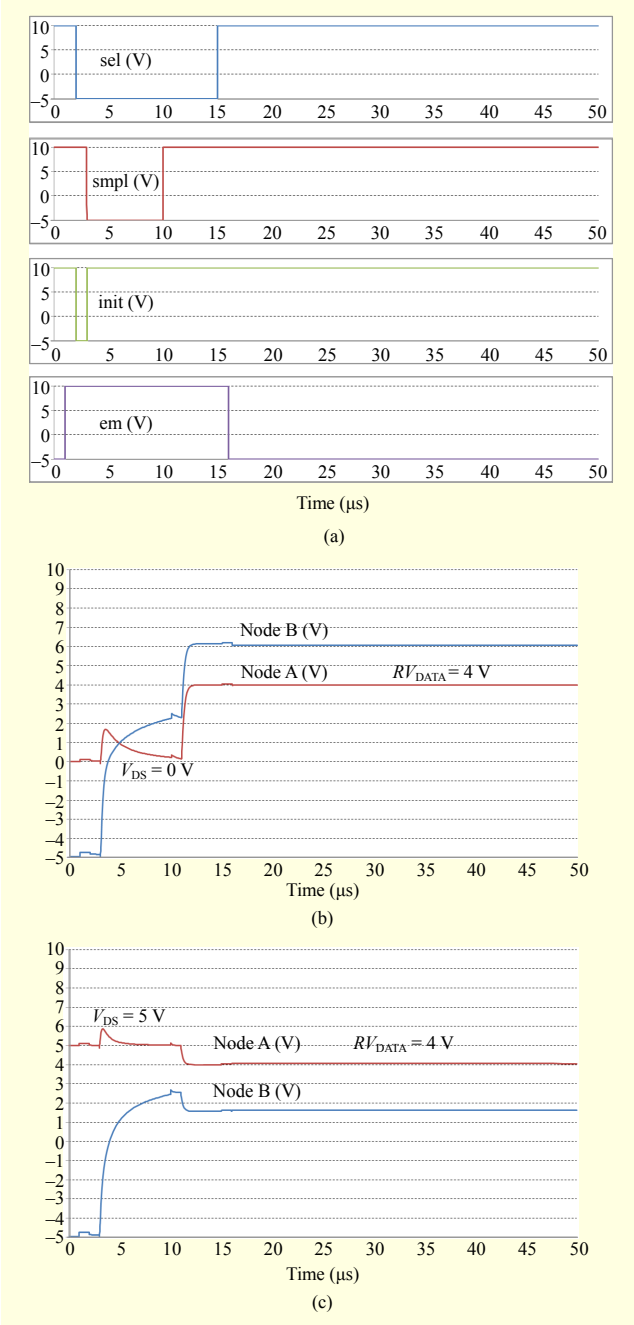

Fig. 4. Waveforms (a) for control signals, (b) for nodes A and B at V_{DS}=0 V, and (c) for nodes A and B at V_{DS}=5 V.

the data voltage swings as well. However, because the data voltage level of the sampling period is different according to the required V_B, the power estimation is accomplished by the more complicated method.

Since the output luminance is proportional to the current, the normalized luminance of an i-th column and j-th row subpixel ($L_{NO}(i,j)$) can be given as (6), where $g(i,j)$ is the gray level of an i-th column and j-th row subpixel in an 8-bit depth, γ is the gamma value of a display, and V_{MIN} is the minimum voltage

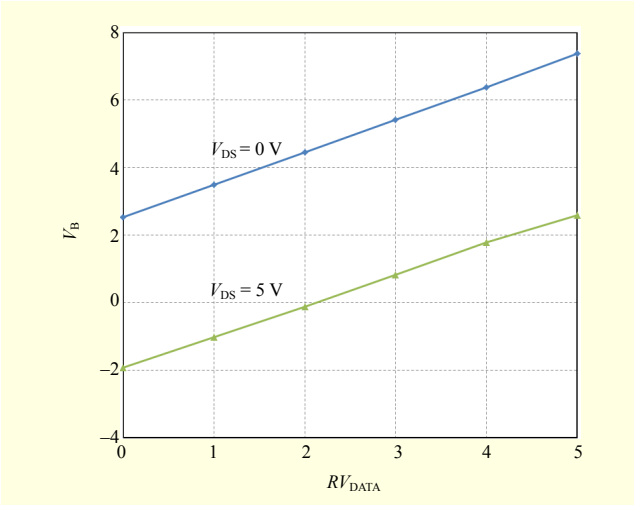

Fig. 5. Plot of V_B with respect to RV_{DATA} and V_{DS}.

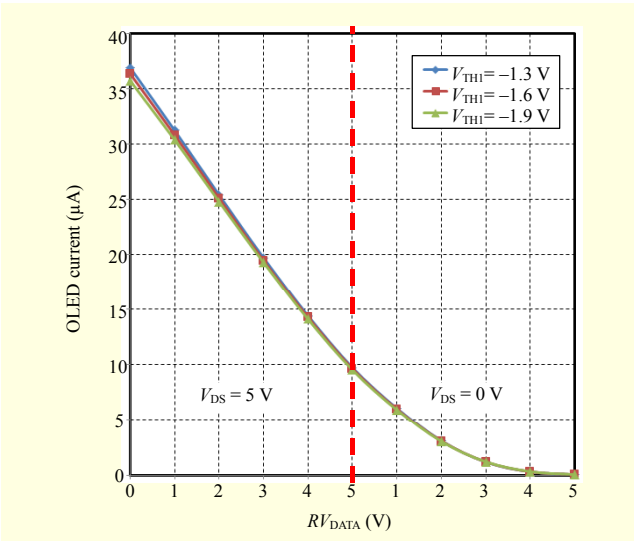

Fig. 6. Plot of OLED currents with respect to RV_{DATA} and V_{DS} at V_{TH1} variation of ±0.3 V.

level of V_B. Then, $V_B(i,j)$ and $RV_{DATA}(i,j)$ are calculated with the gray level by (7) and (8):

$$L_{NO}(i,j) = \frac{(EVDD - V_B(i,j))^2}{(EVDD - V_{MIN})^2} = \left(\frac{g(i,j)}{255}\right)^{\gamma}, \quad (6)$$

$$V_B(i,j) = EVDD - (EVDD - V_{MIN})\left(\frac{g(i,j)}{255}\right)^{\gamma/2}, \quad (7)$$

$$V_{DATA}(i,j) = \begin{cases} V_B(i,j), & V_B(i,j) < EVDD/2, \\ V_B(i,j) - EVDD/2, & V_B(i,j) \geq EVDD/2. \end{cases} \quad (8)$$

The resultant squares of the voltage swing ($DV_{PRO}(i,j)$) at a

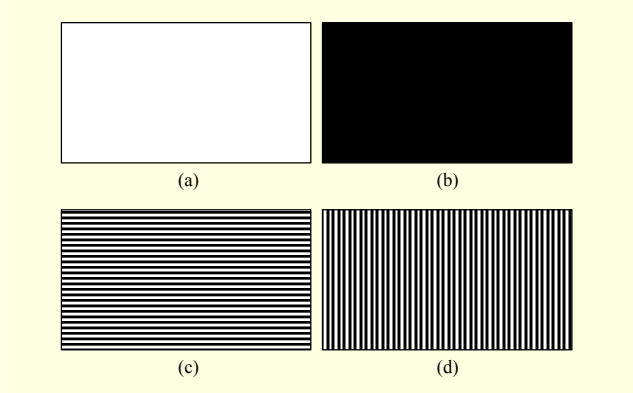

Fig. 7. Test patterns used to measure dynamic powers of data drivers: (a) white (b) black, (c) H-line, and (d) V-line.

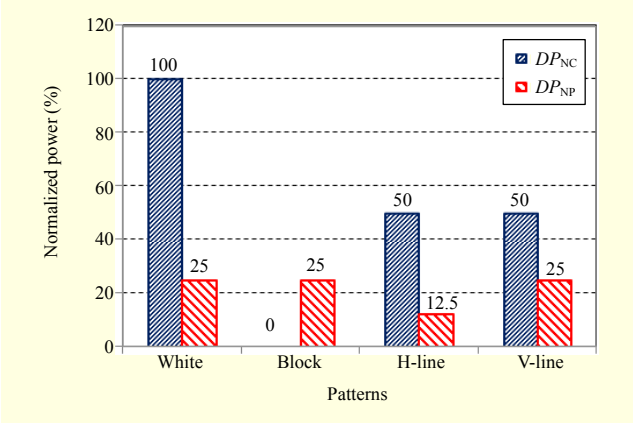

Fig. 8. Simulated power consumptions DP_{NC} and DP_{NP} depending on images displayed on conventional and proposed schemes.

given subpixel are estimated by considering the four cases as (9) to (12) and the dynamic power consumption of the proposed scheme (DP_{PRO}) is achieved as their sum, shown in (13):

$$\text{When } V_B(i,j) < EVDD/2 \quad \& \quad V_B(i,j+1) < EVDD/2,$$
$$DV_{PRO}(i,j) = 2 \cdot \left(\frac{EVDD}{2} - V_{DATA}(i,j) \right)^2; \tag{9}$$

$$\text{When } V_B(i,j) < EVDD/2 \quad \& \quad V_B(i,j+1) \geq EVDD/2,$$
$$DV_{PRO}(i,j) = \left(\frac{EVDD}{2} - V_{DATA}(i,j) \right)^2 + \left(V_{DATA}(i,j) \right)^2; \tag{10}$$

$$\text{When } V_B(i,j) \geq EVDD/2 \quad \& \quad V_B(i,j+1) < EVDD/2,$$
$$DV_{PRO}(i,j) = \left(V_{DATA}(i,j) \right)^2 + \left(\frac{EVDD}{2} - V_{DATA}(i,j) \right)^2; \tag{11}$$

$$\text{When } V_B(i,j) \geq EVDD/2 \quad \& \quad V_B(i,j+1) \geq EVDD/2,$$
$$DV_{PRO}(i,j) = 2 \cdot \left(V_{DATA}(i,j) \right)^2; \tag{12}$$

Fig. 9. 24 test images in use for evaluation.

$$DP_{PRO} = k \sum_{i=1}^{3N} \sum_{j=1}^{M} DV_{PRO}(i,j). \tag{13}$$

At the condition of V_{MIN}=0 V, the normalized dynamic power consumption of conventional and proposed schemes (DP_{NC}, DP_{NP}) is defined as (15) and (16) by means of the maximum dynamic power (DP_{MAX}) of (14):

$$DP_{MAX} = k \cdot 2 \sum_{i=1}^{3N} \sum_{j=1}^{M} (EVDD)^2 = 6kNM(EVDD)^2, \tag{14}$$

$$DP_{NC} = \frac{DP_{CON}}{DP_{MAX}} = \frac{\sum_{i=1}^{3N} \sum_{j=1}^{M} \left(EVDD - V_{DATA}(i,j) \right)^2}{3NM(EVDD)^2}, \tag{15}$$

$$DP_{NP} = \frac{DP_{PRO}}{DP_{MAX}} = \frac{\sum_{i=1}^{3N} \sum_{j=1}^{M} DV_{PRO}(i,j)}{6NM(EVDD)^2}. \tag{16}$$

First, we measure DP_{NC} and DP_{NP} according to the four test images shown in Fig. 7. In the conventional scheme, the voltage swings become the maximum and minimum values at the white and black patterns, respectively. Thus, we can expect the white and black patterns to show the largest and smallest amount of dynamic power consumption of DP_{MAX} and 0. Since the H-line and V-line patterns contain the same number of white and black pixels, the H-line and V-line patterns lead the medium power consumption of $DP_{MAX}/2$.

However, in the proposed system, the white and black patterns show the lower maximum power of $DP_{MAX}/4$, and the H-line and V-line patterns consume $DP_{MAX}/8$ and $DP_{MAX}/4$, respectively. The simulation results of the four test patterns are presented in Fig. 8. When the displayed images include more low gray pixels, DP_{NC} can be smaller than DP_{NP}. However, the proposed method guarantees that any image consumes less than $DP_{MAX}/4$.

Table 1. Measured power consumption.

Test image	APL	DP_{NC} (%)	DP_{NP} (%)	Power reduction $(DP_{NC} - DP_{NP})/DP_{NC}$
1	105	17.36	5.30	0.70
2	76	11.78	9.56	0.19
3	96	15.40	5.96	0.61
4	98	16.08	5.97	0.63
5	80	11.85	8.71	0.26
6	127	28.05	6.81	0.76
7	104	16.97	4.49	0.74
8	121	26.55	7.15	0.73
9	129	25.20	2.92	0.88
10	119	21.51	3.14	0.85
11	90	13.17	6.33	0.52
12	155	37.74	4.82	0.87
13	101	18.49	7.27	0.61
14	89	14.43	7.75	0.46
15	106	26.67	12.10	0.55
16	101	16.32	4.93	0.70
17	76	10.82	9.01	0.17
18	67	8.12	9.82	–0.21
19	112	20.50	4.92	0.76
20	170	55.76	15.53	0.72
21	114	20.72	4.40	0.79
22	107	18.68	4.90	0.74
23	102	19.11	7.02	0.63
24	105	19.61	6.57	0.67
Average	-	20.45	6.89	0.60

We evaluate the power consumption of the 24 real picture images, as shown in Fig. 9. Table 1 shows the average pixel levels (APLs), the normalized power consumption, and the power reduction ratios for test images. Particularly, in image 18, DP_{NP} is larger than DP_{NC} because most of its pixels are located in the low gray region. The proposed scheme establishes a substantial average power reduction of 60% for the 24 images.

IV. Conclusion

Our low data supply scheme was established by reducing the data voltage range by half. Even at the reduced data voltage range, the full dynamic range of an OLED current was achieved using level-shifting through a sampling capacitor according to the level of a data voltage in the sampling period. The feasibility of the proposed scheme was verified by SPICE. In addition, we showed that the power consumption is smaller than one-fourth of the maximum power in the conventional method over any displayed images.

References

[1] S.S. Kim, "The Next Big Thing in Displays," keynote presentation, *SID*, 2010.

[2] J. Souk and S. Whangbo, "Green Technology in LCDs," *Information Display*, vol. 26, no. 11&12, Nov./Dec. 2010, pp. 4-7.

[3] K. Teunissen and L.J. de OLDE, "EcoDesign for TV Displays' Information Display," *Inf. Display*, vol. 26, no. 11&12, Nov./Dec. 2010, pp. 10-14.

[4] J.Y. Lee, J.H. Kwon, and H.K. Chung, "High Efficiency and Low Power Consumption in Active Matrix Organic Light Emitting Diodes," *Organic Electron.*, vol. 4, no. 2-3, Sept. 2003, pp. 143-148.

[5] S.H. Jung et al., "A New Low-Power pMOS Poly-Si Inverter for AMDs," *IEEE Electron Device Lett.*, vol. 26, no. 1, Jan. 2005, pp. 23-25.

[6] H. Kanno et al., "Reduction in Power Consumption for Full-Color Active Matrix Organic Light-Emitting Devices," *Jpn. J. Appl. Phys.*, vol. 45, no. 35, Sept. 2006, pp. L947-L950.

[7] H. Nam and S.-W. Lee, "Low-Power Liquid Crystal Display Television Panel with Reduced Motion Blur," *IEEE Trans. Consum. Electron.*, vol. 56, no. 2, May 2010, pp. 307-311.

[8] N. Komiya et al., "Comparison of Vth Compensation Ability among Voltage Programming Circuits for AMOLED Panels," *Proc. 10th Int. Display Workshops*, 2003, pp. 275-278.

[9] T. Sasaoka et al., "A 13.0-inch AM-OLED Display with Top Emitting Structure and Adaptive Current Mode Programmed Pixel Circuit (TAC)," *Soc. Inf. Display (SID) Symp. Digest*, 2001, pp. 384-386.

[10] T. Inukai et al., "4.0-in. TFT-OLED Displays and a Novel Digital Driving Method," *Soc. Inf. Display (SID) Symp. Digest*, 2000, pp. 924-927.

[11] R.M.A. Dawson et al., "Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display," *Soc. Inf. Display (SID) Symp. Digest*, 1998, pp. 11-14.

Hyoungsik Nam received his BS, MS, and PhD in EECS from the Korea Advance Institute of Science and Technology (KAIST), Daejeon Rep. of Korea, in 1996, 1998, and 2004. He was involved in several projects of the VDSL transceiver, PLL/DLL, and LDIs for portable devices. He joined Samsung Electronics as a senior engineer in 2005, where he worked on Active-Matrix Liquid-Crystal Displays in the area of motion picture quality improvement, new image signal interfaces, the compression algorithm, low-power

technology, and low-cost display solutions for LCDs. He was in charge of the development of the world's first clock embedded intra panel interface, AiPi™. He is currently an assistant professor in the Department of Information Display at Kyung Hee University, Seoul, Rep. of Korea. His current research interests are low-power technologies, integrated circuits, and signal/user interfaces for flat panel displays. He has been active with SID and IMID as a member of the Program Committee.

Hoon Jeong received his MS in electronic engineering from Kyungpook National University, Daegu, Rep. of Korea, in 1999. Between 1999 and 2010, at LG Displays Co. Ltd, he was in charge of developing high-resolution mobile applications for low temperature polycrystalline silicon TFTs. Since 2010, he has been pursuing his PhD at Kyung Hee University, Seoul, Rep. of Korea. His current research is focused on oxide TFTs, LTPS, and AMOLED display.