Design of Dual-Mode Digital Down Converter for WCDMA and cdma2000

Miyeon Kim and Seungjun Lee

We propose an efficient digital IF down converter architecture for dual-mode WCDMA/cdma2000 based on the concept of software defined radio. Multi-rate digital filters and fractional frequency conversion techniques are adopted to implement the front end of a dual-mode receiver for WCDMA and cdma2000. A sub-sampled digital IF stage was proposed to support both WCDMA and cdma2000 while lowering the sampling frequency. Use of a CIC filter and ISOP filter combined with proper arrangement of multi-rate filters and common filter blocks resulted in optimized hardware implementation of the front end block in 292k logic gates.

Keywords: Software defined radio (SDR), digital down converter, dual-mode, WCDMA, cdma2000.

I. Introduction

Software defined radio (SDR) is a wireless interface technology where multiple wireless communication standards can be implemented into a single transceiver system [1]. In an SDR, most of the functional blocks including RF signal processing blocks are performed by a software module implemented with a high-speed processing unit. By doing this, a single hardware platform can support multiple wireless communication standards without replacing hardware components. Change of services according to user preferences and real-time acceptance of new services can be made on the fly by downloading new application software. Downloaded software reconfigures the internal hardware such that it can now process the new services. Manufacturers can provide updated wireless standards and protocol software later on through downloading once they sell SDR transceivers. In this way, they can rapidly adapt to the evolving communication market and maintain their competitiveness. Because SDR enables reconstructing previous systems into new systems by the direct processing of RF/IF signals with a high-speed digital signal processor and reconfigurable field-programmable gate array, it increases system interoperability and product life and minimizes developing time.

In accordance with various wireless specifications and systems, transceiver systems need an open-structure that supports the simplification and alteration of their functions with flexibility, considering the co-existence of two different standards for 3G mobile telecommunication, interoperability with 2G during the conversion period toward 3G, and mobile telecommunication after 3G. Therefore, SDR, which enables multimode, multiband, and multi-function through a software upgrade, is expected to be one of the most important mobile

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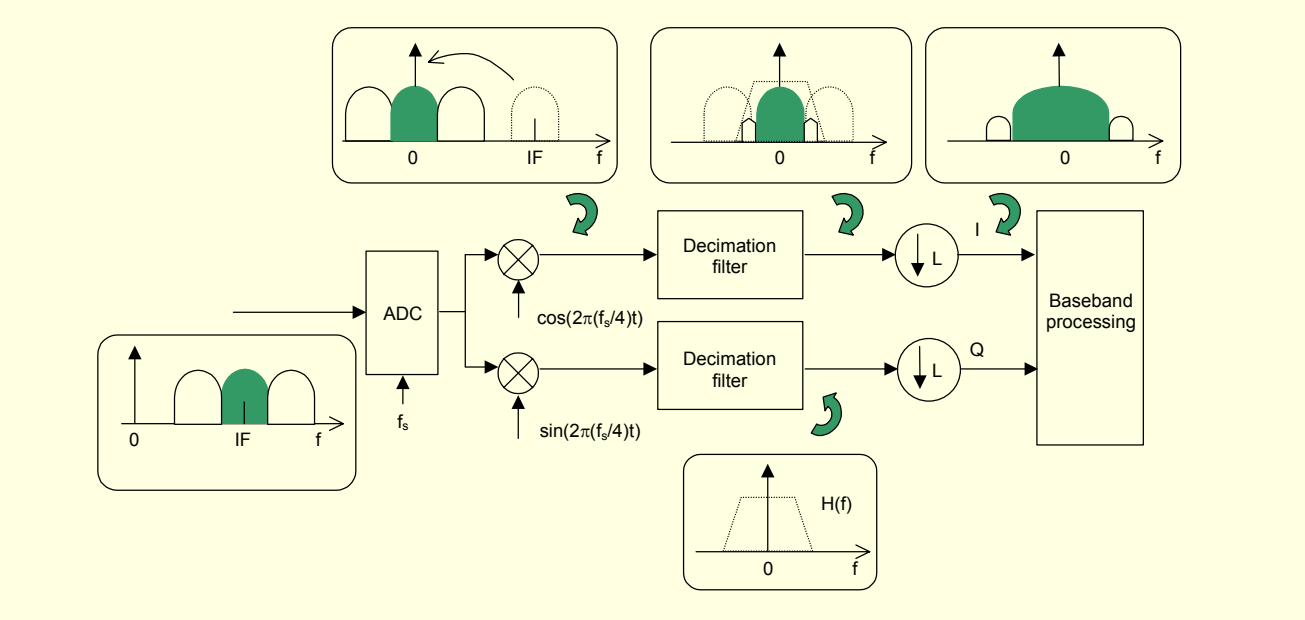

Fig. 1. Digital down converter architecture.

telecommunication technologies in the 21st century. In an SDR, digital intermediate frequency (IF) processing is required because it is difficult for analog circuits to process an IF which supports all standards for various mobile telecommunication terminals. In this paper, we propose a digital IF down converter architecture that can support multiple mobile telecommunication standards. An area-efficient digital down converter for both wideband code division multiple access (WCDMA) and cdma2000 has been implemented.

II. Digital IF System

Many communication devices and systems are gradually converted from analog to digital. The reason for this is that digital components are easier to produce, maintain, and repair than their analog counterparts.

They also show better performances than their analog counterparts in many cases. Digitally implemented modules often have the advantages of a smaller size, less power dissipation, and lower cost than analog modules. The digitally-implemented down conversion block in a receiver is called a digital down converter (DDC).

Figure 1 illustrates the general structure of a DDC. A DDC converts an intermediate frequency band signal into a baseband signal by using a mixer in the digital region and a low-pass filter after the analog-to-digital conversion.

III. Digital Down Converter Algorithm

A DDC is a basic building block used in many communication systems, as depicted in Fig 1. The input IF signal, s(t), is first converted into a digital signal with an analog-to-digital converter. A digitized IF signal is separated into I and Q signals through a digital mixer and inputted to low-pass filters [2].

It is important to select the IF and sampling frequencies carefully for an efficient DDC block architecture. In this paper, we opted for an IF frequency that is a quarter of the analog-to-digital sampling frequency, such that the output from the local oscillator becomes either 0, 1, or −1, as shown in Fig. 2. With this, a mixer doesn't require a local oscillator or multipliers, and it can be implemented as a simple multiplexer.

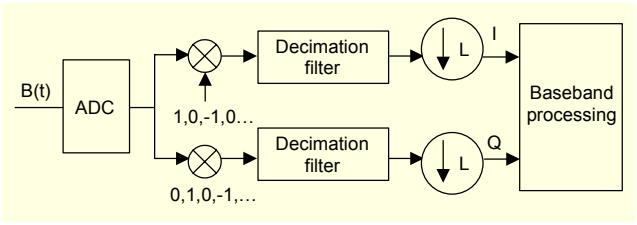

Fig. 2. Simplified DDC architecture.

Selecting a suitable sampling frequency is another important issue in the design of an SDR. For feasible digital IF processing, a low IF receiver architecture with sub-sampling is mainly preferred. 'Sub-sampling' is a process to sample a band-pass signal at a frequency several times higher than the signal bandwidth instead of at the Nyquist frequency. In a sub-sampled system, the sampling frequency can be much lower than the Nyquist frequency, which should be at least twice the carrier frequency; therefore, the computation overhead at the

digital IF block becomes greatly reduced [3].

The sub-sampling frequency can be decided from the minimum and maximum frequencies of the band-pass signal, f_L and f_H, respectively. It should meet the following constraints to avoid aliasing after the sampling:

$$f_H \le n\frac{f_S}{2}(\text{Hz}) \quad \text{and} \tag{1}$$

$$f_L \ge (n-1)\frac{f_S}{2}(\text{Hz}) . \tag{2}$$

In these equations, n is an arbitrary integer satisfying $n \le (f_H / B)$, where B denotes the bandwidth of the signal defined as $B = f_H - f_L$. Using (1) and (2), sampling frequency f_S, which is free from aliasing, can be defined as in (3). Figure 3 shows the signal spectrum of the sub-sampled signal.

$$\frac{2}{n} f_H \le f_S \le \frac{2}{n-1}(f_H - B) . \tag{3}$$

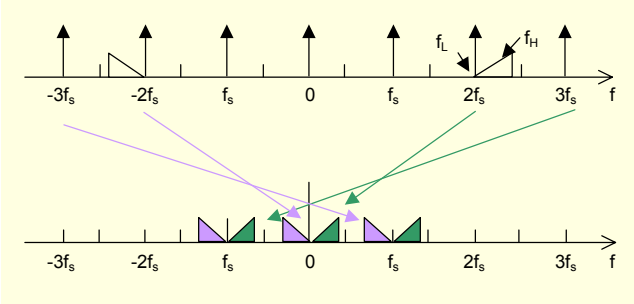

Fig. 3. Sub-sampling spectrum.

IV. Digital Down Converter Architecture

In this paper, we applied the following schemes to design an efficient DDC architecture for a dual-mode WCDMA/cdma2000. First, digital IF sub-sampling is used to reduce power dissipation with a lower sampling frequency than the Nyquist rate. We also used a cascaded-integrator-comb (CIC) filter and an interpolated finite impulse response (IFIR) filter to reduce hardware complexity. The sizes of the down sampler and filter orders have been optimized through an extensive simulation process. Finally, we reduce the complexity of the serially-connected multiple stage filter blocks by extracting the common filter blocks.

Figure 4 shows the overall architecture of the designed DDC. The input sampling rate is 15.36 MHz for WCDMA and 4.9152 MHz for cdma2000, which is four times the over-sampled rate of the baseband chip rates of 3.84 MHz for WCDMA and 1.2288 MHz for cdma2000. Hence, the actual sampling rate is decided as 61.44 MHz, which is an integer multiple of 15.36 MHz and 4.9152 MHz, and the IF frequency is decided to be 138.24 MHz, which satisfies the sub-sampling constraints previously stated in (1) through (3).

The over-sampled data are first down-sampled by 4 to make 15.36 MHz WCDMA samples. They are either filtered to meet the WCDMA filter mask specification, or up-sampled by 8 and down-sampled by 25 to make 4.9152 MHz cdma2000 samples. As the over-sampled data passes through a mixer and DDC, undesired channel data gets attenuated with multiple-stage filtering to meet the filter mask specification. Figures 5 and 6 show the frequency responses of the designed filters, WCDMA and cdma2000, respectively.

To reduce the complexity of the hardware, we extensively used CIC filters. CIC filters have the advantage of not requiring multipliers. However, they do have unwanted drooping in the passband, and stopband attenuation is less than that of an FIR filter. More stop band attenuation causes passband signal loss due to the drooping. Interpolated second-order polynomial (ISOP) filters were added after the CIC filters to solve the problem [4]-[6]. Figure 7 shows the effect of adding ISOP

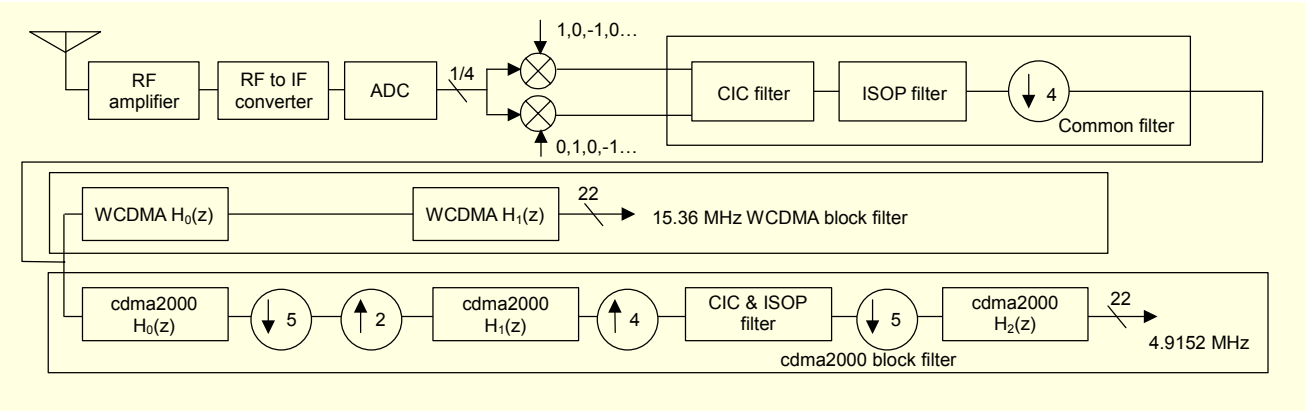

Fig. 4. Dual-mode DDC for WCDMA/cdma2000.

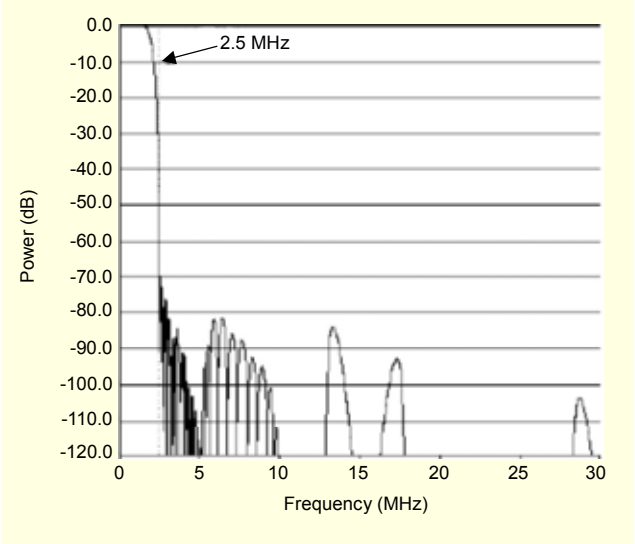

Fig. 5. Overall frequency response for WCDMA application.

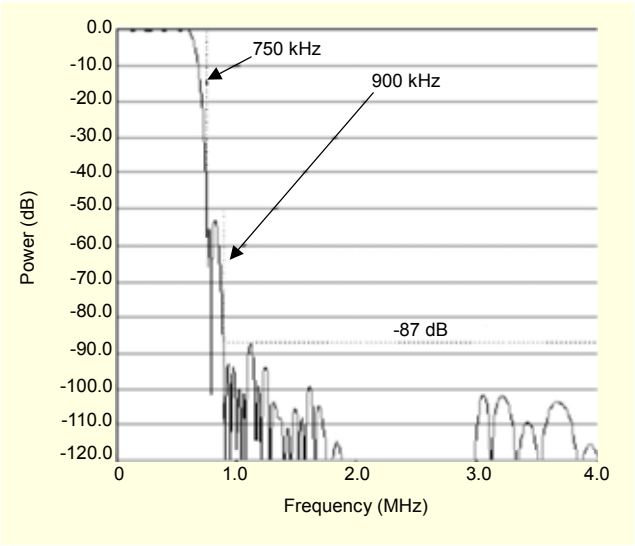

Fig. 6. Overall frequency response for cdma2000 application.

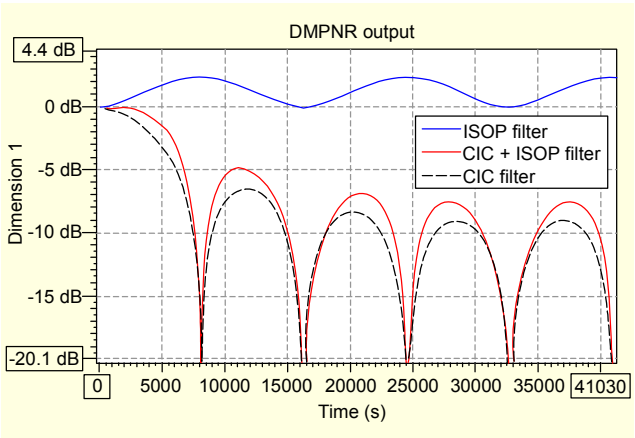

Fig. 7. Droop improvement with an ISOP filter.

filters to improve the filter performance.

To reduce the number of multiplications in the filter design, all the filter coefficients were made to be symmetric. IFIR filters were used to realize narrow band filters, which gives a reasonable performance with a reduced number of taps, compared with conventional FIR filters. The order of filters, in/out bit width of each filter, and bit width of the filter coefficients were optimized through an extensive simulation to minimize the hardware requirement while satisfying the desired filter masks.

V. DDC Hardware Implementation and Optimization

C and matlab programming are used to verify the DDC algorithm. Filter coefficients were automatically synthesized in a fixed-point format from a filter synthesis tool, and verified to meet the stopband, passband attenuation, and passband ripple of WCDMA and cdma2000 filter masks. Logic synthesis using a 0.35 micron standard cell library produced a 466,878 gate count. Figure 8 shows an improved architecture of DDC for hardware area reduction. More common blocks were extracted to minimize the hardware requirement. Cdma2000 requires a narrower passband, so it has to go through additional filtering stages, which are depicted as "$H_0(z)$" and "CIC & ISOP filter" in the figure. The new architecture was synthesized using 292,391 logic gates so that a 37% area reduction was achieved. These results are summarized in Table 1.

Table 1. Logic synthesis results.

Using 0.35 micron standard cell library		
proposed design	Figure 4	Figure 8
in/out length	14/22	14/22
system clock	61.44 MHz	61.44 MHz
total area	466,877	292,390

VI. Conclusion

In this paper, the design of a dual-mode DDC supporting mobile telecommunication standards for WCDMA and cdma2000 were presented. A sub-sampled digital IF stage was proposed to support both WCDMA and cdma2000 while lowering the sampling frequency. Use of a CIC filter and ISOP filter, proper arrangement of multi-rate filters, and common filter blocks resulted in optimized hardware implementation in 292k logic gates.

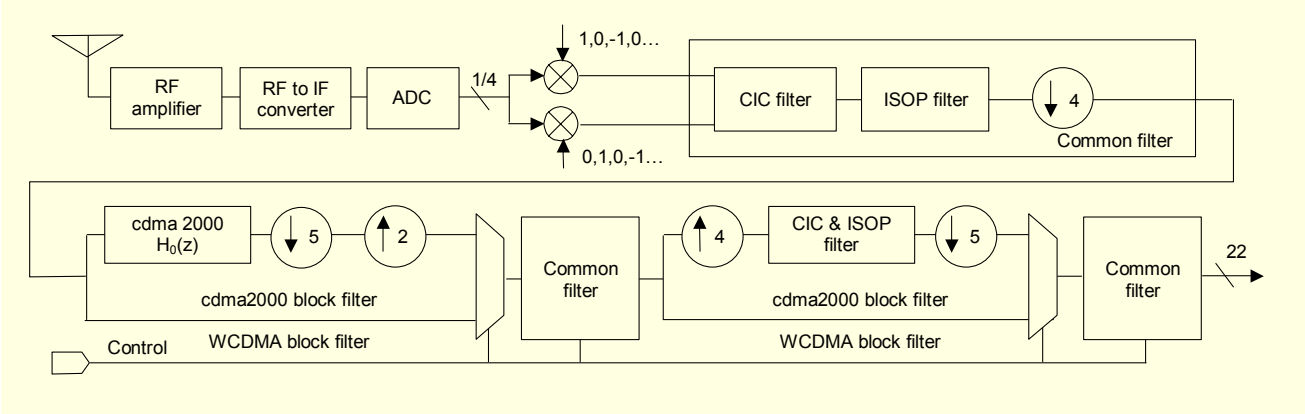

Fig. 8. Improved architecture of a dual-mode DDC.

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