Design of Gate-Ground-NMOS-Based ESD Protection Circuits with Low Trigger Voltage, Low Leakage Current, and Fast Turn-On

Yong-Seo Koo, Kwangsoo Kim, Shihong Park, Kwidong Kim, and Jong-Kee Kwon

In this paper, electrostatic discharge (ESD) protection circuits with an advanced substrate-triggered NMOS and a gate-substrate-triggered NMOS are proposed to provide low trigger voltage, low leakage current, and fast turn-on speed. The proposed ESD protection devices are designed using 0.13 μm CMOS technology. The experimental results show that the proposed substrate-triggered NMOS using a bipolar transistor has a low trigger voltage of 5.98 V and a fast turn-on time of 37 ns. The proposed gate-substrate-triggered NMOS has a lower trigger voltage of 5.35 V and low leakage current of 80 pA.

Keywords: ESD protection circuit, GGNMOS, leakage current, turn on.

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I. Introduction

Electrostatic discharge (ESD) damage has become the main reliability issue for deep-submicron CMOS integrated circuit products. To overcome this ESD problem, on-chip ESD protection circuits have been added around the input and output pads of CMOS ICs as shown in Fig. 1. The effectiveness of ESD protection circuits is also seriously degraded by advanced CMOS fabrication technologies, especially when a lightly doped drain structure and salicide diffusion are used. Therefore, salicide blocking, and ESD implantation [1], [2] process modifications have been added to the CMOS processes to improve the ESD robustness of MOSFETs. These additional process modifications in CMOS technology require extra process steps and mask layers, which increase the fabrication cost and slow down the throughput of production. Moreover, with aggressive device scaling, the circuit operating voltage has been decreased correspondingly. Some early 5 V systems have changed from 5 V to 3.3 V, or even 1.8 V. Thus, system voltages have not been kept at 5 V but are a mixture of 5 V and 3.3 V. For mixed-voltage I/O design, an IC with a 3.3 V power supply needs to accept 5 V input signals. In the traditional ESD protection design, the normal input signal with high voltage may turn on the ESD protection device, which is connected between the input pad and the power line. Therefore, the traditional input ESD protection circuit must be modified for application in this mixed-voltage interface.

To sustain the required ESD levels, ESD protection devices are often designed with large device dimensions with a multi-finger layout style to reduce the total occupied silicon area. Typically,

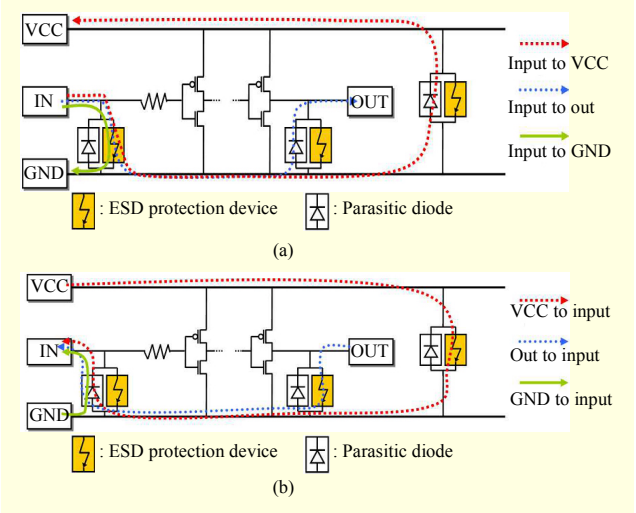

Fig. 1. On-chip ESD protection strategy for (a) positive ESD surge and (b) negative ESD surge.

multi-finger gate-grounded NMOS (GGNMOS) devices are widely used as ESD protection structures due to the effectiveness of the parasitic lateral NPN bipolar junction transistor in handling high ESD current. However, it has been reported that, sometimes, a multi-finger GGNMOS is not uniformly turned on under ESD stress [3]-[6]. Only some fingers of the GGNMOS are turned on and this often causes a low ESD level. The substrate-triggered technique and gate-substrate-triggered technique are useful methods to reduce the trigger voltage and enable the GGNMOS to turn on uniformly. However, ESD protection circuits using these methods are not effective for low leakage current and fast turn-on [7]. In this paper, ESD protection circuits with advanced substrate-triggered NMOS (STNMOS) and gate-substrate-triggered NMOS (GSTNMOS) are proposed for low trigger voltage, fast turn-on, and low leakage current. This work has been successfully verified using the 0.13 μm CMOS process.

II. Proposed ESD Protection Circuit

1. STNMOS

The substrate-triggered technique is widely used to reduce the trigger voltage and to enhance the turn-on uniformity of GGNMOSs. Figure 2(a) shows a conventional substrate-triggered NMOS [7] using PMOS (GGNMOS PMOS). However, the conventional method has two problems due to the use of PMOS. The first problem is that the trigger PMOS (MP1) with a long channel length which reduces gate leakage slows the turn-on time. The second is that the gate oxide of the trigger PMOS can be easily broken down by an ESD surge. These problems are solved by using PNP bipolar transistors

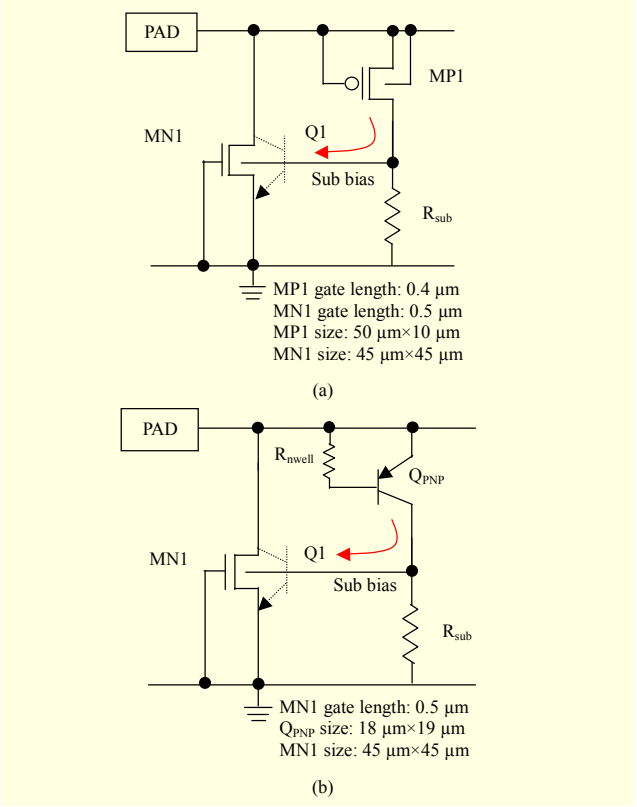

Fig. 2. (a) Conventional substrate-triggered NMOS using PMOS (GGNMOS PMOS) and (b) proposed substrate-triggered NMOS using PNP bipolar transistor (STNMOS).

instead of a trigger PMOS as shown in Fig. 2(b). Under normal operating conditions, the gate and substrate voltages of the NMOS (MN1) are zero, and the NMOS is turned off. Therefore, the protection circuit does not interfere with the normal functions of the input circuits. When a positive ESD voltage is zapping on the grounded pad, the ESD voltage can trigger the PNP (QPNP) bipolar transistor into avalanche breakdown. Therefore, a substrate current generated by the PNP bipolar transistor flows into the base of the parasitic bipolar transistor (Q1) in the GGNMOS. This helps the forward bias base-emitter junction of the parasitic bipolar transistor. As a result, the trigger voltage is reduced, and the turn-on uniformity of the multi-finger GGNMOS is enhanced. Also, the use of a PNP bipolar transistor with a narrow base width can speed up the turn-on time, which is the disadvantage of a trigger PMOS with a long channel.

2. GSTNMOS

Figure 3(a) shows a conventional GSTNMOS [8]. However, these conventional methods have some problems. In the case of the STNMOS, its trigger voltage is not higher than that of the GSTNMOS. In the case of the GSTNMOS, the main

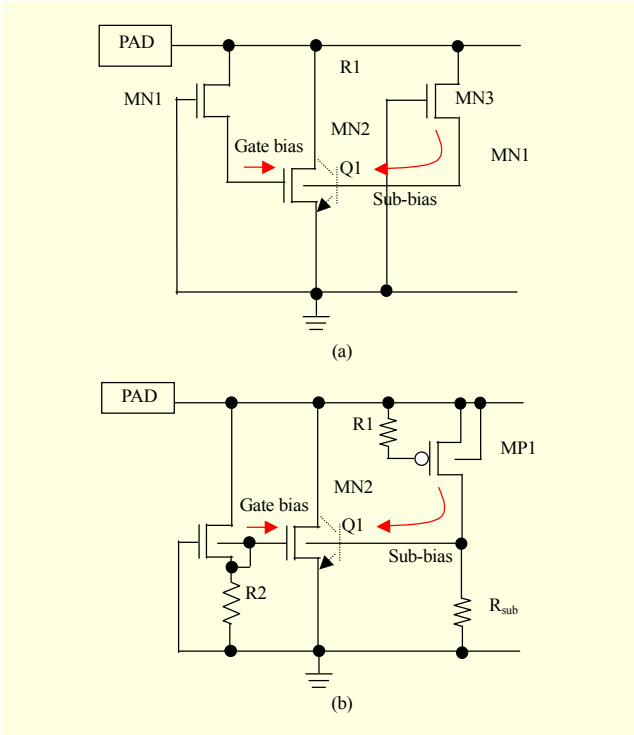

Fig. 3. (a) Conventional GSTNMOS and (b) proposed GSTNMOS.

disadvantage of this technique is its high leakage current under normal operating conditions. This is due to biasing of both the gate and substrate of the main transistor. Biasing the gate moves the protection NMOS transistor (MN2) towards moderate and strong inversion, while biasing the substrate reduces the threshold voltage of the transistor. This leakage for a 0.18 μm CMOS technology is in the milliampere range [8]. These problems are solved by using the proposed GSTNMOS as shown in Fig. 3(b).

Under normal operating conditions, as in the STNMOS, the gate and substrate voltage of the NMOS (MN2) are zero and the NMOS (MN2) is turned off. Therefore, the protection circuit does not interfere with the normal functions of the input circuits. When a positive ESD voltage is zapping on the grounded pad, ESD voltage can trigger the NMOS (MN1) and PMOS (MP1) into avalanche breakdown. Therefore, a substrate current generated by trigger devices (MN1, MP1) flows into the base of the parasitic bipolar transistor (Q1) in the GGNMOS. As in the STNMOS, this helps the forward bias base-emitter junction of the parasitic bipolar transistor. As a result, the trigger voltage is reduced and the turn-on uniformity of the multifinger GGNMOS is enhanced. Also, in order to reduce the leakage, another resistor (R2) can be used to tie the gate of the protection NMOS (MN2) to the ground under operating conditions.

III. Experimental Results

1. Transmission Line Pulse Measurement

A rectangular pulse can be obtained when discharging an open-ended transmission line with 50 ohm impedance over an attenuator as shown in Fig. 4. The transmission line is charged via a high voltage power supply (HV) and discharged via a switch. The current and voltage values are captured after the attenuator. A short coaxial cable connects the attenuator with the device under test (DUT).

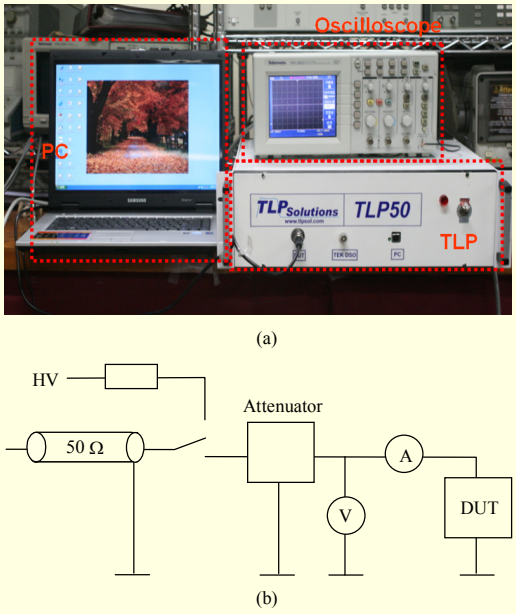

Fig. 4. Transmission line pulse test system.

A. STNMOS

The I-V characteristic and DC-leakage current was measured with a transmission line pulse (TLP) tester with the pulse duration of 100 ns and a rising time of 10 ns. Figure 5 shows the TLP I-V curves of the conventional GGNMOS, GGNMOS PMOS, and STNMOS circuits having the same areas (a width of 400 μm). While the GGNMOS has a high trigger voltage of 9.92 V, each circuit with the substrate-triggered technique has a low trigger voltage of about 6 V. This result is very important for effective ESD protection circuit design. For the CMOS 0.13 μm process, the target design window can be determined between the operating voltage of 3.3 V and the oxide breakdown voltage of 10 V. Although ESD protection circuits have high robustness, the effective robustness is limited by the design window. As the results demonstrate, the robustness of the STNMOS (1.71 A) is higher than that of the conventional GGNMOS (1.4 A).

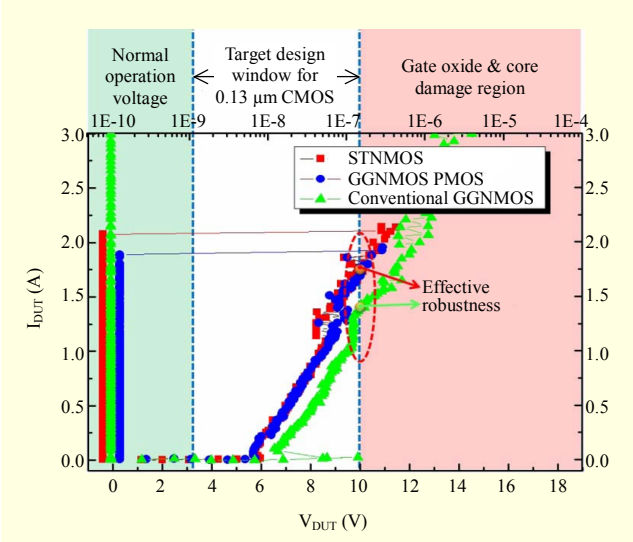

Fig. 5. Measured TLP I-V characteristics of the conventional GGNMOS, GGNMOS PMOS, and STNMOS.

B. GSTNMOS

Figure 6(a) shows the TLP I-V curves of the conventional GGNMOS, GGNMOS PMOS, and GSTNMOS circuits. While the GGNMOS has a high trigger voltage of 9.92 V, the circuit with GGNMOS PMOS has a low trigger voltage of about 6 V. Also, the proposed GSTNMOS has a trigger voltage of 5.3 V, which is lower than that of the GGNMOS PMOS. Figure 6(b) shows the trigger voltage of the conventional GGNMOS, GGNMOS PMOS, and the proposed GSTNMOS.

As the results demonstrate, the robustness of GSTNMOS (2.23 A) is higher than that of conventional GGNMOS (1.4 A) and STNMOS (1.68 A). However, the ESD protection circuits using the conventional gate-substrate triggered technique are not effective for low leakage current [7]. Therefore, the proposed GSTNMOS reduced the leakage current. Figure 7 shows the leakage current at 3.6 V (normal operating condition) as obtained by a semiconductor parameter analyzer. The experimental result is 80 pA at 3.6 V (normal operating condition).

2. HBM/MM Test

The result from the TLP test with a 100 ns pulse width can be well correlated to the human body model (HBM) [8], [9]. However, a miscorrelation between TLP and HBM still exists because of the system's limitations and its testing environments [10], [11].

The HBM and MM ESD robustness of the proposed devices are measured by the ESS-6008 ESD simulator. The failure criterion is defined as 20% current shifting from the original I-V

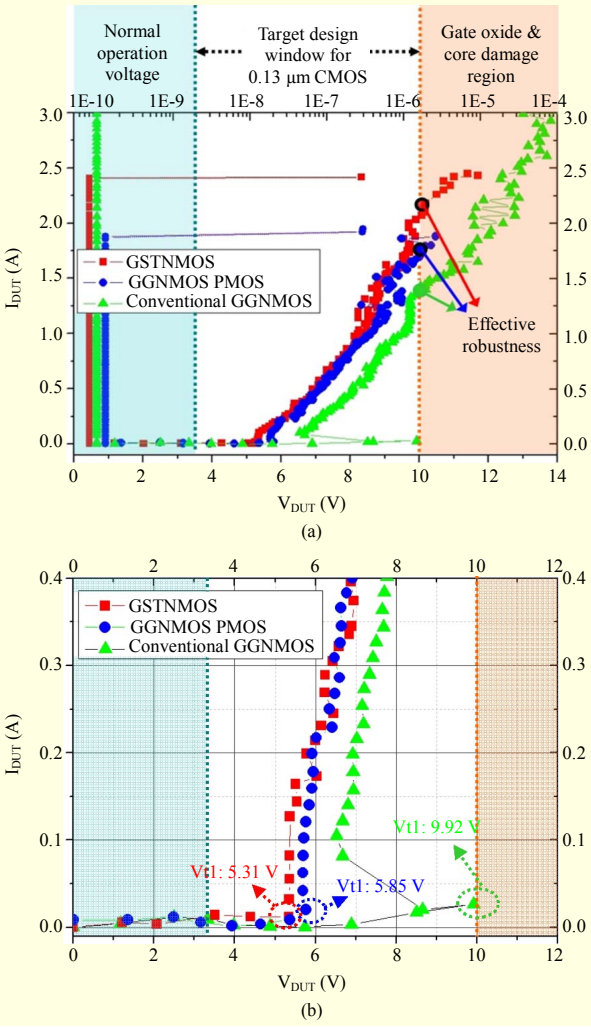

Fig. 6. (a) Measured TLP I-V characteristics and (b) trigger voltage of the proposed GSTNMOS.

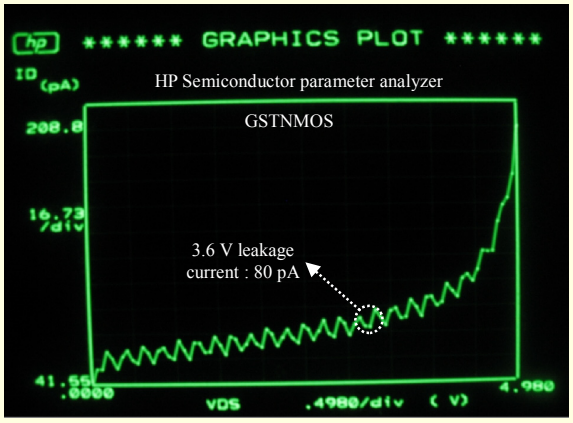

Fig. 7. Leakage current of the proposed GSTNMOS.

curve at 3.6 V (operating voltage+10%). The proposed STNMOS and GSTNMOS can pass the ESD of HBM 3.2 kV

and 3.7 kV and MM 210 V and 230 V. All the proposed devices meet commercial standards (HBM 2 kV, MM 200 V).

3. Turn-On Speed

The measured voltage waveform of the input signal on the pad with the proposed STNMOS using a PNP bipolar transistor under normal operating condition is shown in Fig. 8(a). The voltage waveform with no operating condition is shown in Fig. 8(a). The voltage waveform shows no degradation when a 3.3 V voltage signal is applied to the pad. The experimental setup to measure the turn-on speed of the ESD protection circuit under transient conditions is shown in Fig. 8(b). Figure 9 shows a comparison of turn-on speeds of the GGNMOS PMOS and the STNMOS under a 0 V to 10 V voltage pulse with the pulse rising time of 25 ns. The turn-on time of the STNMOS (about 37 ns) is faster than that of the GGNMOS PMOS (about 80 ns) under a 0 V to 10 V voltage pulse. From the experimental results, the STNMOS is more suitable than the GGNMOS PMOS for quick discharge of the electrostatic energy.

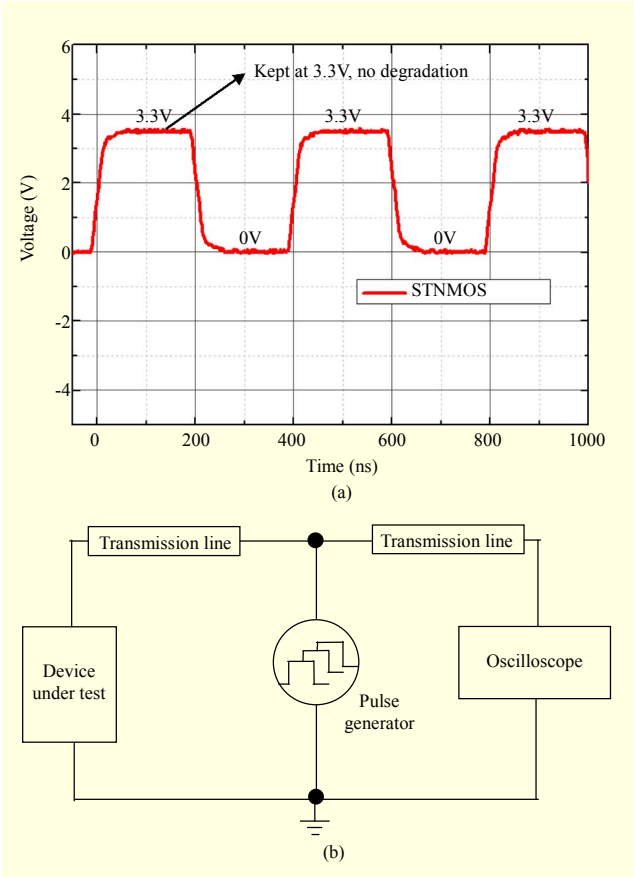

Fig. 8. (a) Measured voltage waveform of input signals on the pad with the STNMOS under normal circuit operating conditions and (b) experimental setup to measure the turn-on speed.

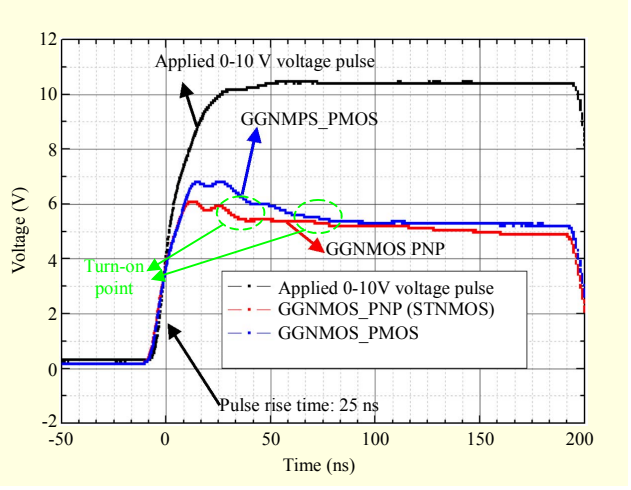

Fig. 9. Turn-on waveform of GGNMOS PMOS and GSTNMOS.

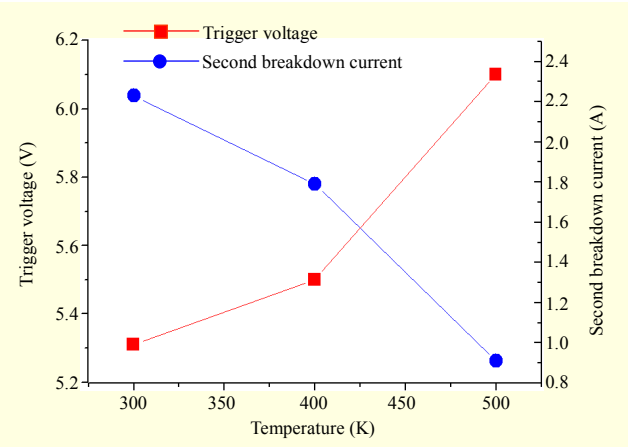

Fig. 10. Thermal characteristics of the I-V curve.

4. Thermal Characteristics

To investigate the temperature dependency of the proposed ESD protection circuits, we repeated TLP characteristics at various temperatures from 300 K to 500 K using a hot-chuck temperature controller. As shown in Fig. 10, as the temperature increases, the trigger voltage increases, and the second breakdown current decreases. A summary of the comparison of the ESD characteristics is presented in Table 1.

IV. Conclusion

In this paper, ESD protection circuits with a substrate-triggered technique and a gate-substrate-triggered technique were proposed. The proposed ESD protection circuits have been verified using the 0.13 μm CMOS process. Compared to the conventional GGNMOS, the proposed STNMOS using a bipolar transistor can provide a much lower trigger voltage of 5.98 V. It shows a turn-on time of 37 ns, which is faster than

Table 1. Comparison of the ESD characteristics of GGNMOS, GGNMOS PMOS, STNMOS, and GSTNMOS.

	GGNMOS	GGNMOS PMOS	STNMOS	GSTNMOS
V_{t1} (V)	9.92	5.95	5.98	5.31
V_h (V)	6.58	5.91	5.71	5.30
V_{t2} (V)	14.52	10.58	10.54	11.71
Effective robustness @ 10 V (A)	1.4	1.68	1.71	2.23
I_{leak} @ 3.6 V (pA)	100	130	85	80
Turn-on time (ns)	~120	~80	~37	~71

that of the conventional substrate-triggered ESD protection circuit of about 80 ns. Also, compared to the conventional GGNMOS, the proposed GSTNMOS can provide a much lower trigger voltage of 5.35 V. It also showed a leakage current of 80 pA at 3.6 V normal operation, which is lower than that of the conventional gate-substrate-triggered ESD protection circuit of about 10 to 100 mA. The trigger voltage of the proposed ESD protection circuits decreases, and the second breakdown current decreases as the temperature increases. The proposed ESD protection design is still suitable for use in protecting the input and output stages of ICs in future nanoscale CMOS technology.

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