# Effect of Shield Line on Noise Margin and Refresh Time of Planar DRAM Cell for Embedded Application

Junghwan Lee, Seongdo Jeon, and Sung-Keun Chang

**In this paper we investigate the effect of a shield metal line inserted between adjacent bit lines on the refresh time and noise margin in a planar DRAM cell. The DRAM cell consists of an access transistor, which is biased to 2.5V during operation, and an NMOS capacitor having the capacitance of 10fF per unit cell and a cell size of 3.63 $\mu m^2$. We designed a 1Mb DRAM with an open bit-line structure. It appears that the refresh time is increased from 4.5 ms to 12 ms when the shield metal line is inserted. Also, it appears that no failure occurs when $V_{cc}$ is increased from 2.2 V to 3 V during a bump up test, while it fails at 2.8 V without a shield metal line. Raphael simulation reveals that the coupling noise between adjacent bit lines is reduced to 1/24 when a shield metal line is inserted, while total capacitance per bit line is increased only by 10%.**

**Keywords: DRAM, noise margin, planar cell, refresh time, shielded metal line.**

Manuscript received Nov. 25, 2003; revised June 23, 2004.

Junghwan Lee (phone: +82 43 270 3930, email: junghwan.lee@magnachip.com) and Seongdo Jeon (email: seongdo.jeon@magnachip.com) are with the SoC Device Team, MagnaChip Semiconductor Inc., Cheongju, Korea.

Sung-Keun Chang (email: skchang@chungwoon.ac.kr) is with the Department of Electronics Engineering, Chungwoon University, Hongseong, Korea.

## I. Introduction

There has been increasing interest in embedded DRAM for system-on-chip application [1]. The advantages of embedding DRAM to logic circuits are an increased bandwidth [2], [3], reduced power consumption, and small die size. However, there are critical problems such as a degraded refresh time in the DRAM cell and a low yield caused by the increase in processing steps when one embeds a conventional DRAM cell to the logic process [4]. This is caused by incompatibility between DRAM and the logic process. While the DRAM process focuses on the reduction of cell size with a sacrifice in device performance, the logic process mainly focuses on increasing device performance by using a dual gate transistor, salicide, and multi-level metals. Unfortunately, those steps in the logic process degrade the refresh time of the DRAM cell and also reduce the total yield due to the increase in process steps. Therefore, one should modify the conventional logic process when a conventional DRAM cell is embedded. This results in a modification of the logic library and intellectual properties (IPs) since they were proved using the conventional logic process.

Recently, a planar DRAM cell has been investigated to solve these problems [5], [6]. A planar DRAM cell consists of one access transistor and MOS capacitor with a metal bit line. Although its cell size is normally four to seven times larger than a stack or trench type DRAM cell, it uses a conventional logic process and thus enables the use of the conventional logic library and IPs. When a new DRAM cell is developed, two major parameters should be optimized. The first is the refresh

time of the memory cell, which depends on the total leakage currents of the cell region. The total leakage current mostly consists of leakage currents in the access transistor, a bit line junction, and isolation between the cells. The second parameter to be optimized is the sensitivity of signals in the bit line, which is mainly affected by noise on adjacent bit lines. This is caused by the electrically-floating state of bit lines during the sensing operation. There are several methods to reduce bit line coupling noise such as widening the space between bit lines, canceling the noise by twisting the bit lines, or inserting a shield line between bit lines [7]-[9]. In terms of design architecture, optimization of the sense amplifier can also enhance refresh time [10], [11].

In this paper, we report on the influence of a shield bit line with a ground voltage inserted between adjacent bit lines on the refresh time and sensing margin of a planar DRAM cell. It appears that the addition of the shield line enhances both refresh time and the sensing margin, although the total bit line capacitance is increased by only 10%. It has been revealed that both the coupling noise and $C_b/C_s$ ration are also important factors in a sensing operation.

## II. Cell Design and Integration

Figure 1 shows the layout and vertical structure of a memory cell. As shown, NMOS is used as the access transistor and capacitor in the memory cell. Capacitance per cell is about 10fF at 2.5 V inversion mode operation. The total memory density is 1 Mb. An open bit line structure is used to reduce the block size. The areas of the unit cell and capacitor are 3.63 and 1.59 $\mu m^2$, respectively. To obtain maximum cell capacitance, spacing in adjacent active regions of the memory cell has a shorter distance than in the normal logic rule. Since the active region under the capacitor plate is not exposed to a high-dose source/drain implantation, the electrical space margin between adjacent actives in the capacitor region is sufficient to shrink the spacing design rule as long as the lithography margin permits it. After checking the electrical parameters with several different active spacings, the design rule is reduced from 0.36 to 0.32 μm.

A conventional 0.25 μm logic process is used to integrate the DRAM block. A triple well is used to prevent a noise current from the DRAM peripheral and logic regions. In a conventional DRAM, the P-well in the cell array has a negative well bias to decrease the bit line capacitance and leakage current. However, to reduce the lithography step and block size, the P-well is tied to the ground. It appears that the behavior of both NMOS and PMOS is little affected when a deep N-well is added. Their variation in threshold voltage is ±0.02 V, which can be regarded as a process variation. Another notable change

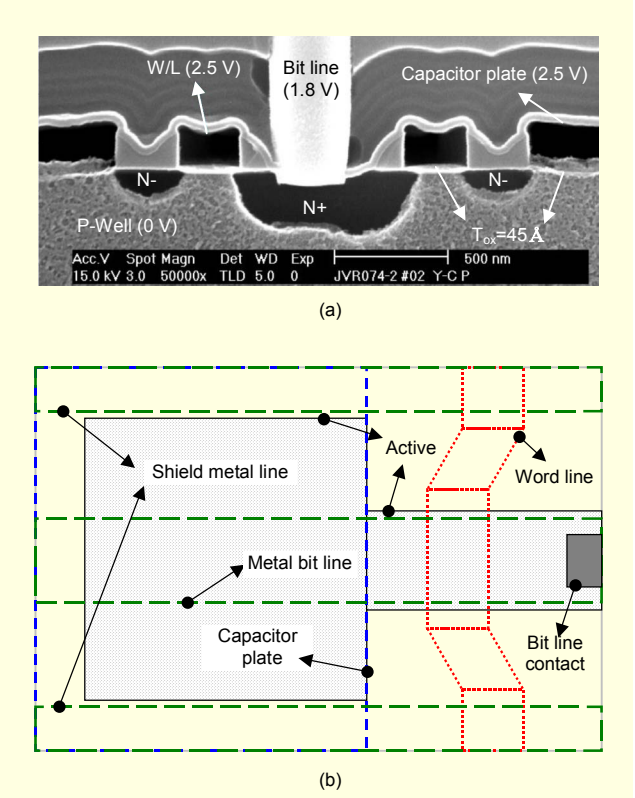



Fig. 1. (a) Cross-sectional SEM view of the vertical structure of a planar DRAM cell. (b) Cell layout.

in this technology compared with normal DRAM is that the word line is biased to the supply voltage (2.5 V) rather than to a higher voltage. To minimize the leakage current of the cell transistor, several methods are used. First, the channel length of the cell transistor is optimized to 0.31 μm at which the reverse short channel effect is maximized. In this condition, channel mobility degradation can be minimized since a small implantation dose is needed to increase the threshold voltage of the cell transistor. Note that the threshold voltage is adjusted to 1.1 V. Second, a lightly doped junction is used in the storage node to reduce the junction leakage current. While the junction in the bit line contact region is exposed to a high-dose implantation, the junction of the storage node is blocked from it by the remaining thick oxide. Figure 2 shows the process flow. As shown, the spacing between the word line and capacitor plate is less than double the thickness of the spacer oxide. After the lightly-doped drain (LDD) implantation in the junction of the bit line contact and storage node region, an LDD spacer oxide is deposited. Since the space between the gate and capacitor polysilicon is fully filled with oxide, no spacer formation occurs at this region. Therefore, no impurities arrive in the active region during high-dose implantation due to low energy. In this case, a salicide layer is also not formed in the

storage node junction during the salicide process while it is formed on the bit line junction, word line, and capacitor plate. The LDD junction with non-salicidation used in this study is similar to that of the conventional DRAM for minimizing the leakage current.

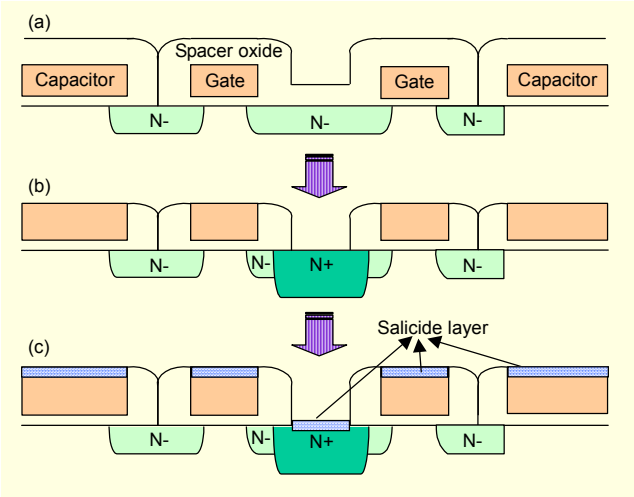



Fig. 2. Process flow to reduce the leakage current in the storage node contact. (a) Deposition of a spacer oxide after N-LDD implantation. (b) After spacer oxide etching. Note that the spacer is not formed on the storage node due to the gap fill. (c) After N+ implantation and salicide formation.

In this cell, a MOS capacitor takes a 43.7% portion of the cell area; therefore, the leakage current under the capacitor area is one of the major factors to reduce the refresh time. In a "0" data state, an electron inversion layer is formed under the capacitor plate, while in a "1" data state, a deep depletion region is formed. The "0" and "1" data states are erased and written states, respectively. The "0" state is stable because the electron inversion layer is maintained in an equilibrium state. On the other hand, the "1" data state is unstable because the deep depletion region under the capacitor plate tends to be converted to an electron inversion state ("0" state) as time goes on due to the leakage current from the P-well or storage node junction to the deep depletion region. To improve the refresh characteristics of the "1" data state, a Hi-C structure is used in the capacitor region in order to suppress the leakage current under the capacitor plate. The Hi-C structure is formed by phosphorus implantation before the capacitor dielectric oxide is grown.

As mentioned, a 0.25 μm logic process is used for fabrication. First, after the patterning of shallow trench isolation using lithography and reactive etching, a thick oxide is deposited and planarized using chemical-mechanical polishing. The shallow trench isolation depth is 0.35 μm. Then, a well formation is followed using the normal logic process flow. After that, the capacitor area in the memory cell array is opened using lithography, and Hi-C implantation is performed. Next, after removal of the photo resist, a gate oxide having a 45 Å physical thickness is thermally grown. Finally, after deposition of the polysilicon used for both the capacitor electrode and gate, the normal logic process flow is followed for fabrication.

## III. Cell Characteristics and Discussion

In DRAM operation, cells lose their charge stored in the capacitor for various reasons. One reason is the leakage current from the capacitor itself as well as from the access transistor, which bring about a direct effect on the charge loss of the cell. As mentioned earlier, the leakage current is minimized by optimization of the process and cell design. Noises from the well and peripheral circuits are minimized by using a deep N-well. The leakage current under the capacitor at a "1" data state is minimized by using a Hi-C structure to 1/10 the level, which is confirmed on the wafer. The leakage current from the access transistor is minimized to less than 1/1000 of that of the logic transistor by raising the cell threshold voltage to up to 1.0 V. With the above optimization, the leakage current from the deep depletion regions ("1" data state) under the capacitor plate and access transistor channel are 80 fA/cell and 70 fA/cell at 85°C, respectively. The sum of the leakage current from the capacitor LDD junction and through the capacitor dielectric oxide is less than 10 fA/cell at 85°C, which takes a minor part in the total leakage current. Another source for losing cell charge is instant noise due to voltage fluctuation of the adjacent conducting lines by the capacitive coupling between them. In a read operation, a bit line is in a floating state and thus affected by the voltage fluctuation of the adjacent bit lines. In this process, metal 1 is used as a bit line, and a logic gate is used for a word line as well as a cell capacitor plate. Note that metal 1 thickness is 0.45 μm, which is about twice that of the bit line in conventional DRAM. A thick metal bit line not only brings about capacitive coupling noise due to an increased fringe capacitance, but also increases the bit line capacitance itself. The coupling noise due to the voltage fluctuation of the adjacent bit lines can be affected by the data type of the adjacent cell. The dependency on the data type of the adjacent cell is determined by measuring the disturb characteristics. As shown in Fig. 3, check board patterns A and B give the worst data patterns during refreshing; thus, they are used for a disturb test. In check board pattern A, the adjacent bit lines have the opposite voltage to each other in a read operation. Note that a word line maintains itself for 8.5 ms during the disturb test and that bit lines are biased to 0 V or 1.8 V, respectively, during the measurement time. If a cell that belongs to a bit line with 1.8 V has "0"data, the cell easily loses the "0" data through the channel

leakage current for 8.5 ms. The opposite case results in a similar situation. In this case, the voltage difference between the bit line node and storage node of the cell transistor is 1.8 V. In a non-disturb test, the voltage difference is only 0.8 V because the bit lines have 0.9 V. During a sensing operation, the bit line is in a floating state with a precharge voltage (Vblp) of 0.9 V, which is chosen using half the voltage of the "1" data (1.8 V).

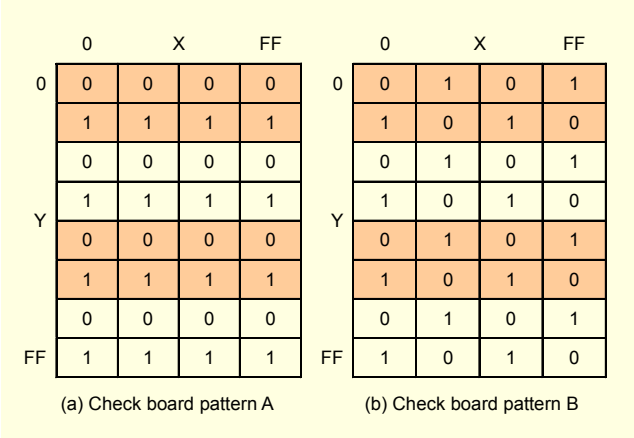



Fig. 3. Check board pattern used to test the refresh characteristic.

In a DRAM cell operation, the sensing voltage (ΔV) after charge sharing is given by

$$\Delta V = (V_s - V_{blp}) / (1 + C_b/C_s), \quad (1)$$

where $V_s$ is voltage in the storage node, $V_{blp}$ is the bit line pre-charge voltage, $C_s$ is cell capacitance, and $C_b$ is total bit line capacitance. Note that ΔV in (1) is the case in which the bit lines are not in a floating state. $C_b$ can be expressed as follows:

$$C_b = C_j + C_c + C_g, \quad (2)$$

where $C_j$ is the capacitance between the junction of the bit line contact to the well, $C_c$ is the capacitance between adjacent bit lines, and $C_g$ is the capacitance between bit lines and other conducting lines. If two conducting lines, X,Y, are in parallel while electrically floating, the voltage change (+ΔV) in line X shifts the voltage of line Y by (+ΔV)*($C_{xy}/C_y$), where $C_x$ is the capacitance of line X, $C_y$ is the capacitance of line Y, and $C_{xy}$ is the coupling capacitance between bit line X,Y. Thus, during a sensing operation when the charge in the cell capacitor is shared with the bit line, the resultant sensing voltage ΔV is affected by the voltage change of the adjacent two bit lines, and the magnitude ($V_{noise}$) in the worst case is

$$V_{noise} = 2\Delta V(C_c/C_b). \quad (3)$$

Note that (3) is relevant only when the bit lines are in a floating state. The worst case is the situation in which all cells in the bit line have the opposite data of the cells of the adjacent bit lines, as shown in Fig. 3(b). In the worst case, the net sensing $\Delta V_{net}$ considering the bit line coupling noise is

$$\Delta V_{net} = \Delta V^*( 1\text{-}2(C_c/C_b) ). \quad (4)$$

To investigate the effect of an inserted ground metal line between bit lines, two types of cells are fabricated: one is with an inserted ground line, the other is without a ground line. Table 1 shows the results of our simulation and measurement. For the simulation, a Raphael simulation is used with the equations given above. As shown, $C_b$ is increased from 37.6 fF to 40.5 fF with the addition of a shielded line. However, $C_c$ is dramatically reduced from 5.98 fF to 0.25 fF when the shielded line is added. This implies that the noise margin is improved by 96% with the addition of the shielded line. This is confirmed by measuring the test pattern in the silicon wafer. For the measurement, an LCR meter (Hewlett-Packard, Model 4284A) is used with a 8 kb cell array test pattern. The increase of $C_c$ results in Vnoise which is calculated from (3). $V_{noise}$ is significantly reduced from 60.1 mV to 2.2 mV when the ground line is inserted. Therefore, although total bit line capacitance is slightly increased with the addition of the ground line, the actual sensing margin voltage ($\Delta V_{net}$) is increased from 129 mV to 176 mV due to the reduction of noise voltage between the bit lines.

Table 1. Results of simulation and the measurement of bit line capacitances and sensing margins.

| | No shield | | With shield | |
|---|---|---|---|---|
| | on wafer | simulation | on wafer | simulation |
| $C_b$ (fF/BL) | 40 | 37.6 | 44 | 40.5 |
| $C_c$ (fF/BL) | - | 5.98 | - | 0.25 |
| $C_s$(fF/cell) | 9.0 | 10 | 9.0 | 10 |
| $C_b/C_s$ | 4.44 | 3.76 | 4.89 | 4.05 |
| $\triangle V_{initial}$ | 165 | 189 | 153 | 178 |
| $\triangle V_{noise}$ | - | 60.1 | - | 2.2 |
| $\triangle V_{total}$ | - | 129 | - | 176 |

The refresh time of memory cells is evaluated at 85°C with a memory tester (Teradyne, Model J997). To characterize the cell, several test vectors are used. A March-X test is performed to screen the initial hard fail, while a March-Y test is used to evaluate the refresh time. A disturb test is performed to check the disturbance effect of the adjacent cell when a word line maintains a turn-on state for 8.5ms. Note that this test is repeated at 2.2 V, 2.5 V, and 2.8 V, respectively, to check the voltage margin. Also, to check the sensitivity of voltage fluctuation during the sensing operation, a bump test is

performed. A bump up test is used to read data at 2.8 V after writing data on the cell at 2.2 V. A bump down test is used to read data at 2.2 V after writing data on the cell at 2.8 V. The March-X and March-Y patterns are used to test the cell array in which the cell is accessed in the x-address first and y-address first, respectively. It appears that the bump up characteristic is weaker than the bump down. There are two reasons for this. First, there is a relatively smaller charge stored in the cell during the bump up test than in the bump down test since a lower $V_{cc}$ generates a smaller charge. Second, since the capacitor plate is biased to $V_{cc}$, the voltage of the capacitor plate is raised from 2.2 V to 2.8 V when $V_{cc}$ is increased from 2.2 V to 2.8 V during the bump up test. This increment of 0.6 V in the cell plate also shifts the cell voltage 0.6 V and thus, if the cell is in a "0" data state, charge loss occurs. Cell voltage means the voltage under the capacitor plate which is in a floating state during a read operation. Since the cell junction is under the capacitor plate with the floating state during a read operation, the voltage change of the capacitor plate induces a voltage change of the cell junction. Table 2 shows the effect of an inserted ground line on the refresh time and bump margin of a 1 Mb DRAM chip. As shown, the refresh time is increased about 33%. Also, the bump up margin is improved from 2.8 V to 3.0 V. Figure 4 shows the corresponding Shmoo data.

Table 2. Comparison of measured refresh time and bump margin with/without ground metal line.

| @ 85C, 2.2V | tREF | Bump up | Bump down |
|---|---|---|---|
| Without shielded B/L | 8−10ms | 2.2V→2.8V | 3.0→2.2V |
| With shielded B/L | 12−16ms | 2.2V→3.0V | 3.0→2.2V |

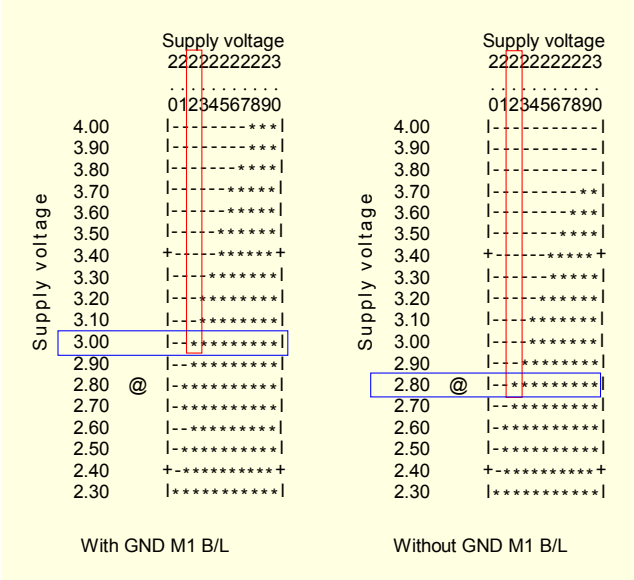



Fig. 4. The Shmoo characteristics of a 1 Mb test chip with/without ground metal line.

## IV. Conclusion

In this study, it is shown that a shielded metal line inserted between adjacent bit lines is effective to increase the refresh time and noise margin of a planar DRAM cell. The DRAM cell consists of an access transistor which is biased to 2.5 V during operation and an NMOS capacitor having a capacitance of 10 fF per unit cell. Its cell size is 3.63 $\mu m^2$. The cell is optimized to minimize the leakage current. Hence, the channel length of the cell transistor is optimized to 0.31 μm at which the reverse short channel effect is maximized. Also, no high-dose implantation is performed on the storage node region, which blocks silicidation on that region. A single Mb DRAM is designed with an open bit line structure. It appears that the refresh time is increased from 4.5 ms to 12 ms when a shield metal line is inserted. Also, it appears that no failure occurs when $V_{cc}$ is increased from 2.2 V to 3 V during a bump up test, while it fails at 2.8 V without a shield metal line.

## References


[1] Y.H. Park, S.H. Han, J.H. Lee, and H.J. Yoo, "A 7.1 GB/s Low-Power Rendering Engine in 2D Array Embedded Memory Logic CMOS for Portable Multimedia System," *IEEE J. Solid-State Circuits*, vol.36, 2001, pp. 944-955.

[2] W. Kim, "A Platform-Based SoC Design of a 32-Bit Smart Card," *ETRI J.*, vol. 25, no. 6, Dec. 2003, pp.510-516.

[3] S. Lee, "Pipelined Macroblock Processing to Reduce Internal Buffer Size of Motion Estimation in Multimedia SoCs," *ETRI J.*, vol. 25, no. 5, Oct. 2003, pp.297-304.

[4] D.H. Suh and J.H. Lee, "A Process Technology for 0.16μm Embedded DRAM with Fast Logic Speed and Small DRAM Cell," *J. Electrochem. Soc.*, vol. 151, 2004, pp. G618-622.

[5] Y.J. Kim, J.H. Lee, Y.C. Jeong, and J.H. Cho, "Investigation of a Relationship between Refresh Time and Implantation Overlap in Capacitor Region of P-MOS DRAM Cell," *Microelectronic Eng.*, vol. 71, 2004, pp. 262-265.

[6] D.H. Suh, J.H. Cho, Y.C. Jeong, S.Y. Chi, J.G. Park, Y.J. Kim, and J.H. Lee, "Characterization of 3 Dimensional Capacitor Prepared by Oxide Recess in Shallow Trench Isolation," *J. Electrochem. Soc.*, (in press).

[7] Dong-Sun Min and Dietrich W. Langer, *Senior Member, IEEE*, "Multiple Twisted Dataline Techniques for Multigigabit DRAM's," *IEEE J. Solid-State Circuits*, vol. 34, 1999, pp. 856-865.

[8] H. Hidaka, F. Fujishima, Y. Matsuda, M. Asakura, and T.

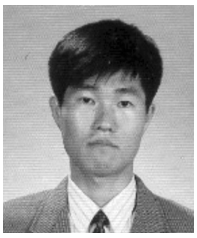
Yoshihara, "Twisted Bit-Line Architecture for Multi-Megabit DRAM's," *IEEE J.Solid-State Circuits*, vol. 24, 1989, pp. 21-28.

[9] M. Aoki, M. Horiguchi, and K. Itoh, "An Experimental 16-Mbit DRAM with Transposed Data Line Structure," *ISSCC Dig. Tech. Papers*, 1998, pp. 250-251.

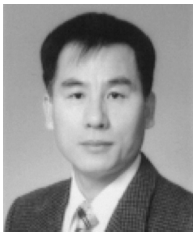
[10] W. Leung and F. C. Hsu, "Method and Apparatus for Complete Hiding of the Refresh of a Semiconductor Memory," US Patent #5,999,474, 1999.

[11] M. Hashimoto, K. Abe, and A. Seshadri, "An Embedded DRAM Module Using a Dual Sense Amplifier Architecture in a Logic Process," *ISSCC Dig. Tech. Papers*, 1997, pp. 64-65.

**Junghwan Lee** received the PhD degree in chemical engineering from Drexel University, Philadelphia, PA, in 1996, the MS degree from Korea Advanced Institute of Science and Technology (KAIST), Seoul, Korea in 1985, and the BS degree from Hanyang University, Seoul, Korea, in 1983. In 1989, he joined Hynix Semiconductor Inc., where he had been engaged in development of 4M, 16M, and 64M DRAM as a process integration engineer. Since 1996, he has been Team Leader for the development of embedded memories such as embedded DRAM, Flash, and EEPROM. Before joining MagnaChip Semiconductor, Inc. (formerly Hynix Semicondutor's System IC Business), he had worked as a device researcher for Samsung Electronics during 1985-1988. During that time period, his duty was to develop SRAM devices such as 16 k, 64 k, and 256 k SRAM.



**Seongdo Jeon** was born in Korea in 1964. He received the BS degree in 1987 and MS degree in 1990 in physics from Hanyang University, Seoul, Korea. In 1994, he joined the Semiconductor R&D Center, Hynix Semiconductor Inc., Korea, where he has participated in the development of 16M and 64M DRAM as a process and device engineer. Since 1998, he has been with the System IC R&D Center of MagnaChip Semicondutor, Inc., Cheongju, Korea, where he works on SoC device development and process integration. His major interests are in the electrical characteristics of various SoC devices.



**Sung-Keun Chang** was born in Kyungnam, Korea, in 1962. He received the BS degree in electronic engineering from Kyungpook National University, Daegu, in 1984, and the MS and PhD degrees in electronics and electrical engineering from Pohang University of Science and Technology, Pohang, in 1993 and 1996, respectively. In 1996, he joined the memory research division, Hyundai Electronics Industries Co., Ltd. in Ichonsi, Korea, where he worked on the development of a deep-submicron DRAM memory process and MOS device design for giga bit DRAM technology. In 2000, he moved to Chungwoon University, where he is currently a Professor in the Department of Electronics Engineering. His research interests are focused on devices and circuits design for SoC and display devices.