Switched-Capacitor Variable Gain Amplifier with Operational Amplifier Preset Technique

Young-Kyun Cho, Young-Deuk Jeon, and Jong-Kee Kwon

ABSTRACT—We present a novel operational amplifier preset technique for a switched-capacitor circuit to reduce the acquisition time by improving the slewing. The acquisition time of a variable gain amplifier (VGA) using the proposed technique is reduced by 30% compared with a conventional one; therefore, the power consumption of the VGA is decreased. For additional power reduction, a programmable capacitor array scheme is used in the VGA. In the 0.13 μm CMOS process, the VGA, which consists of three-stages, occupies 0.33 mm^2 and dissipates 19.2 mW at 60 MHz with a supply voltage of 1.2 V. The gain range is 36.03 dB, which is controlled by a 10-bit control word with a gain error of ±0.68 LSB.

Keywords—VGA, op-amp, preset technique, acquisition time.

I. Introduction

Variable gain amplifiers (VGAs) with a dB-linear gain control are a key building block for the analog front end (AFE) of image sensor interfaces, which are used to accommodate a large dynamic range of signals [1]-[5]. Recently, the more the number of pixels in the sensors is increased, the more power consumption is required to operate the AFE at higher speed. Therefore, designing a wide bandwidth and high linearity VGA with low power dissipation is a real challenge. Conventional switched-capacitor (SC) VGAs have a long slew period to settle and high power consumption to reduce the acquisition time.

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In this letter, a novel operational amplifier (op-amp) preset technique based on an SC architecture is discussed. The proposed technique reduces the acquisition time by improving the slewing and power consumption. As a test vehicle for the proposed technique, a VGA using a programmable capacitor array was implemented.

II. Operational Amplifier Preset Technique

The proposed op-amp preset technique is shown in Fig. 1. It uses a two-stage op-amp with folded-cascode and common source architectures to obtain a high DC gain and large output swing [6]. Switches SW4, SW5, SW6, and capacitor C_I are added to implement the proposed technique in the conventional circuit. Capacitor C_P is the sum of the parasitic capacitances at node T2, and C_L is the load capacitor of the second-stage op-amp output. In conventional SC op-amps, the input signal is sampled on the sampling capacitor, C_s, while the feedback capacitor, C_F, is discharged to the common mode voltage, V_{CM}, during the sampling phase, Q1. The second-stage op-amp is simply reset to V_{CM} and does not contribute any functionality. The proposed technique resets the second-stage op-amp to around the settling value during Q1, which improves the

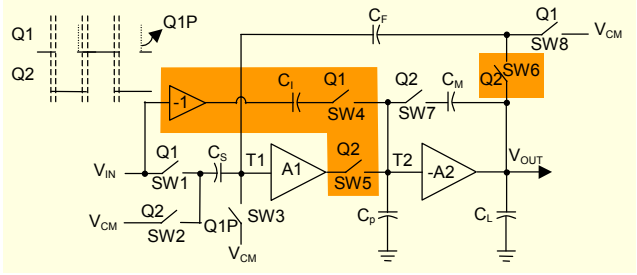

Fig. 1. Op-amp preset technique based on the SC architecture.

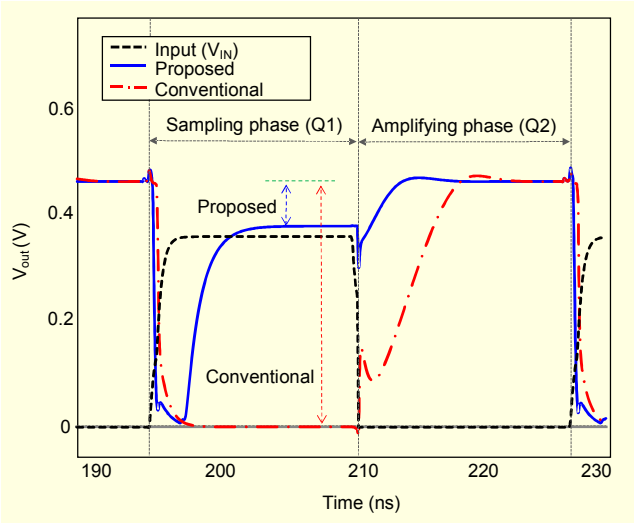

Fig. 2. Comparison of proposed and conventional techniques.

slewing of the op-amp. During Q1, the analog input signal is sampled on C_S by the clock Q1P. At the same time, in order to operate only the second-stage op-amp, SW4 is turned on, and SW5 and SW6 are turned off. Then, the analog input is applied to C_I through the inverting op-amp with a DC gain of –1 and is divided by the ratio of C_I and C_P at node T2. The inverting op-amp is easily implemented by the cross-coupled connection of the differential input.

The voltage of T2, V_{T2}, is amplified by the DC gain of the second-stage op-amp, –A2; therefore, the output voltage during Q1, V_{OUT_Q1}, is given by

$$V_{OUT\_Q1} = -A2 \times V_{T2} = A2 \times V_{IN} \times C_I / (C_I + C_P). \quad (1)$$

Voltage V_{OUT_Q1} can be controlled by C_I as C_P and A2 are decided on the circuit.

During the amplifying phase, Q2, the switches SW2, SW5, SW6, and SW7 are turned on, and the sampled analog input is amplified by the ratio of C_F and C_S as in a conventional circuit. In this case, the amplified output moves from V_{OUT_Q1}. Thus, the acquisition time of the SC op-amp is decreased because of the reduced slewing time, and low power consumption can be achieved.

The simulated output waveform of the proposed SC op-amp is compared with a conventional one in Fig. 2. The parameters used in this simulation are C_S=C_L=4 pF, C_I=295 fF, and C_F=3.1 pF. The results show that the proposed technique reduces the acquisition time of the op-amp by about 30% at 60 MS/s without additional power consumption.

III. Three-Stage VGA with PCA

Figure 3 shows a block diagram of the VGA for the AFE of image sensor interfaces. The op-amp preset technique was

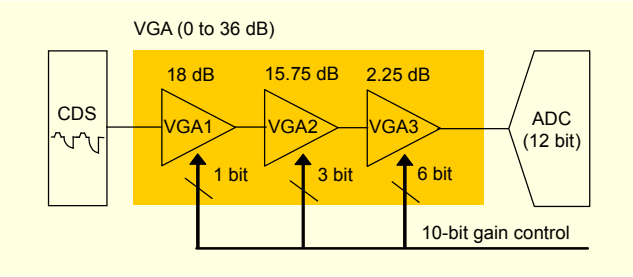

Fig. 3. Block diagram of the VGA in the image sensor interface.

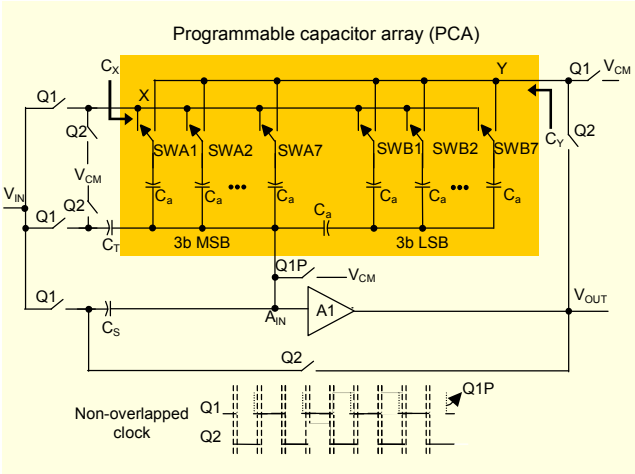

Fig. 4. Proposed VGA3 topology with a programmable capacitor array.

applied to a VGA. The VGA is composed of three stages for a 36 dB gain range. The gains of VGA1 and VGA2 are changed by selecting feedback capacitors with 18 dB steps of a 1-bit digital code and 2.25 dB steps of a 3-bit digital code, respectively. In the circuits, the Miller capacitors are digitally controlled to compensate the –3 dB bandwidth, $f_{-3\,dB}$, and phase margin variations that are caused by changing the feedback factor. The gain of VGA3 is 2.25 dB with 0.035 dB steps depending on the 6-bit LSBs.

Figure 4 shows VGA3 with the proposed programmable capacitor array (PCA) used to minimize the number of capacitors and switches. The PCA can adjust a dB-linear gain that follows the first order approximation $(1+x)/(1-x)$ [2], [3]. It is composed of the unit capacitor array, which is segmented between the upper 3-bit and lower 3-bit capacitors by a split capacitor. The value of the unit capacitor is 60 fF. In the PCA, the capacitors connected between nodes X and A_{IN} are indicated to C_X, and the capacitors connected between nodes A_{IN} and Y are indicated to C_Y. The total capacitance (=C_X+C_Y) of the PCA is identical to the capacitance of C_T. In Q1, the analog input signal is sampled on C_S, C_T, and C_X. The remaining capacitors C_Y of the PCA are connected to V_{CM}. In Q2, the bottom plates of C_S and C_Y are connected to the

op-amp output and C_T and C_X are connected to V_{CM}. Therefore, the voltage gain of VGA3 can be expressed as $(C_S+C_T+C_X)/(C_S+C_T-C_X)$. Due to the additional capacitor, C_T, the VGA3 has a larger feedback factor of $(C_S+C_T-C_X)/(C_S+2\times C_T)$, which reduces power consumption and kT/C noise compared with a conventional one [2].

IV. Experimental Results

The prototype VGA was fabricated in a 0.13 μm 1P6M CMOS process as shown in Fig. 5. The proposed three-stage VGA occupies an active area of 0.33 mm^2 and consumes 19.2 mW at a supply voltage of 1.2 V and a sampling frequency of 60 MHz. Figure 6 shows the measured gain and gain errors against a 10-bit control word. The proposed VGA offers 36.03 dB of dB-linear gain control range with 0.0352 dB gain steps and a gain error of less than ±0.68 LSB. The proposed VGA and previously reported VGAs are compared in Table 1. The proposed VGA has a larger dynamic range, a higher operating speed, and lower power consumption than conventional VGAs.

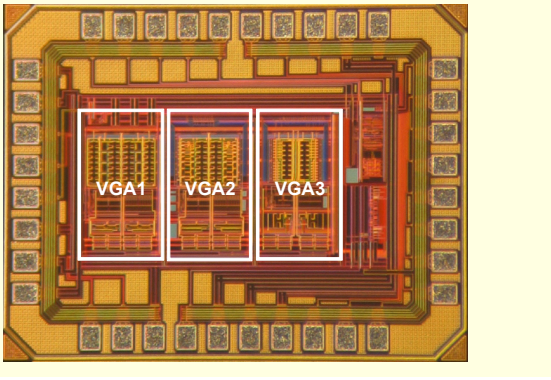

Fig. 5. Chip photograph.

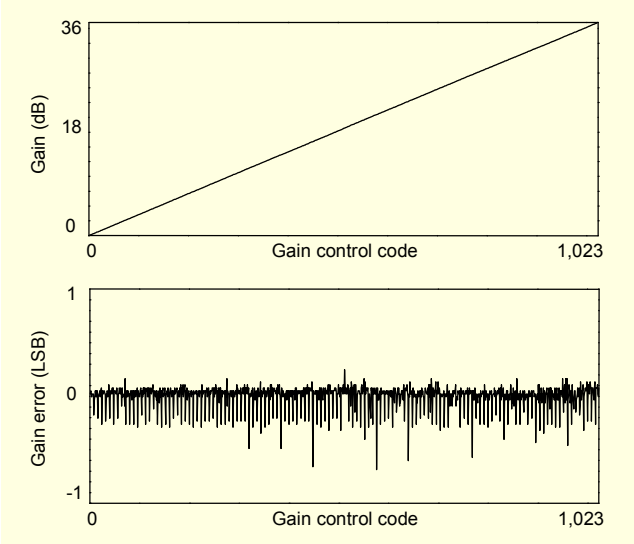

Fig. 6. Measured gain and gain error against 10-bit control word.

Table 1. Comparison of reported VGAs.

Reference	Dynamic range (dB)	Sampling rate (MHz)	Gain resolution (bit)	Power consumption (mW)
[1]	32	25	8	approx. 138
[2]	18	33	9	-
[3]	24	18	8	18.7
This work	36	60	10	19.2

V. Conclusion

A novel op-amp preset technique for an SC circuit is proposed and implemented with a VGA for low-power applications. The reduced op-amp acquisition time decreases the power consumption of the VGA. An additional reduction of the power consumption can be achieved by the PCA scheme. The proposed circuits are expected to be useful in the design of an analog front end and other analog signal processing applications.

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