A VLSI Architecture for Novel Decision Feedback Differential Phase Detection with an Accumulator

Chang-kon Kim, and Jong-wha Chong

This paper proposes a novel decision feedback differential phase detection (DF-DPD) for M-ary DPSK. A conventional differential phase detection method for M-ary Differential Phase Shift Keying (DPSK) can simplify the receiver architecture. However, it possesses a poorer bit error rate (BER) performance than coherent detection because of the prior noisy phase sample. Multiple-symbol differential detection methods, such as maximum likelihood differential phase detection, Viterbi-DPD, and DF-DPD using L–1 previous detected symbols, have attempted to improve BER performance. As the detection length, L, increases, the BER performance of the DF-DPD improves but the complexity of the architecture increases dramatically. This paper proposes a simplified DF-DPD architecture replacing the conventional delay and additional architecture with an accumulator. The proposed architecture also improves BER performance by minimizing the current differential phase noise through the accumulation of previous differential phase noise samples.

The simulation results show that the BER performance of the proposed architecture approaches that of a coherent detection with differential decoding.

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I. INTRODUCTION

Among the different methods for digital radio communication, *M*-ary phase shift keying (*M*-ary PSK), which modulates and demodulates the signal by using phase, has been widely used for various applications. Demodulating *M*-ary PSK modulated signals requires a process that recovers a synchronous carrier signal to demodulate the received signal in a receiver. Thus, the *M*-ary PSK receiver adopts a module for carrier recovery such as the Costas loop. Under modest channel conditions such as a Gaussian noise environment, coherent detection would be considered the most suitable. However, the receiver with a complex coherent circuit is so complicated that its implementation is difficult. For noncoherent detection, *M*-ary DPSK uses phase differences in symbols for modulation and demodulation. The receiver of *M*-ary DPSK can be simplified and fabricated at low cost because *M*-ary DPSK uses a previous signal as a phase reference in demodulation. Due to such advantages, *M*-ary DPSK has been widely used for several receivers. However, the bit error rate (BER) performance of *M*-ary DPSK is inferior to that of coherent detection. Recent investigations have proposed a variety of multiple symbol differential detection methods using *L* consecutively received signals during the detection length to improve BER performance. These include maximum likelihood differential detection (ML-DD) [1], ML-DD using the Viterbi decoder (Viterbi-DD) [2], and decision feedback differential detection (DF-DD) [3], [4]. However, ML-DD and Viterbi-DD are generally too complicated to be implemented. For ease of implementation, decision feedback differential phase detection (DF-DPD), which uses the phase difference between symbols, has been suggested.

Though the structure of DF-DD is considerably better than ML-DD and Viterbi-DD, it still needs further structural im-

provement [7]-[11].

Thus, one architecture which has relatively low complexity compared to DF-DD was proposed [6]. That scheme modifies DF-DPD into a DPD for which the phase reference can be generated using a simple recursive structure. However, to obtain the same performance as that of the coherent detection scheme, it needs a more complex structure.

In this paper, we review previously proposed methods and propose a novel DF-DPD method which can maintain a performance similar to that of the coherent detection scheme while using a simpler architecture than those of the previously proposed methods. To evaluate the performance of the proposed novel DF-DPD method, we apply it to a DQPSK modulator and demodulator.

II. CONVENTIONAL DPDs

1. Differential Phase Detection

M-ary DPSK is an *M*-ary PSK method that adopts the process of differential encoding and decoding in noncoherent detection. The phase demodulation of the received signal through differential decoding is called differential phase detection (DPD).

Conventional differential phase detection detects the current received phase as follows: The received differential phase $\Delta\psi_n$ is obtained and then compared to the reference phases $\Delta\phi_m|_{m=1,2,\cdots,M}(=2(m-1)\pi/M)$. The differential phase $\Delta\bar{\phi}_n$ in the receiver is the reference phase $\Delta\phi_m|_{m\in\{1,2,\cdots,M\}}$ that is adjacent to $\Delta\psi_n$. The process can be summarized as

$$\Delta\bar{\phi}_n = \min_{over\Delta\phi_m}|\Delta\eta_m| = \min_{over\Delta\phi_m}|\Delta\psi_n - \Delta\phi_m|, \qquad (1)$$

where $\Delta\eta_m = \Delta\psi_n - \Delta\phi_m$.

The architecture of the conventional DPD described by (1) is shown in Fig. 1.

2. Decision Feedback Differential Phase Detection

The DF-DPD algorithm proposed by Adachi and Sawahashi uses *L* consecutively received symbols while the conventional DPD takes only a current phase and one previous phase [4]. The decision rule of the DF-DPD is given by

$$\begin{aligned}\Delta\bar{\phi}_n &= \min_{over\Delta\phi_m}\sum_{l=1}^{L}\mu_l^{\,2} = \min_{over\Delta\phi_m}\sum_{l=1}^{L}|\mu_l| \\ &= \min_{over\Delta\phi_m}\left(|\Delta\eta_m| + \sum_{l=2}^{L}\left|\Delta\eta_m + \sum_{i=2}^{l}\Delta\bar{\eta}_{n-i+1}\right|\right) \\ &= \min_{over\Delta\phi_m}\left(|\Delta\psi_n - \Delta\phi_m| + \sum_{l=2}^{L}\left|(\Delta\psi_n - \Delta\phi_m) + \sum_{i=2}^{l}(\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1})\right|\right),\end{aligned}$$

where $\Delta\bar{\eta}_{n-i+1} = \Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1}$, $\mu_l = \Delta\eta_m + \sum_{i=2}^{l}\Delta\bar{\eta}_{n-i+1}$.

(2)

In (2), $\Delta\bar{\phi}_n$ is the reference phase, $\Delta\bar{\phi}_m|_{m\in\{1,2,\cdots,M\}}$, that minimizes the sum of absolute values of $\mu_l|_{l=1,2,\cdots,L}$, the phase noises of *l* DPD. The performance of DF-DPD is improved as the detection length, *L*, increases. When *L* is indefinite, the performance is the same as coherent detection with differential decoding.

III. A NOVEL DF-DPD

1. Algorithm

The characteristics of the DF-DPD get closer to those of co-

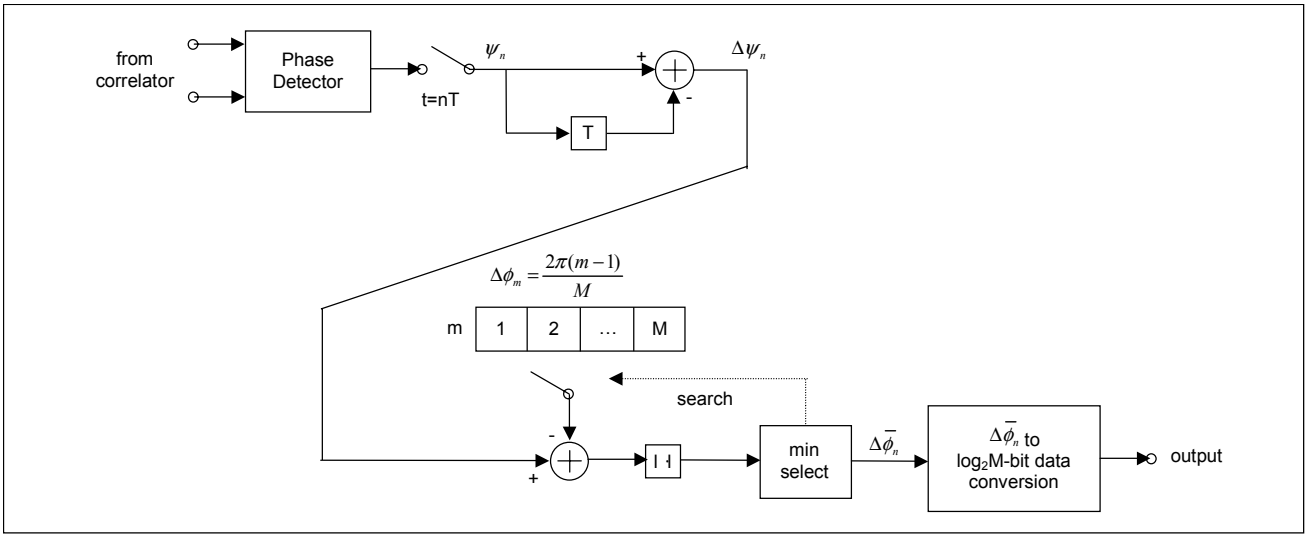

Fig. 1. Architecture of the conventional DPD.

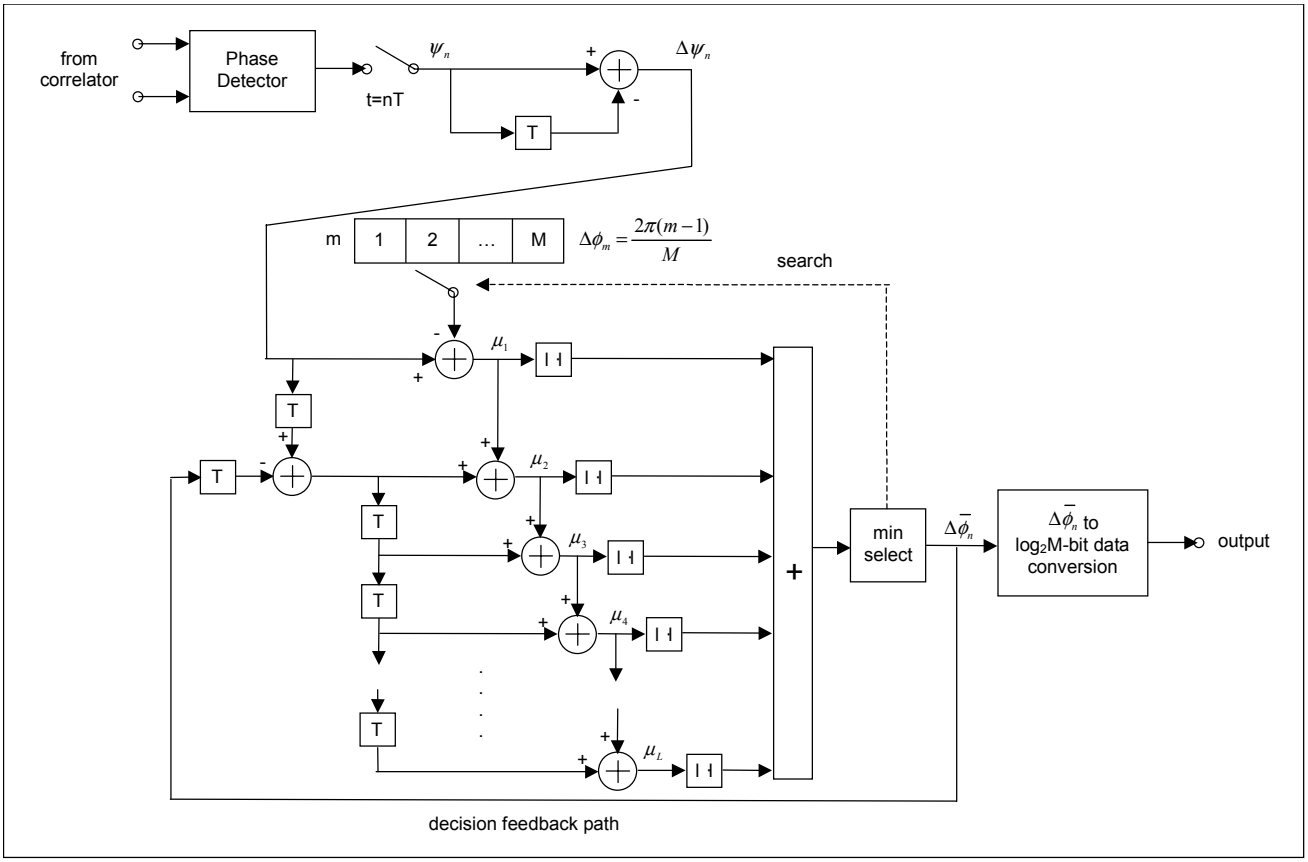

Fig. 2. Architecture of the DF-DPD.

herent detection as the detection length, *L,* increases. However, obtaining a recursive DF-DPD is difficult since the complexity increases rapidly compared to the differential detection as *L* increases. The proposed novel DF-DPD obtains a simple structure and superior BER performance by improving the structure of the conventional DF-DPD.

The decision rule of the conventional DF-DPD, as shown in (2), contains two principal characteristics. One is a differential phase noise μ_l of the *l*-th symbol DPD detector that includes the accumulation of previous differential phase noises $\left[\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1}\right]_{i=2,3,\cdots,l}$ as follows:

$$\begin{aligned}\mu_l &= \left(\Delta\eta_m + \sum_{i=2}^{l}\Delta\bar{\eta}_{n-i+1}\right) \bmod 2\pi \\ &= \left((\Delta\psi_n - \Delta\phi_m) + \sum_{i=2}^{l}(\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1})\right) \bmod 2\pi.\end{aligned} \tag{3}$$

The other is that the performance is improved as the detection length *L* increases. Combining these characteristics, the decision rule of the novel DF-DPD has a reduced hardware complexity. This reduced complexity results from the novel DF-DPD employing one DPD detector instead of *L* DPD detectors, which result in high complexity in the conventional DF-DPD. However, the DPD detector in the novel DF-DPD algorithm should still maintain two characteristics, the accumulative function and the adaptively increasing detection length *L*. In other words, the single DPD detector in the novel DF-detector possesses the accumulative function and the adaptively increasing detection length *L*. Here, the adaptively increasing detection length *L* is the length that accounts for all the symbols received. The detection length is the length that with *L* = *n* includes the symbols ranging from the first symbol to the current symbol received. Given those conditions, the accumulative DPD detector of the novel DF-DPD has the accumulative differential phase noise as follows:

$$\begin{aligned}\mu_n &= \left(\Delta\eta_m + \sum_{i=2}^{n}\Delta\bar{\eta}_{n-i+1}\right) \bmod 2\pi \\ &= \left((\Delta\psi_n - \Delta\phi_m) + \sum_{i=2}^{n}(\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1})\right) \bmod 2\pi.\end{aligned} \tag{4}$$

With the DPD detector, the decision rule of the novel DF-DPD with such characteristics can be written as

$$\Delta\bar{\phi}_n = \min_{over\Delta\phi_m} |\mu_n| = \min_{over\Delta\phi_m} \left| \Delta\eta_m + \sum_{i=2}^{n} \Delta\bar{\eta}_{n-i+1} \right|$$
$$= \left| (\Delta\psi_n - \Delta\phi_m) + \sum_{i=2}^{n} (\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1}) \right|. \quad (5)$$

2. Architecture

The novel DF-DPD only takes account of the absolute value of the differential phase noise of the single accumulative DPD detector while the conventional DF-DPD sums the absolute values of the L differential phase noises with L DPD detectors. In (5), representing the decision rule of the novel DF-DPD, $\sum_{i=2}^{n}(\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1})$ implies the accumulation of the previous differential phase noises. With the assumption that λ_{n-1} is the accumulation of $[\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1}]_{i=2,3,\cdots,n}$, the decision rule of the novel DF-DPD can be rewritten as

$$\Delta\bar{\phi}_n = \min_{over\Delta\phi_m} |\Delta\psi_n - \Delta\phi_m + \lambda_{n-1}|. \quad (6)$$

The architecture of the novel DF-DPD with the decision rule defined in (6) is shown in Fig. 3.

It is easy to note that the novel DF-DPD has a simple structure since the accumulative value λ_{n-1} is obtained with a single accumulator. The detection process is as follows. At first, the phase detector obtains the current received phase ψ_n, and the differential phase $\Delta\psi_n$ is evaluated for the current received phase as in the conventional DPD. The differential phase $\Delta\phi_n$ is then determined from the sum of $\Delta\psi_n - \Delta\phi_m|_{m\in\{1,2,\cdots,M\}}$ and λ_{n-1} in the novel DF-DPD, while the differential phase $\Delta\phi_n$ is determined with respect to the reference phase $\Delta\phi_m|_{m\in\{1,2,\cdots,M\}}$ that is closest to the current received differential phase $\Delta\psi_n$ in the conventional DPD.

3. Performance Prediction

The decision rule of the conventional DF-DPD uses the differential phase noise of L DPD detectors. This means that the differential phase noise plays an important role in determining the performance of the conventional DF-DPD. In the same way, the performance of the novel DF-DPD can be predicted by figuring out the effect of the accumulative differential phase noise λ_{n-1} of an accumulative DPD detector.

Assuming that the received phase is only dependent on the channel noise and the initial received phase noise η_0 is zero, and the current received differential phase $\Delta\psi_n$ is $\Delta\bar{\phi}_n$, μ_n can be defined as follows:

$$\mu_n = \left[(\Delta\psi_n(1) - \Delta\bar{\phi}_n) - \sum_{i=2}^{n} (\Delta\psi_{n-i+1}(1) - \Delta\bar{\phi}_{n-i+1}) \right] \bmod 2\pi$$
$$= \left[(\eta_n - \eta_{n-1}) + (\eta_{n-1} - \eta_{n-2}) + \cdots + (\eta_1 - \eta_2) \right] \bmod 2\pi$$
$$= (\eta_n) \bmod 2\pi. \quad (7)$$

From (7), it is clear that μ_n of the accumulative DPD detector in the novel DF-DPD is only a function of the current phase noise η_n. This means that $\phi_{n-1} + \theta$ does not include the previous phase η_{n-1}. In other words, the performance of

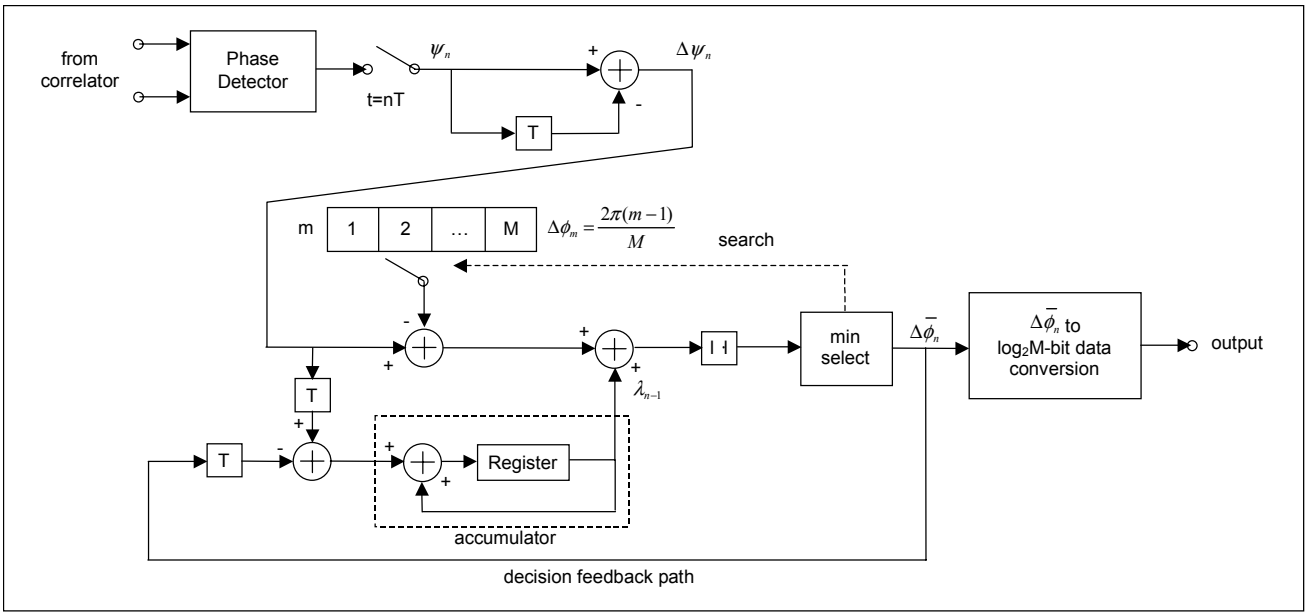

Fig. 3. Architecture of the novel DF-DPD.

the novel DF-DPD is similar to that of the coherent DPD with differential decoding. Thus, the performance of the novel DF-DPD should be better than that of other DPD schemes. Section IV gives the simulation results on the predicted performance.

IV. VLSI DESIGN OF NOVEL DF-DPD

1. Design Model

This section compares the computer simulation results of the conventional DPD, the DF-DPD ($L = 2, 4, 6, 8$), and the novel DF-DPD applied to a DPSK MODEM. To evaluate the effectiveness of both the algorithm and architecture of the novel DF-DPD, a computer simulation is done on the performance and the hardware complexity in the DPSK MODEM designed with the hardware description language (HDL).

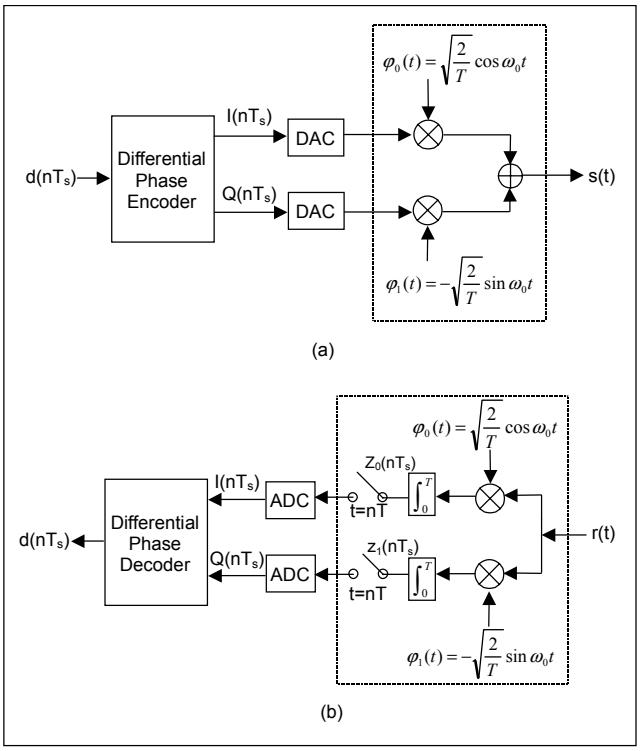

Fig. 4. Architecture of the DPSK MODEM.

Figure 4 shows how the PSK modulator and demodulator in the analog area are linked to the differential phase encoder and decoder in the digital area through a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC), respectively. At this time, the performance and complexity of the DPSK MODEM rely greatly on the amplitude resolution, that is, the number of quantization levels or bits of the DAC and ADC. The higher the level of quantization, the closer the digital signal processing approximates the analog signal processing

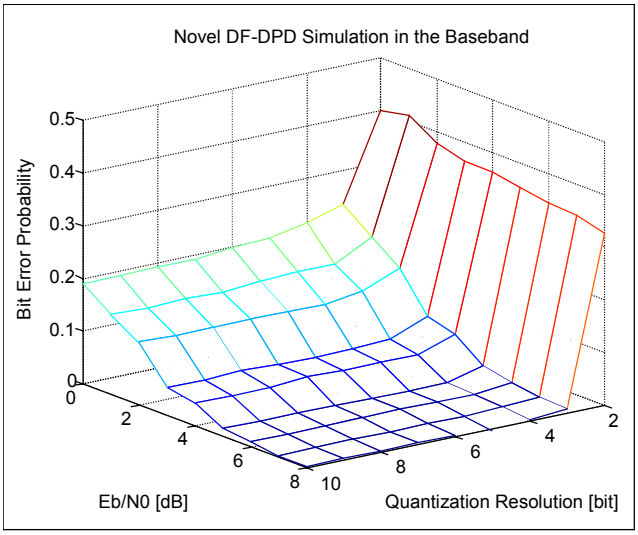

Fig. 5. Simulation result for obtaining the adequate quantization Resolution.

and the performance of the DPSK MODEM approximates the theoretical performance. However, the complexity increases with the number of bits. On the other hand, with fewer quantization levels, the DPSK modem complexity decreases, but the performance deteriorates. Thus, it is important to select the quantization resolution that assures both acceptable performance and low complexity. Figure 5 shows the simulation result for determining the optimum quantization resolution.

When the quantization resolution is higher than 4-bit, the bit error probability does not change much (Fig.5). Therefore, for constant performance and the lowest hardware complexity, the I-component and Q-component should be quantized at 4-bit.

Figure 6 shows the block diagram of the differential phase encoder and decoder of the differential encoded QPSK proposed in this paper.

The differential phase encoder in Fig. 6 (a) consists of a serial-to-parallel converter, phase mapper, differential encoder, and constellation mapper. The serial-to-parallel converter turns the serial data into a symbolic form. The phase mapper maps the symbol into the gray coded digitalized phase. Table 1 shows the phase mapping.

The differential encoder differentially encodes the digitalized phase. The constellation mapper takes as input the digitalized phase that is differentially encoded and provides as output the I-component and Q-component of a 4-bit resolution. Here, the I-component is an in-phase component of the phase and the Q-component is a quadrature component of the phase. Table 2 shows the constellation mapper.

The differential phase decoder shown in Fig. 6 (b) consists of a phase table, a differential phase detector, symbol decider, and parallel-to-serial converter. The phase table takes as input the

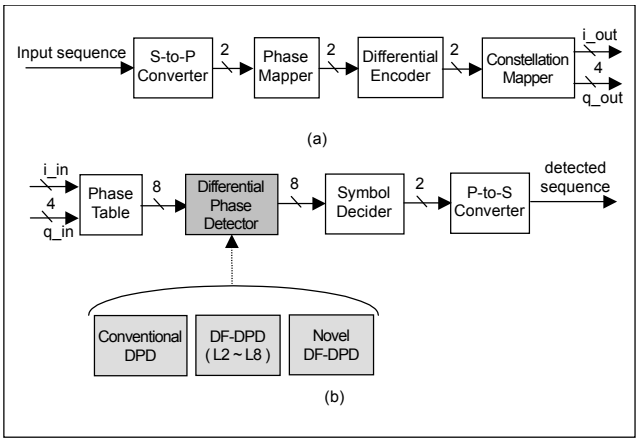

Fig. 6. Block diagram of the differential phase encoder and decoder for QDPSK.

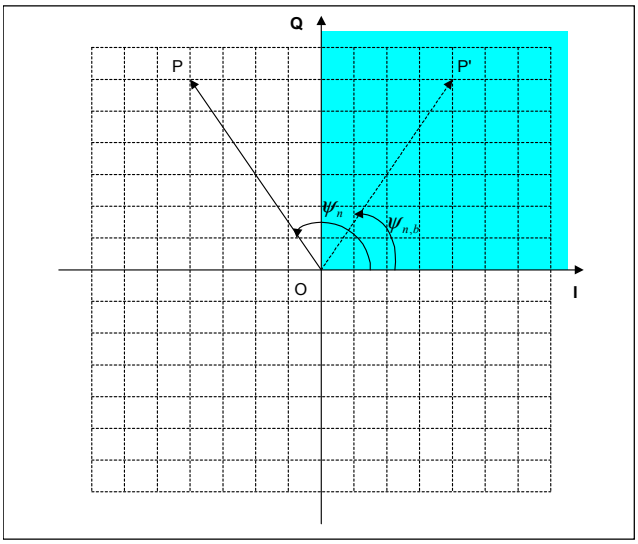

Fig. 7. Signal constellation for phase table.

Table 1. Phase mapping.

Symbol	Phase	Digitalized phase
0 0	0	0 0
0 1	π/2	0 1
1 0	–π/2	1 1
1 1	–π (π)	1 0

Table 2. Constellation mapping.

Digitalized Phase	Phase	(I, Q)	Digitalized (I, Q)
0 0	0	(1, 0)	(0111, 0000)
0 1	π/2	(0, 1)	(0000, 0111)
1 1	–π/2	(0, –1)	(0000, 1001)
1 0	π (–π)	(–1, 0)	(1001, 0000)

4-bit quantized values of the I-component and Q-component interrupted by the channel noise and provides as output the digitalized phases for each. In this manner, the phase table represents the digitalized phase having a quantized I-component and Q-component as the index. In this case, the number of bits for a digitalized phase is '8'; this can be obtained from Fig. 7, which shows the signal constellation for the phase table, and (8).

$$\begin{cases} ((7\times 7)-6-(2+1)\times 2)\times 4+4=152 \\ 7 \le \log_2 152 < 8. \end{cases} \quad (8)$$

The first equation in (8) shows possible cases of discrete phases that can be combined with the I-component and Q-component with a 4-bit resolution. The second equation decides the resolution of the digital value that can express all cases of the discrete phases.

For consistency with the differential phase decoder, the digitalized phases for 4 basic phases are shown in Table 3.

Building the table for all cases of the digitalized phases increases the hardware complexity. To reduce the hardware complexity according to the phase table, we use the symmetry of the phase in Fig. 7. We assume that ψ_n is the phase to be detected and that $\psi_{n,b}$ is the phase obtained from the absolute values of the I-component and Q-component. Here, two vectors of $\overrightarrow{OP}$ and $\overrightarrow{OP'}$ representing the angle are symmetrical on the Q-axis. Therefore, $\psi_n = \pi - \psi_{n,b}$ is obtained. This means that the phase with a particular I-component and Q-component can be expressed as the phase with an absolute I-component and absolute Q-component, as shown in (9). Using this relation, all of the digitalized phases can be represented by the table based on the shaded area in Fig. 7.

Table 3. Digitalized phases for the basic phases.

Quantized (I, Q)	Phase	Digitalized phase
(0111, 0000)	0	00000000
(0000, 0111)	π/2	01000000
(0000, 1001)	–π/2	11000000
(1001, 0000)	–π (π)	10000000

$$\begin{aligned}
\psi_n &= \psi_{n,b} && \text{for } 0 \le \psi_n < \pi/2 \\
\psi_n &= \pi - \psi_{n,b} && \text{for } \pi/2 \le \psi_n < \pi \\
\psi_n &= \pi + \psi_{n,b} && \text{for } -\pi \le \psi_n < -\pi/2 \\
\psi_n &= -\psi_{n,b} && \text{for } -\pi/2 \le \psi_n < 0
\end{aligned} \qquad (9)$$

$$\left(\text{where } \phi_n = \tan^{-1}\left(\frac{Q}{I}\right), \phi_{n,b} = \tan^{-1}\left(\frac{\text{abs}(Q)}{\text{abs}(I)}\right)\right).$$

The differential phase detector performs the process of DPD in which the digitalized phase is taken as input and the original digitalized phase is determined. Thus, this module is the main part of the simulation for investigating the effectiveness of the algorithm and architecture of the novel DF-DPD. The design of the differential phase detector for the novel DF-DPD is described in the next section.

The symbol detector converts the digitalized phase detected by DPD into the original symbol according to the Gray coding. The mapping for this is shown in Table 4. The parallel-to-serial converter changes the symbols into serial data.

Table 4. Symbol deciding.

Digitalized Phase	Phase	Symbol
00000000	0	0 0
01000000	π/2	0 1
11000000	–π/2	1 0
10000000	–π (π)	1 1

2. Design of Novel DF-DPD with Higher Data Rate

The differential phase detector of the *M*-ary DPSK demodulator obtains the difference between the currently received differential phase $\Delta\psi_n$ and each of the reference phases $\Delta\phi_m|_{m=1,2,\cdots,M}\ (=2\pi(m-1)/M)$. This means that one differential phase detection requires at least *M* clock triggers. However, the highest data rate is obtained with the smallest clock triggers. Thus, to operate the *M*-ary DPSK MODEM at the highest data rate, DPD should be completed with *M* clock triggers.

This paper explains the design of a differential phase detector that can obtain the currently determined differential phase $\Delta\bar{\phi}_n$ in *M* clock triggers, and especially the novel DF-DPD in an *M*-ary DPSK MODEM ($M \ge 4$).

The biggest difference between the DF-DPD and the conventional DPD is the decision feedback. Specifically, the currently determined differential phase $\Delta\bar{\phi}_n$ in the DF-DPD is fed back and $\Delta\psi_n - \Delta\bar{\phi}_n$ is then obtained. This is used to decide the next received differential phase $\Delta\psi_{n+1}$. This means that $\Delta\psi_n - \Delta\bar{\phi}_n$ should be included in the steps to decide $\Delta\psi_{n+1}$. Figure 8, which shows the operation of the novel DF-DPD on clock triggers, shows that $\Delta\psi_{n+1}$ is determined only after completing the cycle of *M* steps. This means that the process to obtain $\Delta\psi_n - \Delta\bar{\phi}_n$ cannot be inserted between the decision completion of $\Delta\psi_n$ and the decision start of $\Delta\psi_n - \Delta\bar{\phi}_n$. We still need to describe the design of the structure in which the decision of $\Delta\psi_n - \Delta\bar{\phi}_n$ is obtained before

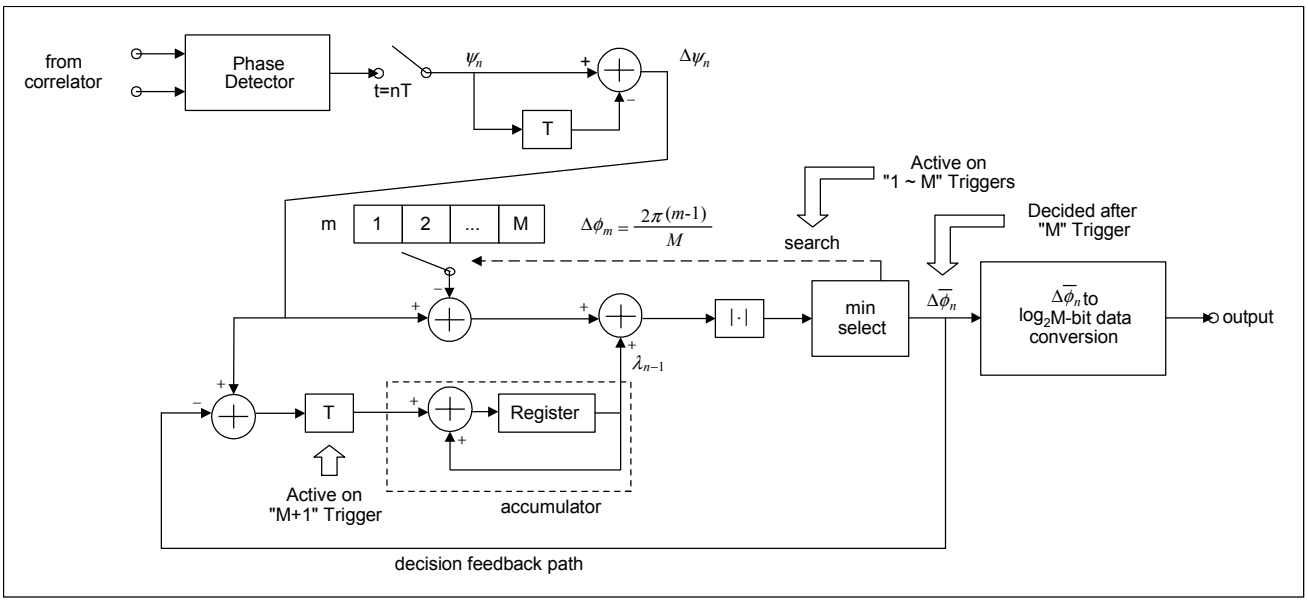

Fig. 8. Operation of novel DF-DPD on clock triggers.

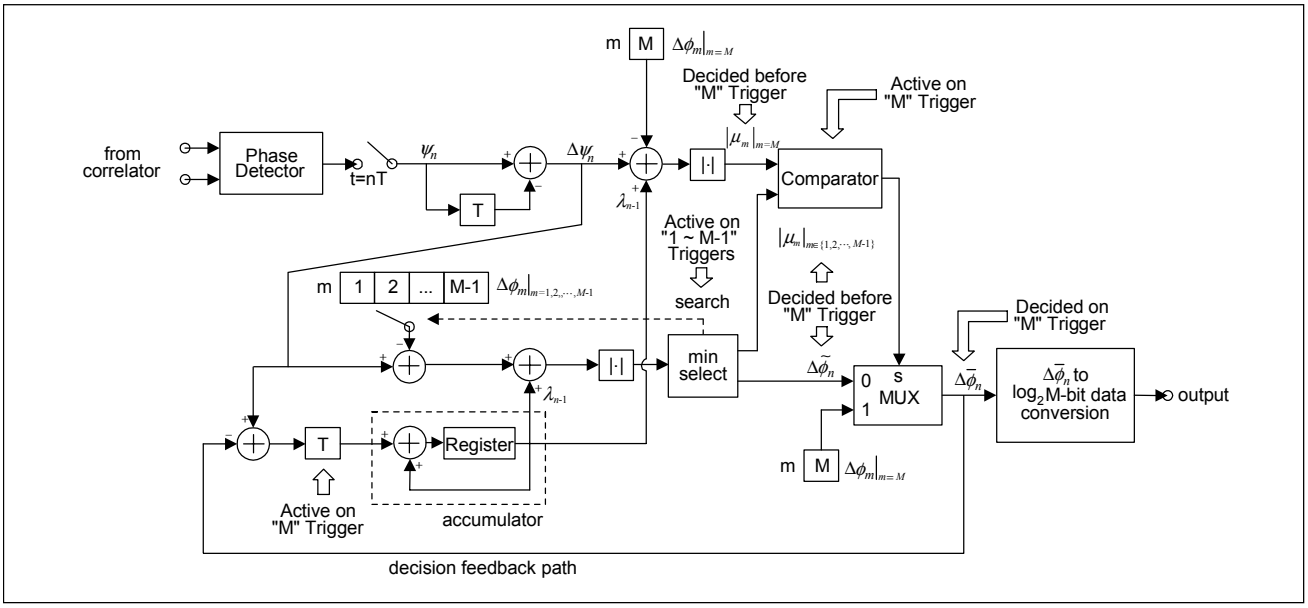

Fig. 9. Proposed design method for novel DF-DPD with higher data rate.

$\Delta\psi_n$ is decided.

In Fig. 9, which shows the proposed design method for the novel DF-DPD with a higher data rate, the decision of $\Delta\psi_n - \Delta\bar{\phi}_n$ is completed in M-times clock triggers. The operation of the proposed method is the same as the conventional operation in 1 to M–1 clock triggers. However, the accumulative differential phase noise, $\mu_m|_{m=M}$, for M-th reference phase, $\Delta\phi_M$, in the proposed architecture is decided before the M-th step begins. Then, the currently determined differential phase, $\Delta\bar{\phi}_N$, is only transferred to the accumulator through the 2×1 MUX with selection input connected to the comparator which compares $\mu_m|_{m=M}$ with the minimum value of the accumulative differential phase noises, $\mu_m|_{m\in\{1,2,\cdots,M-1\}}$, for 1 to M–1 reference phases. Thus, the currently accumulative differential phase noise λ_n can be obtained in M steps, and the process to estimate the current differential phase, $\Delta\bar{\phi}_n$, needs only M-times clock triggers.

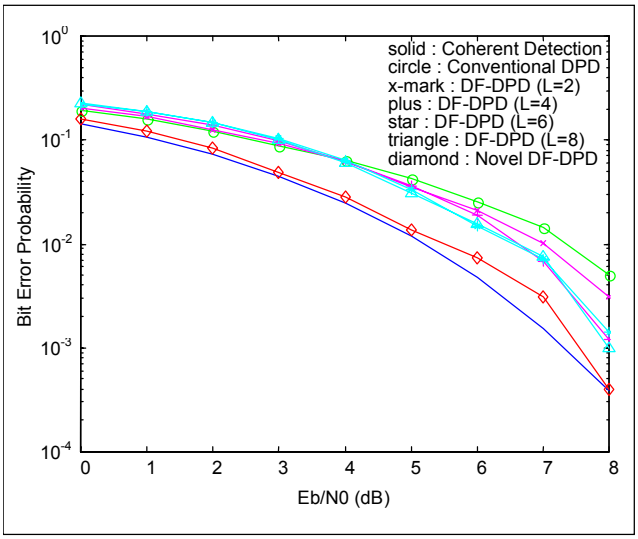

Fig. 10. Simulation results for performance compared with DF-DPD.

V. SIMULATION & COMPARISON RESULTS

This section presents the results of the DQPSK modem simulation on the performance of the algorithm and the architectural hardware complexity.

Figure 10 shows the simulation results of the performance. The simulation is performed in the additive white Gaussian noise (AWGN) channel. The figure reveals that the BER performance is very close to the theoretical BER performance of the coherent DPD $\left(P_B = 2Q\left(\sqrt{2E_b/N_0}\right)\left(1 - Q\left(\sqrt{2E_b/N_0}\right)\right)\right)$, and it is better than that of the conventional DPD and the DF-DPD (L = 2, 4, 6, 8). Specifically, the novel DF-DPD shows a better performance by about 2 dB more than the conventional DPD at $P_B = 10^{-2}$ and by about 1.2 dB more than DF-DPD with L = 8.

The simulation for hardware complexity uses a process in which the differential phase decoder designed with HDL is synthesized to a specific field programmable gate array (FPGA). Since the simulation is done for DPD, this paper does not include the results on the differential phase encoder.

Table 5 shows the simulation results on hardware complexity. Since the differential phase decoder is designed to process the 2-bit symbol during the 4-period main-clock, the data rate is half the frequency of the main-clock. Although the hardware

complexity of the novel DPD is similar to that of the conventional DF-DPD with $L = 2$ from Table 5, it is still lower than the complexity of the conventional DF-DPD with $L = 4$, 6, and 8. Specifically, the novel DF-DPD has a hardware complexity reduced by 42 % compared to the conventional DF-DPD with $L = 8$.

Table 5. Simulation results for hardware complexity compared with DF-DPD.

	Logic Cells Utilized	Flip-Flops Required	Available Maximum Clock Freq.	Available Maximum Data Rate
Conventional DPD	21 % (364/1728)	112	45.45 MHz	22.72 Mbps
DF-DPD (L = 2)	30 % (525/1728)	154	31.25 MHz	15.62 Mbps
DF-DPD (L = 4)	43 % (760/1728)	187	26.31 MHz	13.15 Mbps
DF-DPD (L = 6)	57 % (999/1728)	220	22.72 MHz	11.36 Mbps
DF-DPD (L = 8)	71 % (1238/1728)	252	20.00 MHz	10.00 Mbps
Novel DF-DPD	29 % (518/1728)	145	35.71 MHz	17.85 Mbps

The algorithm of the novel DF-DPD is similar to that of DPD using the recursively generated phase references (DPD-RGPR) proposed by Wei, since both algorithms use the phase reference generated by a simple recursive form [6]. The decision rule of DPD-RGPR is defined as follows:

$$\Delta\bar{\phi}_n = \min_{over \Delta\phi_m} |\psi_n - \Delta\phi_m + \varphi_{n-1}|,$$
$$\text{where } \varphi_{n-1} = \frac{W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1}) + \psi_{n-1} + 2K_{n-1}\pi}{W+1}. \quad (10)$$

Eqs. (6) and (10) show that the detection process of the DPD-RGPR is based on obtaining the distances of the addition between the received phase, ψ_n , and the recursively generated phase reference, φ_{n-1}, from the reference phases, $\Delta\phi_m|_{m=1,2,\cdots,M}$, while that of the novel DF-DPD takes the absolute value of the subtraction of the reference phases from the addition between the differently received phase, $\Delta\psi_n$, and the recursively generated phase reference, λ_{n-1}. In addition, the update process of the recursively generated phase reference, φ_{n-1} , for the DPD-RGPR consists of the adders, multipliers, and dividers. On the other hand, the recursively generated phase reference, λ_{n-1} , for the novel DF-DPD is obtained with one accumulator for $\left[\Delta\psi_{n-i+1} - \Delta\bar{\phi}_{n-i+1}\right]_{i=2,3,\cdots,n}$.

For the DPD-RGPR to obtain a performance similar to the coherent detection scheme, the parameter, W, concerned with the detection length, L, of the conventional DF-DPD, should be infinite and the detection length also infinite. It is theoretically possible for the detection process to take infinite symbols for the current detection process, but it is realistically impossible that the architecture taking the infinite symbols could be implemented to VLSI circuits. In other words, the performance of DPD-RGPR is limited because of the finite parameter, W, concerned with detection-length. On the other hand, Fig. 10 shows that the performance of the novel DF-DPD, using symbols ranging from the first symbol to the current symbol, is similar to that of the coherent detection without the assumption that the detection process has an infinite detection-length and takes infinite symbols.

Figure 11 gives the simulation results for the performance of the novel DF-DPD and DPD-RGPR. The performance of the novel DF-DPD is better than that of the DPD-RGPR with a finite parameter W.

For a relatively large W, the performance of the DPD-RGPR may approach that of the novel DF-DPD or the coherent detection scheme. Eqs. (6) and (10) show that the update process for the phase reference, λ_{n-1}, of the novel DF-DPD is simpler than that for the phase reference, φ_{n-1}, of the DPD-RGPR. Then, the hardware complexity of the DPD-RGPR may be worse than that of the novel DF-DPD.

The hardware architectures of the novel DF-DPD and the DPD-RGPR must be considered. For DPD-RGPR, to simplify

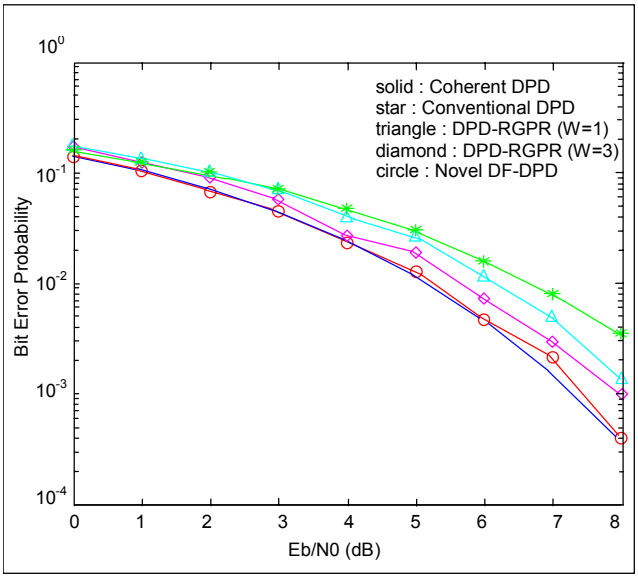

Fig. 11. Simulation results for performance compared with DPD-RGPR.

the operation on $W/(W+1)$ in the decision rule of DPD-RGPR, let's assume that the parameter W of DPD-RGPR is '$2^n - 1$'; then, the division of $W+1$ becomes only an n-bit right shift operation and the multiplication of W is composed of an n-bit left shift operation for the multiplication of 2^n and an adding operation for the subtraction of the multiplicand from the multiplication of 2^n. To reduce the resolution on π and simplify the hardware complexity, π is approximated as '3.' With these assumptions, the decision process of DPD-RGPR consists of five adders for the operations of $\varphi_{n-2} + \Delta\bar{\phi}_{n-1}$, $W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})$, $[W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})] + [\psi_{n-1}]$, $2K_{n-1}\pi$, and $\{[W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})] + \psi_{n-1}\} + \{2K_{n-1}\pi\} + \{2K_{n-1}\pi\}$. In addition, one register is required to store the phase reference, φ_{n-1}, for the next decision process. However, the novel DF-DPD needs an accumulator which is composed of one adder to add the detected phase noise, $\Delta\psi_{n-1} - \Delta\bar{\phi}_{n-1}$, to the previous phase reference, λ_{n-2}, and one register to store the phase reference, λ_{n-1}, for the next decision. Consequently, the hardware complexity of the novel DF-DPD with an update process by one accumulator is simpler than that of the DPD-RGPR with an update process by five adders.

Table 6 compares the novel DF-DPD to the DPD-RGPR with a set of W to '$2^n - 1$' and an approximation of π to '3.' The comparison is based on a gate count which is performed with a specific library, KG80, on a Samsung 0.5 μm sea-of-gate (SOG) process. In KG80, the gate count of the full adder is '7' and that of D filp-flop is also '7.' The resolution of the digitalized phase can be set to '8' from (8). Table 6 shows that the hardware complexity of DPD-RGPR is proportional to 'n×28' and increases rapidly as W increases. When W= 1, the complexity of the novel DF-DPD is simpler by about 69% than that of DPD-RGPR.

Table 6. Comparison results for hardware complexity compared with DPD-RGPR.

	Components	Gate Count
DPD-RGPR	One 8-bit Adder for $\varphi_{n-2} + \Delta\bar{\phi}_{n-1}$ Four (n+8)-bit Adders for $W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})$, $2K_{n-1}\pi$, $[W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})] + [\psi_{n-1}]$, $\{[W(\varphi_{n-2} + \Delta\bar{\phi}_{n-1})] + \psi_{n-1}\}$ $+ \{2K_{n-1}\pi\}$ One 8-bit Register for φ_{n-1}	7×8 + 7 ×(n+8) ×4 +7×8 = 28n + 336
Novel DF-DPD	One 8-bit Adder $\lambda_{n-2} + (\Delta\psi_{n-1} - \Delta\bar{\phi}_{n-1})$ One 8-bit Register for λ_{n-1}	7×8 + 7×8 = 112

VI. CONCLUSION

This paper presented a novel DF-DPD that demonstrates a simpler structure and better BER performance than those of the conventional DF-DPD and DPD-RGPR by reducing the complex structure of the conventional schemes. The novel DF-DPD exhibits a simple structure which uses only one accumulative DPD detector while the conventional DF-DPD uses L DPD detectors. Since the differential phase noise detected at the accumulative DPD detector is affected only by the current phase error, the current differential phase noise becomes the lowest and thus the BER performance of the novel DF-DPD becomes very close to that of the coherent detection with differential encoding.

The proposed algorithm assumes that the received phase is only dependent on the channel noise and the initial phase noise is zero. However, the initial phase noise may not be zero because of receiver noise such as sampling error. The accumulator of the novel DF-DPD may also accumulate initial phase noise and the performance may be degraded. Therefore, a study is needed for developing the novel DF-DPD with an improved algorithm which considers the effects of the initial phase noise.

The performance of the novel DF-DPD may not be better than that of the conventional DPD for a fading channel such as Rayleigh, because the novel DF-DPD was developed from the conventional DF-DPD with the performance improved only slightly for very slow fading. Accordingly, more studies are also called for on simulating and improving the performance in various fading channels.

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