A Class-D Amplifier for a Digital Hearing Aid with 0.015% Total Harmonic Distortion Plus Noise

Dongjun Lee, Jinho Noh, Jisoo Lee, Yongjae Choi, and Changsik Yoo

A class-D audio amplifier for a digital hearing aid is described. The class-D amplifier operates with a pulse-code modulated (PCM) digital input and consists of an interpolation filter, a digital sigma-delta modulator (SDM), and an analog SDM, along with an H-bridge power switch. The noise of the power switch is suppressed by feeding it back to the input of the analog SDM. The interpolation filter removes the unwanted image tones of the PCM input, improving the linearity and power efficiency. The class-D amplifier is implemented in a 0.13-μm CMOS process. The maximum output power delivered to the receiver (speaker) is 1.19 mW. The measured total harmonic distortion plus noise is 0.015%, and the dynamic range is 86.0 dB. The class-D amplifier consumes 304 μW from a 1.2-V power supply.

Keywords: Class-D amplifier, interpolation filter, sigma-delta modulator, hearing aid, CMOS.

I. Introduction

Compared with an analog hearing aid, a digital hearing aid can provide better hearing loss compensation and easy fitting of the hearing loss characteristics to each patient [1], [2]. In a digital hearing aid, a digital signal processor (DSP) performs the required hearing loss compensation with input from an analog-to-digital converter. Conventionally, the output of the DSP is then applied to a digital-to-analog converter (DAC) whose output is then amplified by a linear audio amplifier, as shown in Fig. 1(a) [3]. The DAC and linear audio amplifier, however, can consume a significant amount of power; to address this problem, a class-D audio amplifier was recently employed to replace the DAC and audio amplifier [4]-[11].

In a conventional class-D amplifier, the analog input signal is compared with a triangular wave carrier signal to generate a pulse-width modulated (PWM) signal driving a power switch [4]-[7]. If this type of conventional class-D amplifier is to be used in a digital hearing aid, a DAC must be placed between the hearing aid DSP and the class-D amplifier, increasing the power consumption.

To allow the direct application of the hearing aid DSP output to a class-D amplifier, a class-D amplifier with 16-bit pulse-code modulated (PCM) digital input was developed [8]. From the design in [8], the performance has been improved by employing an interpolation filter in front of the digital sigma-delta modulator (SDM) that can effectively suppress the unwanted image tones.

Section II describes the architecture of the class-D audio amplifier, and the circuit implementation is given in section III. The experiment results are given in section IV, followed by the conclusion in section V.

Manuscript received Dec. 20, 2012; revised Feb. 25, 2013; accepted Mar. 5, 2013.

This work was supported by the Seoul R&BD Program (SS100022). The CAD tools were provided by the IC Design Education Center (IDEC), Korea.

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http://dx.doi.org/10.4218/etrij.13.0112.0852

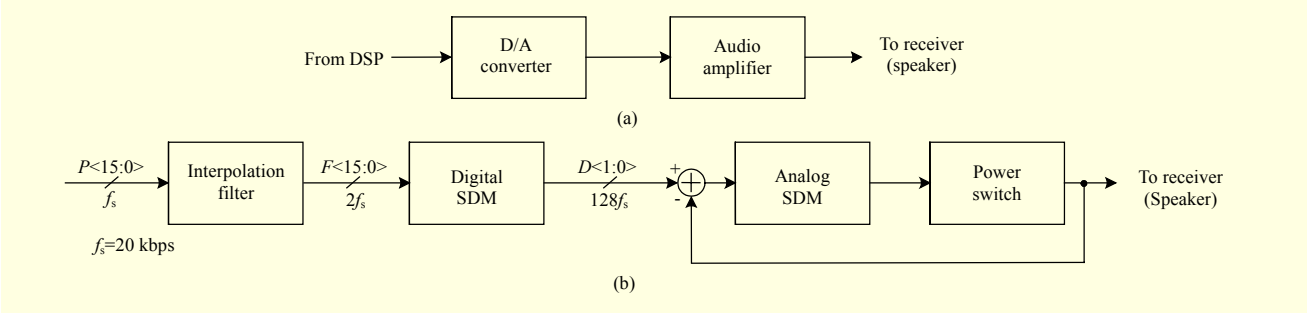

Fig. 1. (a) Conventional DAC and audio amplifier and (b) proposed class-D amplifier for digital hearing aid.

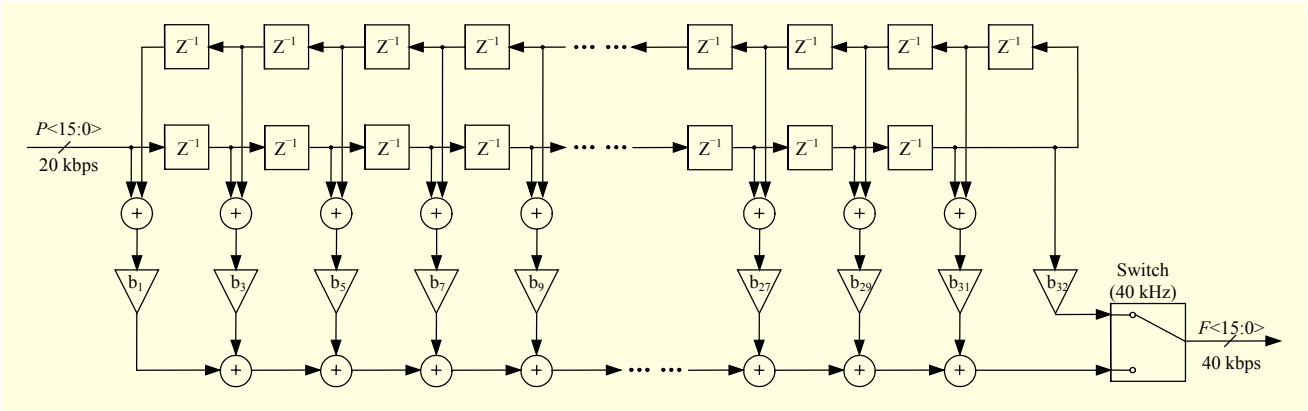

Fig. 2. Interpolation filter.

II. Architecture

The block diagram of the proposed class-D audio amplifier is shown in Fig. 1(b). The hearing aid DSP provides the 1-bit serialized pulse-code modulated (PCM) digital signal as the input of the class-D amplifier at the rate of 320 kbps. The serial input is converted to the 16-bit parallel signal *P*<15:0>, which is then applied to the interpolation filter. The interpolation filter increases the data rate from 20 kbps to 40 kbps and removes the unwanted image tones, which helps to improve the linearity and power efficiency. A digital SDM follows the interpolation filter to reduce the data width from 16 bits to 1.5 bits while increasing the data rate to 2.56 MHz. The output *D*<1:0> of the digital SDM is converted to a three-level analog signal by a simple DAC. The three-level analog signal is then modulated by an analog SDM to generate the driving signal of the final power switch. The power switch drives the receiver (speaker) of a hearing aid. Due to the inherent low-pass filtering characteristic of the receiver and human ear, there is no need to insert a low-pass filtering LC-filter between the power switch and receiver [6], [7].

The cutoff frequency of the class-D amplifier is set to be 7.5 kHz because a hearing aid does not need to provide an audio signal over 7.5 kHz, which is the inaudible frequency range for most patients with hearing loss [12], [13].

Table 1. Specification of interpolation filter.

Cutoff frequency	8 kHz
Width of transition band	4 kHz
Data rate of output	40 kHz
Stopband attenuation	> 90 dB

III. Circuit Implementation

1. Interpolation Filter

The interpolation filter increases the data rate from 20 kbps to 40 kbps and, more importantly, removes the unwanted frequency components from the input data (hearing aid DSP output) for better linearity and power efficiency. The cutoff frequency of the interpolation filter is 8 kHz to ensure it does not affect the overall frequency characteristic of the class-D amplifier. The width of the transition band of the interpolation filter is 4 kHz. For minimum power consumption, the interpolation filter has been realized with only one filtering stage. The target specification of the interpolation filter is summarized in Table 1.

The interpolation filter is realized with a half-band filter (HBF) with the finite impulse response (FIR) structure, as

Table 2. Coefficient of interpolation filter.

Coefficient	Value	CSD	Number of adders	
			Before CSD	After CSD
b_1	–0.000019781406081165187	$-2^{-16}-2^{-18}$	17	2
b_3	0.00007225668741739355	$2^{-14}+2^{-17}$	2	2
b_5	–0.00019523598166415468	$-2^{-12}+2^{-14}$	13	2
b_7	0.00044216740934643894	$2^{-11}-2^{-14}-2^{-16}$	4	3
b_9	–0.00089026472051045857	$-2^{-10}+2^{-13}+2^{-15}-2^{-17}$	13	4
b_{11}	0.00164416972984327	$2^{-10}+2^{-11}+2^{-14}+2^{-16}-2^{-18}$	5	5
b_{13}	–0.0028403192663972732	$-2^{-8}+2^{-10}+2^{-12}+2^{-15}$	11	4
b_{15}	0.0046535299497918459	$2^{-8}+2^{-11}-2^{-14}+2^{-16}+2^{-18}$	6	5
b_{17}	–0.0073105661922454601	$-2^{-7}+2^{-10}$	8	2
b_{19}	0.01112133737115073	$2^{-7}+2^{-9}+2^{-11}+2^{-13}+2^{-15}-2^{-17}$	6	6
b_{21}	–0.016553439221752342	$-2^{-6}+2^{-13}+2^{-15}-2^{-18}$	10	4
b_{23}	0.0244196015282796	$2^{-5}-2^{-7}-2^{-11}-2^{-13}+2^{-18}$	7	5
b_{25}	–0.03640349475426774	$-2^{-5}-2^{-8}+2^{-10}+2^{-13}+2^{-16}+2^{-18}$	11	6
b_{27}	0.056866083965360303	$2^{-4}-2^{-7}-2^{-9}+2^{-11}-2^{-14}+2^{-17}$	8	6
b_{29}	–0.1018922883176856	$-2^{-3}+2^{-5}-2^{-9}+2^{-11}-2^{-14}+2^{-17}$	11	6
b_{31}	0.31688331144505355	$2^{-2}+2^{-4}-2^{-6}-2^{-11}-2^{-13}+2^{-1}5-2^{-17}$	10	7
b_{32}	0.5	$2^{-1}-2^{-5}-2^{-10}-2^{-12}-2^{-15}$	11	5

shown in Fig. 2. The FIR filter is preferred to the infinite impulse response (IIR) filter for its better stability. Because the coefficients of the HBF are symmetric with respect to the center tap, the number of taps is only half that of a general FIR filter [3], which helps to decrease the power consumption and silicon area.

The coefficients of the HBF must be converted to 18-bit binary codes from a real number, which may result in performance degradation. The coefficients of the HBF are determined such that the stopband attenuation is larger than 95 dB even after the coefficients are converted to binary code. The multipliers required to realize the coefficients are implemented with shift registers and adders for a small silicon area. While the internal data is represented in the two's complement form, the coefficients are encoded with the canonic signed digit (CSD) code, which minimizes the number of non-zero coefficients [14]. The adders are realized with the ripple-carry-adder architecture. In Table 2, the coefficients of the filter and the number of adders to realize each coefficient are summarized. As shown in the table, the CSD coding can reduce the number of adders by about 50%. The simulated frequency response of the interpolation filter is shown in Fig. 3, and its signal-to-(noise plus distortion) ratio (SNDR) is over 96 dB.

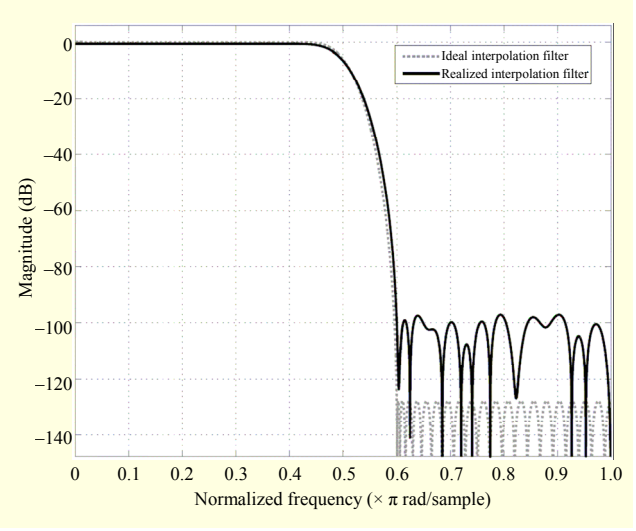

Fig. 3. Frequency response of interpolation filter.

2. Digital SDM

The digital SDM shown in Fig. 4 converts the output of the interpolation filter F<15:0> to the 1.5-bit digital signal D<1:0> while shaping its noise spectrum. The digital SDM has a third-order loop filter, and its oversampling ratio is 128, which

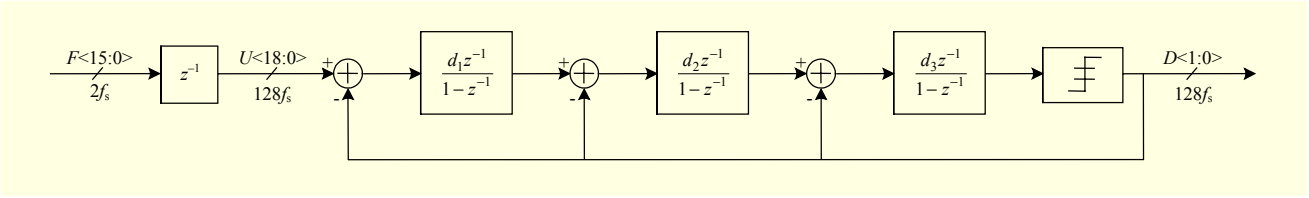

Fig. 4. Digital SDM.

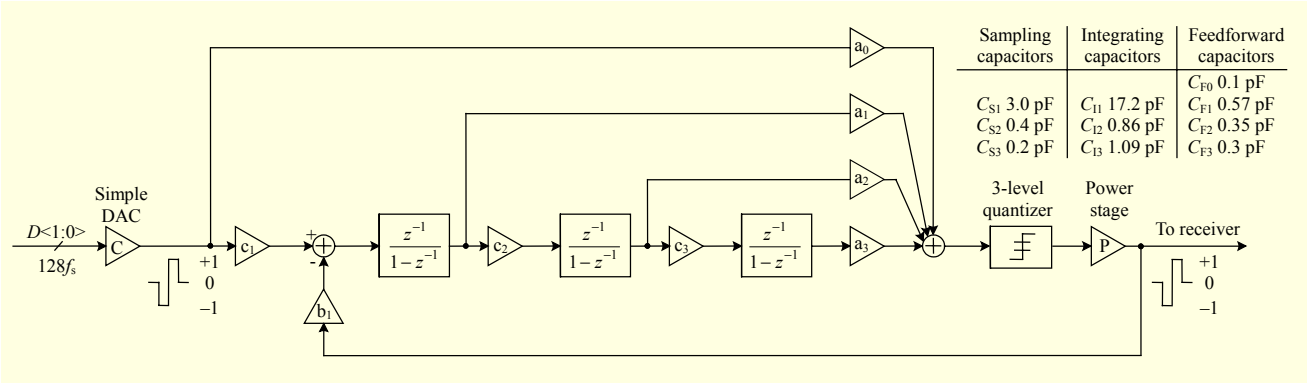

Fig. 5. Third-order analog SDM for class-D amplifier.

ensures that the SNDR of the digital SDM is sufficiently high; this high value does not limit the overall performance of the class-D amplifier. The loop filter has cascaded integrators with distributed feedback architecture to reduce the complexity of the digital SDM. The coefficients d_1, d_2, and d_3 of the digital SDM loop filter are 2^{-2}, 2^{-2}, and 2^0, respectively, which can be realized by a simple shifting operation. To prevent overflow, the internal signals of the digital SDM have a 19-bit width. The final output of the loop filter is truncated to the three-level digital output D<1:0>. The simulated SNDR of the digital SDM is 94.8 dB.

3. Analog SDM

The output of the digital SDM is converted to a three-level analog signal by a simple DAC whose output is then applied to an analog SDM with a third-order loop filter, as shown in Fig. 5 [8]. To reduce the voltage swing of the integrator outputs, the loop filter has the cascade of integrators with feedforward architecture. Table 3 shows the coefficients of the analog SDM loop filter.

The interpolation filter preceding the digital SDM eases the design of the analog SDM by decreasing the voltage swing of each integrator output of the analog SDM, as shown in Fig. 6. The analog SDM loop filter is realized with switched-capacitor integrators for a well-defined frequency response. However, the feedback path b_1 from the power switch is realized by continuous-time integrator to continuously feed back the noise of the power switch [8].

Table 3. Coefficients of analog SDM.

Feedback coefficient	Integrating coefficients	Feedforward coefficients
$b_1 = 0.1740$	$c_1 = 0.1740$	$a_0 = 1.0000$
	$c_2 = 0.4607$	$a_1 = 4.5935$
	$c_3 = 0.1831$	$a_2 = 3.5926$
		$a_3 = 2.9940$

4. Power Switch

From the output of the analog SDM, the non-overlapping signals are generated to drive the power switches without through current, which may lower the power efficiency. The buffer to drive the power switch is implemented with cross-coupled inverter string. So, the differential H-bridge outputs (H_P/H_N) are well matched [15]. As shown in Fig. 7, the power switch has an H-bridge architecture with three levels ("+1," "0," and "–1"), where the "0" level is realized by short-circuiting the differential output and sharing charge with a common-mode holding capacitor [8]. This type of power switch helps to minimize the power consumption and electromagnetic interference emission by preventing the common-mode variation [9].

IV. Experiment Results

The class-D amplifier for a digital hearing aid is

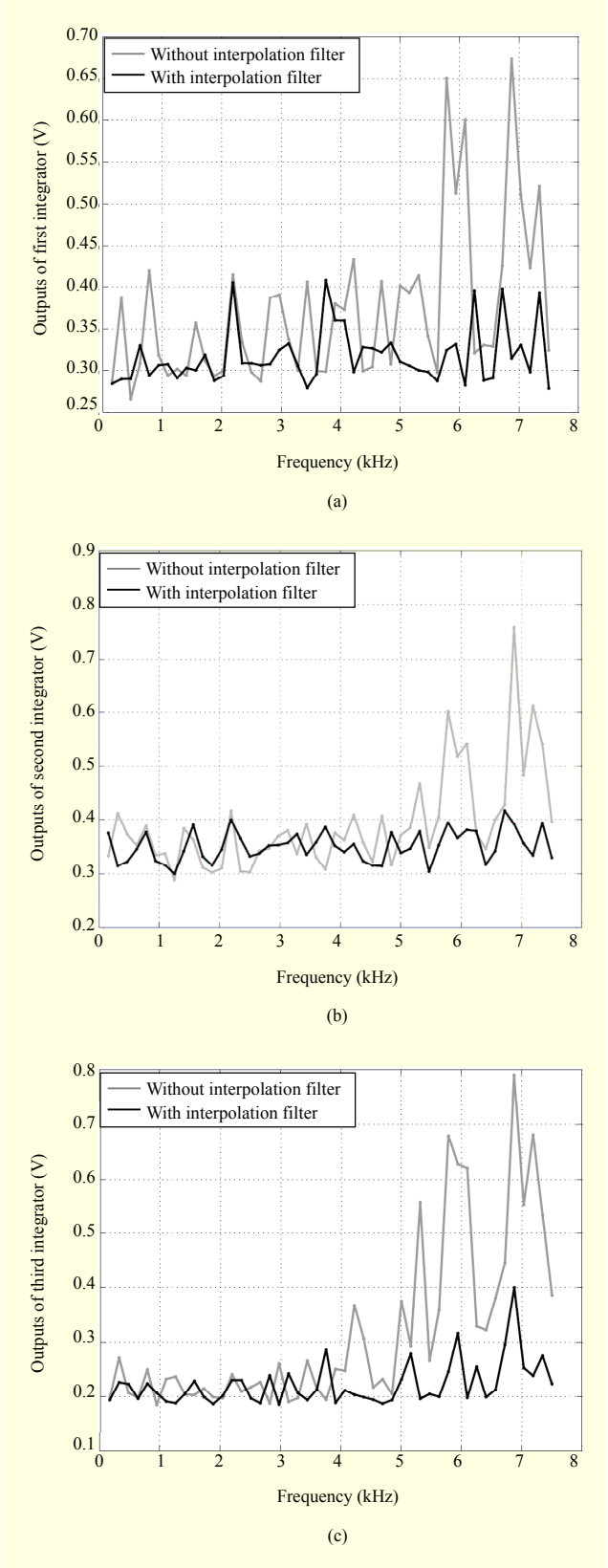

Fig. 6. Voltage swing of outputs of (a) first integrator, (b) second integrator, and (c) third integrator with and without interpolation filter.

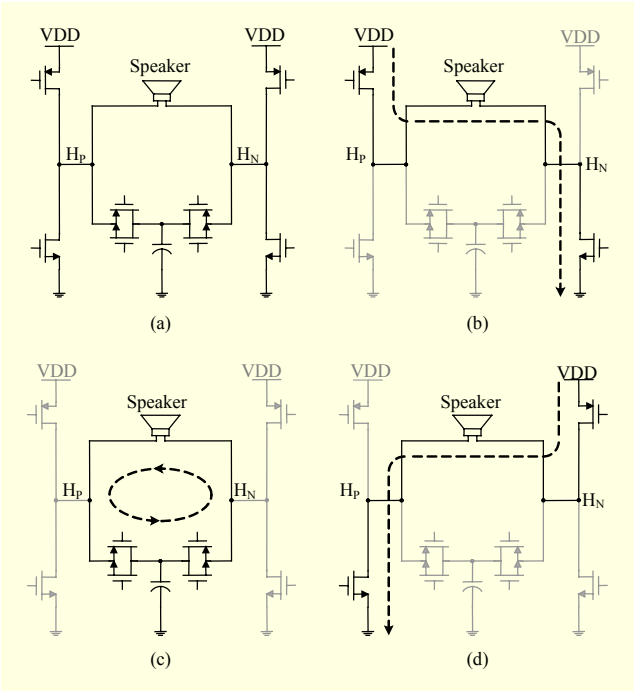

Fig. 7. (a) Architecture of H-bridge power switch and states of transistors for (b) "+1," (c) "0," and (d) "–1."

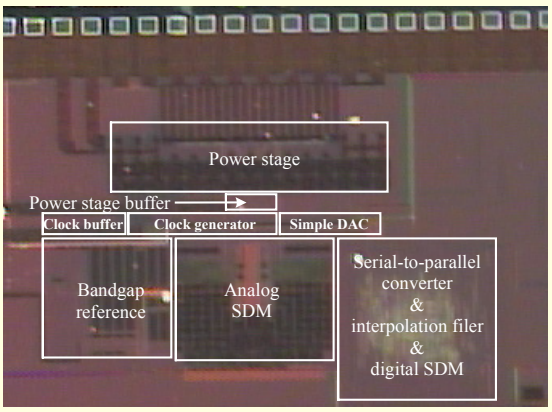

Fig. 8. Chip microphotograph of class-D amplifier.

implemented in a 0.13-μm CMOS process with a metal-insulator-metal capacitor, a microphotograph of which is shown in Fig. 8. The active area of the class-D amplifier is 1.06 mm × 16 mm. Figures 9(a) and 9(b) show the measured spectrum of the class-D amplifier output with –6-dBFS, 5-kHz input with and without the interpolation filter, respectively. From the figures, it is clear that the interpolation filter removes the unwanted imaginary tone at 15 kHz. The elimination of the imaginary tone helps to decrease the unnecessary power consumption when driving the receiver. The ratio of the power consumption with the interpolation filter to that without the interpolation filter is plotted in Fig. 10 for a –6-dBFS input and a −9-dBFS input. For a lower input frequency, the reduction of

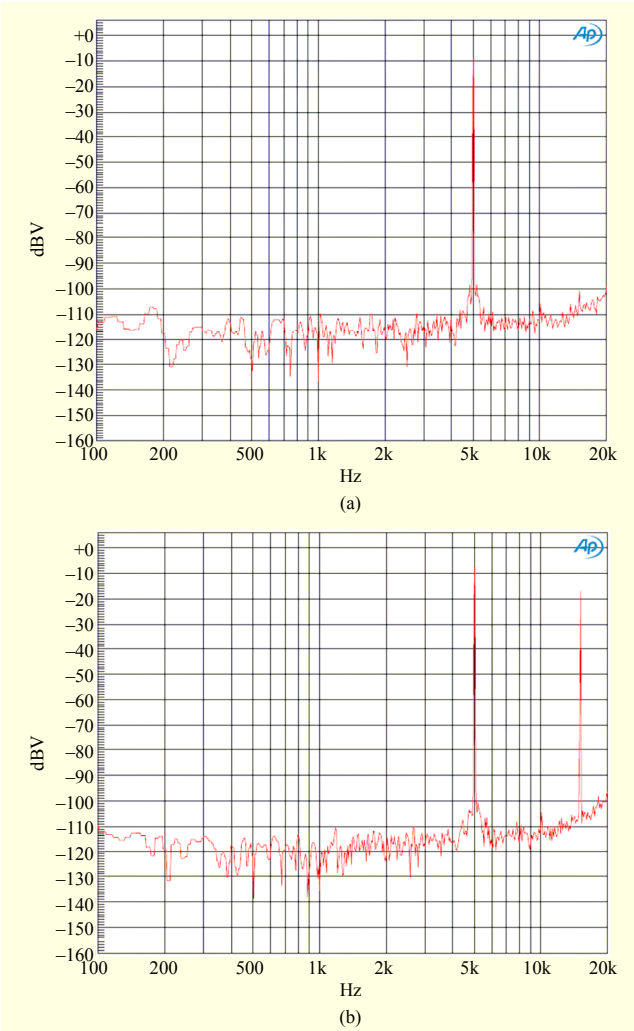

Fig. 9. Output spectrum of class-D amplifier (a) with and (b) without interpolation filter.

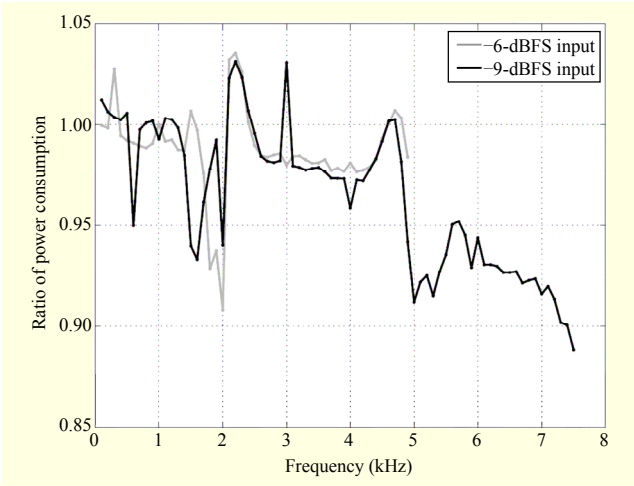

Fig. 10. Ratio of power consumption of the class-D amplifier with interpolation filter to that without interpolation filter.

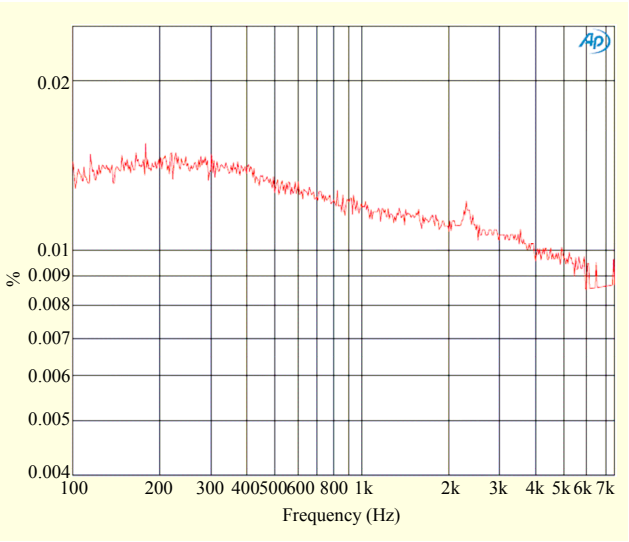

Fig. 11. THD+N vs. input frequency.

the power consumption with the interpolation filter becomes less because the imaginary tone gets smaller. It is impossible to measure the class-D amplifier without an interpolation filter over 5 kHz because the analog SDM becomes unstable.

Figure 11 shows the measured total harmonic distortion plus noise (THD+N) versus the input frequency. The peak signal-to-noise ratio and SNDR measure 94.3 dB and 88.0 dB, respectively. The measured dynamic range (DR) is 86 dB, and the maximum power delivered to the receiver is 1.19 mW. The performance of the presented DAC is summarized and compared with other works in Table 4.

V. Conclusion

A class-D amplifier was developed for a digital hearing aid. The class-D amplifier consists of an interpolation filter, digital SDM, and analog SDM, along with a power switch. The prototype implemented in a 0.13-μm CMOS process showed an 86-dB DR with a 0.015% THD+N. It was shown that the interpolation can effectively remove the unwanted image tones, improving the linearity and decreasing the power consumption.

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Table 4. Performance comparison.

	[10]	[3]	[11]	This work
Technology	0.18-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Area (mm^2)	1.6	0.8	2.46	1.06
Architecture	-	Three-stage HBF Digital SDM Switched-R DAC	Two-stage IIR filter Four-stage comb filter Digital SDM	One-stage HBF Digital SDM Analog SDM
DR (dB)	-	88	90	86
THD+N (%)	0.022	0.035	-	0.015
Supply voltage (V)	3.0	0.8	1.8	1.2
Power consumption of modulator (mW)	7.7	2.6	4.3	0.304
Output power (mW)	33.5	-	-	1.19
Load impedance (Ω)	32	16	376	46.5 @ DC 62.0 @ 0.5 kHz 160.0 @ 1 kHz

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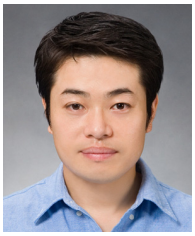

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