

NEW METHOD FOR DETERMINATION OF DRAIN SATURATION VOLTAGE IN SHORT CHANNEL MOS DEVICES BETWEEN LIQUID HELIUM TO ROOM TEMPERATURE

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A new method for drain saturation voltage extraction in submicron MOSFETs is presented. It is based on measurements of the partial derivative of the impact ionization rate. The method has been tested using main of channel length MOSFET devices and compared with others methods.

Keywords: MOS transistor; Drain saturation voltage; Substrate current

1. INTRODUCTION

Drain saturation voltage $V_{d_{sat}}$ is an important parameter in MOSFET modelling and process control. The existing method for $V_{d_{sat}}$ versus the gate voltage V_g extraction can be divided into two categories. The first [1, 2], is based on $I_d - V_d$ plotted curves where I_d is the drain current and V_d is the drain voltage and the second [3, 4], is based on the unique dependence $(V_d - V_{d_{sat}})$ of the ratio (I_{sub}/I_d) where I_{sub} represent the substrate current.

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In this letter a new technique for an accurate determination of drain saturation voltage can be classed with the second methods, and give directly the continuous $V_{d_{sat}}(V_g)$ characteristics.

2. THEORY

Generally, according to the lucky electron model [5], since the impact ionization rate is proportional to $\exp[-B/(Vd - V_{d_{sat}})]$, where B is a constant and $(Vd - V_{d_{sat}})$ is proportional to the drain field. In the literature [6], we found one of the follows expressions of the ratio I_{sub}/Id .

$$I_{sub}/Id = A \exp[-B/(Vd - V_{d_{sat}})] \quad (1)$$

or

$$I_{sub}/Id = A'(Vd - V_{d_{sat}}) \exp[-B'/(Vd - V_{d_{sat}})] \quad (2)$$

where A' , A , B' and B are constants. B' and B have a voltage dimension and are function of the carrier mean free path, and of the length pinch-off region. We note that (1) and (2) are all dependants on the difference $(Vd - V_{d_{sat}})$.

We pose $X(Vg, Vd) = Vd - V_{d_{sat}}$ and $Y(Vg, Vd) = I_{sub}/Id$, the ratio of partial derivative Y on Vd and Vg can be calculated as:

$$\frac{\partial Y/\partial Vd}{\partial Y/\partial Vg} = - \frac{1}{dV_{d_{sat}}/dVg} \quad (3)$$

The characteristic $V_{d_{sat}}(Vg)$ is also obtained by the following integral:

$$V_{d_{sat}}(Vg) = - \int \frac{(\partial Y/\partial Vg)}{(\partial Y/\partial Vd)} dVg. \quad (4)$$

3. RESULTS AND DISCUSSION

The previous analysis is applied at room temperature on the N Channel CNET MOSFET devices, with channel width W is 50 μm and channel lengths are ($L = 0.9, 1.5$ and 10 μm) the Light Doped Drain

Region (LDD) doping is $5 \cdot 10^{13}/\text{cm}^3$, the channel doping N_a ranging between 10^{15} and $10^{16}/\text{cm}^3$, the oxide thickness t_{ox} is 15 nm. The method is also compared to the Chan *et al.*, method [3].

The Figure 1 shows $V_{d_{sat}}(V_g)$ characteristics for three different channel lengths (0.9, 1.5 and 10 μm). The experimental points on these curves are obtained with Chan *et al.*, method [3], the lines curves are obtained with our method. We can see on this figure that the Chan *et al.*, method and our model are in good agreement. Generally, the saturation drain voltage $V_{d_{sat}}$ decrease with decreasing channel length and increase with increasing V_g . Indeed, the increase of V_g provokes the increase of inversion layer charge requiring an important drain voltage to ensure saturation.

The Figure 2 shows $V_{d_{sat}}(V_g)$ characteristics for five different temperatures. $V_{d_{sat}}$ increase with temperature at weak gate voltage and becomes not more sensitive at high gate voltage. We note that the

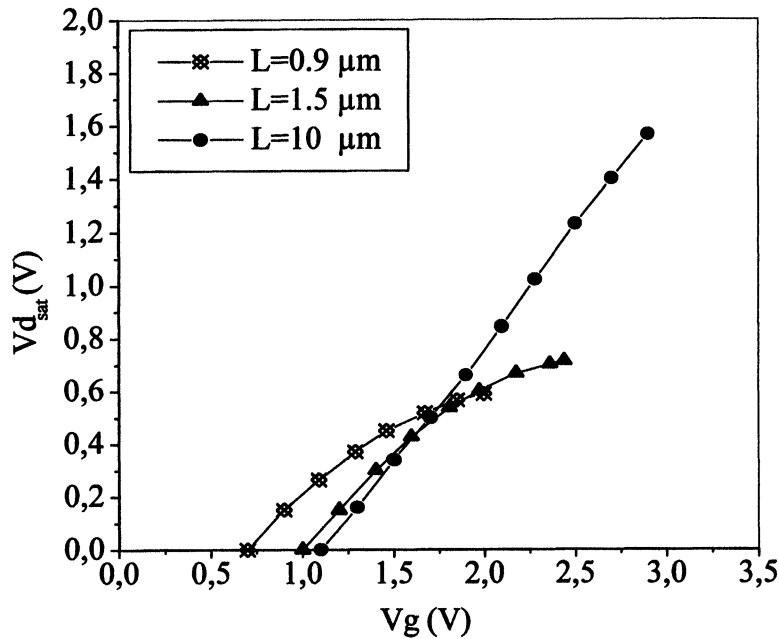


FIGURE 1 $V_{d_{sat}}$ versus V_g characteristics for three different Channel lengths. ($L=0.9$, 1.5 and 10 μm).

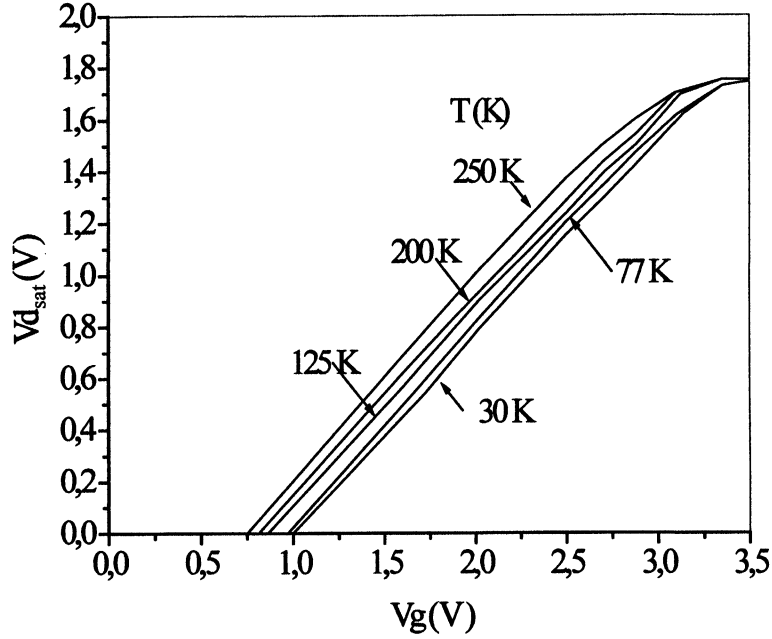


FIGURE 2 $V_{d_{sat}}$ versus V_g characteristics for five temperatures. (NMOS, $W/L = 50/10$, $t_{ox} = 15$ nm).

expression (1) and (2) are also valid at low temperature MOS operation [6].

In order to found the method validity domain we have used $V_{d_{sat}}(V_g)$ characteristics to determine A and B parameters for $1.5 \mu\text{m}$ channel length, and insure that there are constants for different potential gate. Using the expression (1), we can determine A and B parameters value by:

$$B = X^2 \partial(\text{Log } Y) / \partial V_d \quad (5)$$

and

$$A = Y \exp(B/X) \quad (6)$$

The plotted curves A and B versus V_g , Figures 3 and 4 shows that these parameters are nearly constants in $I_{sub}(V_g)$ apparition *i.e.*, in strong inversion, their values are $A = 8.5$ and $B = 23$ V. In the other hand, these parameters are identical to the fitting parameters in the I_{sub}/I_d versus $1/(V_d - V_{d_{sat}})$ plots.

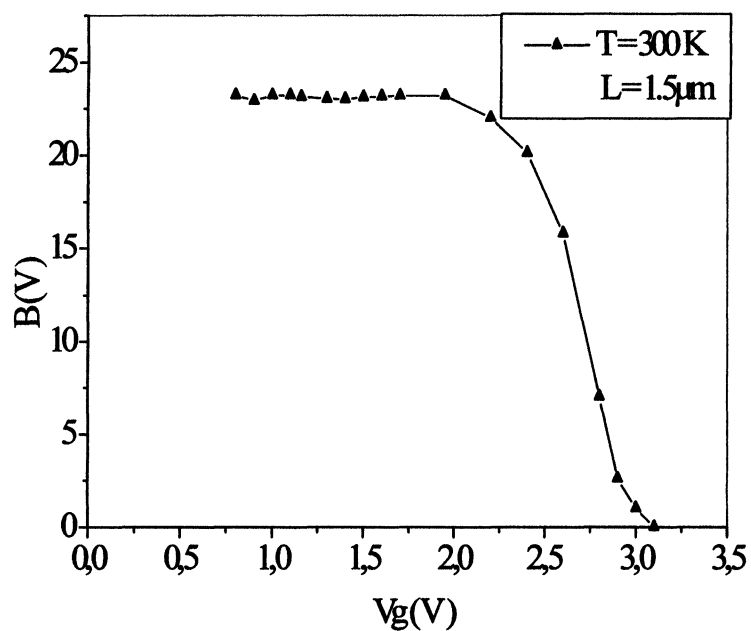


FIGURE 3 B parameter versus V_g characteristic for $1.5\mu\text{m}$ channel length at $T=300\text{ K}$.

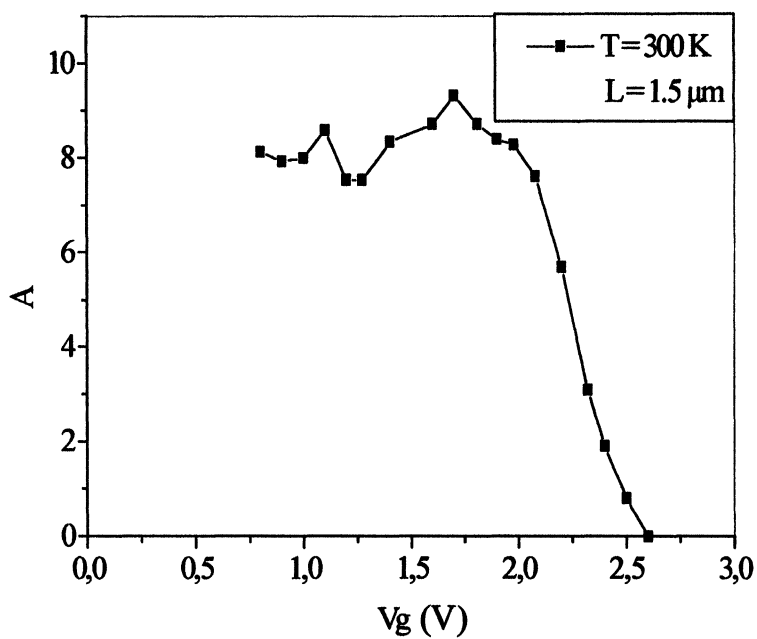


FIGURE 4 A parameter versus V_g characteristic for $1.5\mu\text{m}$ channel length at $T=300\text{ K}$.

4. CONCLUSION

We conclude that this method is the alone method to find experimental continuous $V_{d_{\text{sat}}}(V_g)$ curves, and confirm in the same time the I_{sub}/I_d versus $(V_d - V_{d_{\text{sat}}})$ relation. Its validity temperature range is found between liquid helium and room temperature. Its better applied in short channel MOSFET or in strong drain voltage for long channel MOSFET.

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