A New Method for Extracting Interface Trap Density in Short-Channel MOSFETs from Substrate-Bias-Dependent Subthreshold Slopes

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Interface trap densities at gate oxide/silicon substrate (SiO_2/Si) interfaces of metal oxide semiconductor field-effect transistors (MOSFETs) were determined from the substrate bias dependence of the subthreshold slope measurement. This method enables the characterization of interface traps residing in the energy level between the midgap and that corresponding to the strong inversion of small size MOSFET. In consequence of the high accuracy of this method, the energy dependence of the interface trap density can be accurately determined. The application of this technique to a MOSFET showed good agreement with the result obtained through the high-frequency/quasi-static capacitance-voltage (C-V) technique for a MOS capacitor. Furthermore, the effective substrate dopant concentration obtained through this technique also showed good agreement with the result obtained through the body effect measurement.

I. Introduction

The subthreshold region is particularly important for low-voltage, low-power applications, where metal oxide semiconductor field-effect transistors (MOSFETs) are used as switches in digital logic and memory applications, because the subthreshold region describes the degree of ideality (influences switching speed and power dissipation) between on and off states [1,2]. Therefore, the factors determining the subthreshold slope, such as gate oxide thickness, channel dopant concentration, and interface trap density, should be optimized sufficiently to satisfy the required on-

off current ratio.

One of the most important parameters for the estimation of MOS device reliability is the interface trap density, D_{it}. Up to now, D_{it}s have usually been evaluated using MOS capacitors [3] whose areas are larger than, for example, 100 x 100 μm, due to the limitation of capacitor measurement. Therefore, it is difficult to extract D_{it}s using conductance, [4] high-frequency/quasi-static capacitance-voltage (C-V) method [5], or deep-level transient spectroscopy (DLTS) [6,7] for small devices since all of the above methods are based on the capacitor measurement. The charge-pumping technique has long been used successfully to extract D_{it}s in small size MOSFETs[8,9]. Although this technique gives the energy dependence of interface trap density, various equipments such as pulse generator, oscilloscope, and DC ammeter are required for the measurement and an expertism is needed for the analysis of the data from the experiment. In 1975, the subthreshold slope technique was developed for simple estimations of D_{it}s in MOSFETs [10], but it is not applicable to short-channel MOSFETs because various high drain voltages are required to extract D_{it}, thus leading to an increase of surface potential. Furthermore, only the average interface trap density can be obtained at the surface potential located at near 1.5 times the Fermi potential. The partial derivative of the logarithm of the subthreshold current, with respect to the gate voltage, yields an average D_{it} near the surface potential of 1.5 times the Fermi potential [11,12]. However, this technique requires an accurate evaluation of the channel dopant concentration for the calculation of the depletion layer capacitance prior to the extraction of the equivalent capacitance of the interface traps.

In this paper, a simple method to obtain D_{it} in the range of the surface potential between the midgap and that corresponding to the strong inversion, directly through subthreshold slope measurement of a small size MOSFET, is presented. The depletion layer capacitance can be eliminated by measuring the substrate bias dependence of the subthreshold slope. The interface trap density can be obtained from the subthreshold characteristics of the MOSFET only, so this method is easier to use as compared with the conventional C-V method. Experimental substrate dopant concentration can also be obtained as a by-product of this subthreshold slope measurement, and was compared with the result obtained through the body effect measurement. D_{it}s, after gate-bias stresses on a MOSFET for a time-dependent dielectric-breakdown (TDDB) test, were also extracted. Finally, the limitations of this method are discussed.

II. Theory

The subthreshold region corresponds to the weak inversion region where the surface of the silicon substrate is nearly depleted of electrons or holes. In the weak inversion region of an n-MOSFET, where the surface potential, ψ_s, is larger than the Fermi potential, ϕ_F, and smaller than $2\phi_F$ (more accurately, $\psi_s < 2\phi_F - kT/q$), ψ_s can be approximated as [1]

$$\psi_s = (V_G - V_{FB}) - \frac{\alpha^2}{2\beta} \left\{ \left[1 + \frac{4}{\alpha^2}(\beta V_G - \beta V_{FB} - 1) \right]^{1/2} - 1 \right\}, \quad (1)$$

where V_G is the gate voltage, V_{FB} is the flat-band voltage, β is defined as q/kT, and α is defined as

$$\alpha = \frac{\sqrt{2}\varepsilon_s t_{ox}}{\varepsilon_{ox} L_D}, \qquad (2)$$

where ε_s, ε_{ox}, t_{ox}, and L_D are the permittivity of silicon, the permittivity of SiO_2, the gate oxide thickness, and the extrinsic Debye length, respectively. Equation (1) is an adequate form for n-channel MOSFETs of uniformly doped substrates, with low interface trap densities or thin gate oxides. For p-channel MOSFETs, '-' sign ahead of $\alpha^2/2\beta^2$ term in eq. (1) must be converted into '+' sign. The subthreshold swing, S, is defined as $dV_G/d(\log(I_{DS}))$ where I_{DS} is the drain current, as shown in Fig. 1. For $\alpha >> C_D/C_{ox}$, S is approximated as [1]

$$S \approx \frac{kT}{q} \ln 10 \cdot \left[1 + \frac{(C_D + C_{it})}{C_{ox}}\right], \qquad (3)$$

where C_D and C_{it} are the differential capacitance of the semiconductor depletion layer in the weak inversion region and the equivalent capacitance for the interface traps, respectively. C_D is approximately expressed as

$$C_D \approx \left[\frac{q\varepsilon_s N_A}{2(\psi_s + |V_{BS}| - 1/\beta)}\right]^{1/2}, \qquad (4)$$

where N_A and V_{BS} are the effective substrate acceptor concentration and the substrate bias, respectively. C_{it} is given by

$$C_{it} = qD_{it}. \qquad (5)$$

As V_{BS} approaches infinity, C_D approaches zero so that S becomes close to S_∞ which has the value of

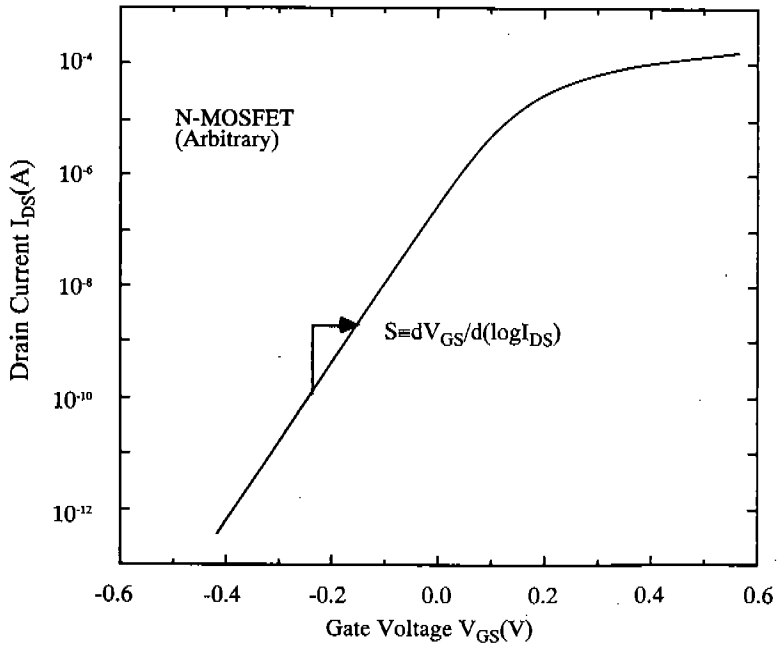

Fig. 1. Definition of the subthreshold swing of an arbitrary n-MOSFET in weak inversion region.

$$S_\infty \approx \frac{kT}{q} \ln 10 \cdot (1 + \frac{C_{it}}{C_{ox}}), \qquad (6)$$

and the slope L_s in the S versus $(\psi_s + |V_{BS}| - 1/\beta)^{-1/2}$ curve is expressed as

$$L_s = \frac{kT}{q} \ln 10 \cdot \frac{t_{ox}}{\varepsilon_{ox}} (\frac{q\varepsilon_s N_A}{2})^{1/2}. \qquad (7)$$

In other word, the S versus $(\psi_s + |V_{BS}| - 1/\beta)^{-1/2}$ plot is a straight line whose y intercept gives S_∞ and the slope is proportional to $N_A^{1/2}$. Therefore, the effective substrate acceptor concentration, N_A, can also be experimentally extracted from L_s using eq. (7). L_s may be reduced for a short-channel MOSFET due to charge sharing between the gate and the source/drain, which leads to threshold voltage reduction for short channel device. [13] To avoid this reduction, the application of this method must be restricted to MOSFETs showing negligible reduction of the threshold voltage as compared with long-channel MOSFETs.

Figure 2 shows the threshold voltages of n-MOSFETs as a function of the channel length. Threshold voltages were determined from the intercepting point on the gate voltage axis, which is obtained by taking the linear extrapolation of the drain current in the linear region of the measured I_{DS}-V_G curve. At the drain voltage of 0.1 V and substrate bias of 0 V, the MOSFETs with channel length larger than 0.8 μm have negligible

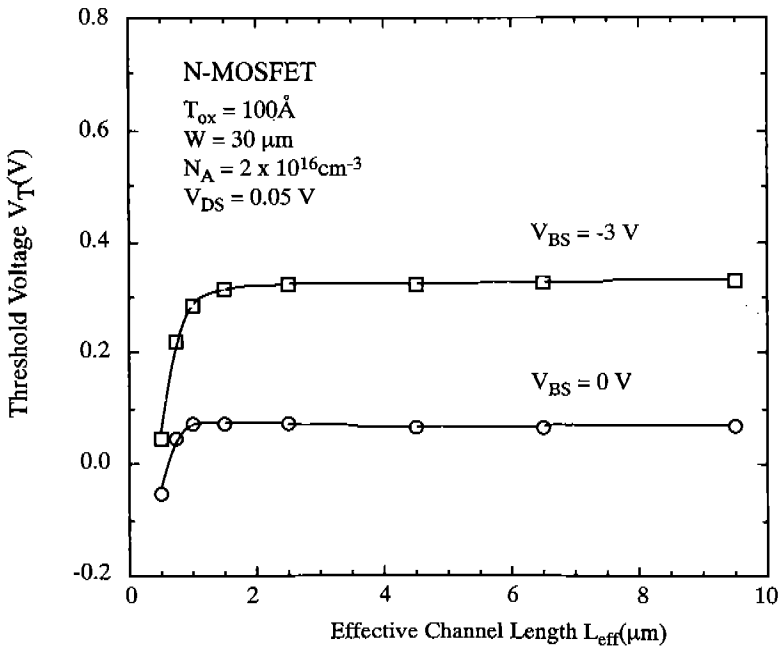

Fig. 2. Short-channel effect (threshold voltage shift) of n-MOSFETs. The effective channel dopant concentration is about 2×10^{16} cm^{-3}. When the drain voltage is low (< 0.1 V), threshold voltage shift is negligible for the channel lengths larger than 0.8 μm so that the MOSFETs have long-channel behaviors.

threshold voltage reductions as compared with the MOSFET with channel length of 30 μm. At the substrate bias of -3 V, the threshold reduction due to charge sharing increases as compared with the case of 0 V. This short channel effect is still negligible for MOSFETs with channel length over 1.0 μm. The subthreshold swing is measured at one drain current corresponding to a certain surface potential, given by eq. (1) at zero substrate bias. When substrate biases are applied to the substrate, same ψ_s can be maintained on the assumption that equal drain currents at various V_{BS}s are associated with identical surface potentials. This supposition is similar to the widely accepted assumption that a certain current level, for example, 1 μA, is required to create the threshold condition ($\psi_s = 2\phi_F$) [14].

III. Experimental Results

MOSFETs in this experiment were fabricated using a conventional polysilicon gate complementary-metal-oxide-semiconductor (CMOS) process. All MOSFETs are surface-channel type, where n- and p-MOSFETs have n^+ and p^+ polysilicon gates, respectively. First, N_As and V_{FB}s must be obtained to calculate surface potentials. For this purpose, N_As were crudely estimated through the SUPREM simulation. V_{FB}s were approximated as the work-function difference between the polysilicon gate and the channel. In this approximation, factors contributing to V_{FB}, such as fixed oxide charge density over gate oxide capacitance (Q_{ss}/C_{ox}) and areal mobile charge density in the gate oxide over gate oxide capacitance (Q_m/C_{ox}), were neglected as compared with the work function difference (this is valid for current VLSI process technology). Work functions of highly doped n^+ and p^+ polysilicon were assumed to be 0.5 V lower and higher than the intrinsic silicon, respectively [15]. For the calculation of surface potential, assumed N_A and V_{FB} were inserted into eq. (1).

On the other hand, N_A and V_{FB} may also be determined from the body effect measurement for each MOSFET. The threshold voltage, V_T, is related to the flat-band voltage as [1]

$$V_T = V_{FB} + 2\phi_F + \frac{\left[2\varepsilon_s q N_A (2\phi_F + |V_{BS}|)\right]^{1/2}}{C_{ox}}, \tag{8}$$

and the threshold voltage shift, ΔV_T, becomes

$$\Delta V_T = \gamma\left[(2\phi_F + |V_{BS}|)^{1/2} - (2\phi_F)^{1/2}\right], \tag{9}$$

where the body effect parameter, γ, is defined as

$$\gamma = \frac{2(\varepsilon_s q N_A)^{1/2}}{C_{ox}} . \tag{10}$$

If we measure threshold voltages of large MOSFETs as a function of the substrate bias, effective substrate dopant concentrations can be estimated using eqs. (9) and (10). Then, subtracting $2\phi_F$ from the value at the intersection of the extrapolated line with the V_T-axis at $(2\phi_F + |V_{BS}|) = 0$ results in V_{FB}. Due to the logarithmic dependence of ϕ_F on N_A, ϕ_F can be calculated with relative accuracy from the crude estimation of N_A. Measuring the V_{BS} dependence of V_T and inserting ϕ_F obtained from the first estimation into eq. (9), we can determine N_A more accurately than the estimated value obtained in the first stage. We can continue these iterations to obtain an exact solution, however, we found usually two or three itera-

tions are enough for the practical purpose.

Figure 3 shows the body effect of the n^+ polysilicon gate n-MOSFET with the gate oxide of 100 Å and the mask channel width/length (W/L) of 30 μm/ 30 μm. N_A was initially assumed to be 9×10^{16} cm^{-3} through the SUPREM simulation and V_{FB} to be -0.9 V, for the calculation of the surface potential. Although this n-MOSFET was ion-implanted prior to the thermal oxidation for the gate oxide, the body effect plot is almost linear with respect to $(2\phi_F + |V_{BS}|)^{1/2}$ up to the substrate bias of -3 V. This confirms that the effective dopant concentration is nearly uniform. The measured γ is about 0.497 $V^{1/2}$ so that the calculated N_A is about 8.8×10^{16} cm^{-3}, in good agreement with the SUPREM simulation. The value at the intersection of the extrapolated line with the y-axis is -0.033 V which leads to V_{FB} of about -0.85 V. This is nearly the same as the assumed value.

Figure 4 shows the subthreshold characteristics of an n-MOSFET with the substrate bias as a parameter. The drain was biased at 0.1 V to avoid drain-induced barrier lowering (DIBL) [16]. As the absolute substrate bias increases, the subthreshold slope becomes steeper due to the reduction of the depletion layer capacitance. The subthreshold slope is nearly independent of the gate voltage, representing a nearly constant distribution of the interface traps in the energy gap.

An example of the extraction of D_{it}s for various surface potentials in the n-MOSFET is shown in Fig. 5. This MOSFET has negligible short-channel effect, that is, negligible threshold voltage reduction as compared with the long-channel MOSFET (Fig. 2). To prevent DIBL, the drain was biased at 0.1 V. The subthreshold swing ver-

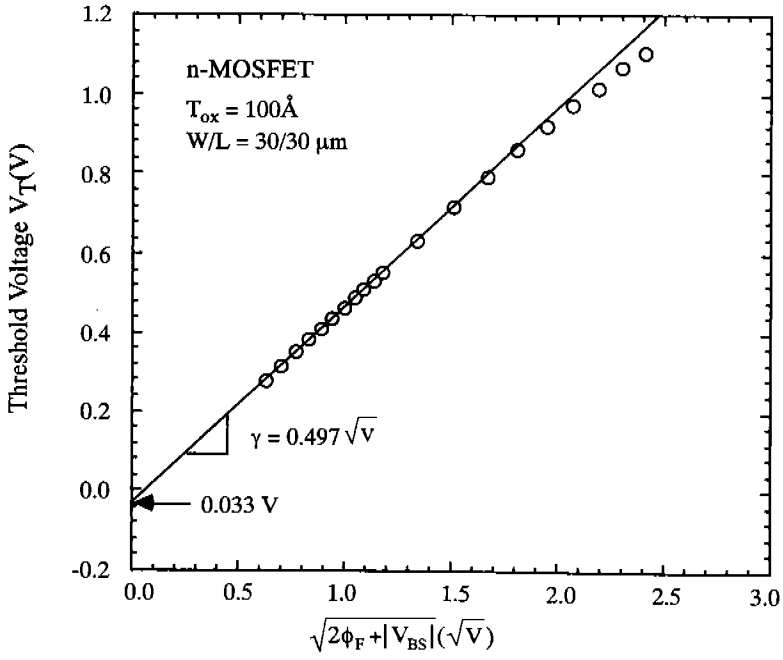

Fig. 3. Body effect of the surface-channel n-MOSFET with n^+ polysilicon gate.

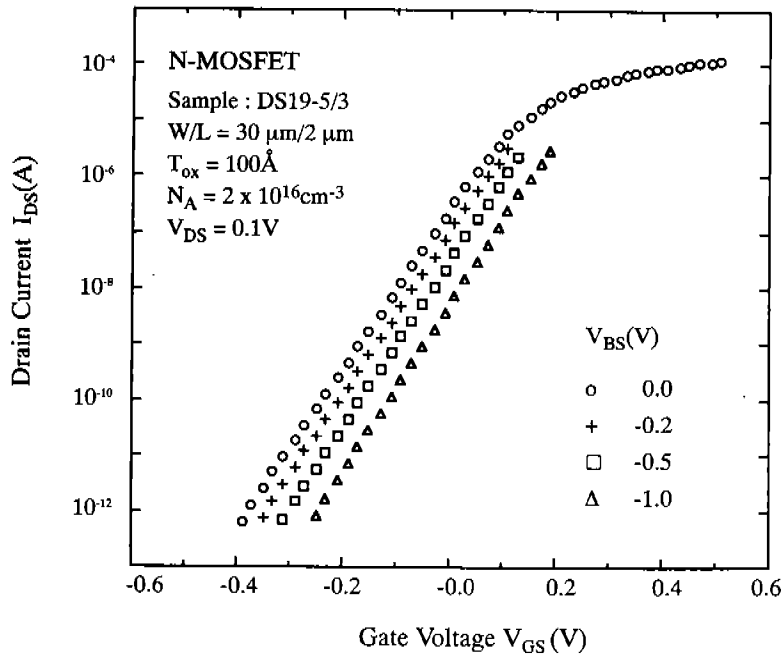

Fig. 4. The subthreshold characteristics of an n-MOSFET with the substrate bias as a parameter.

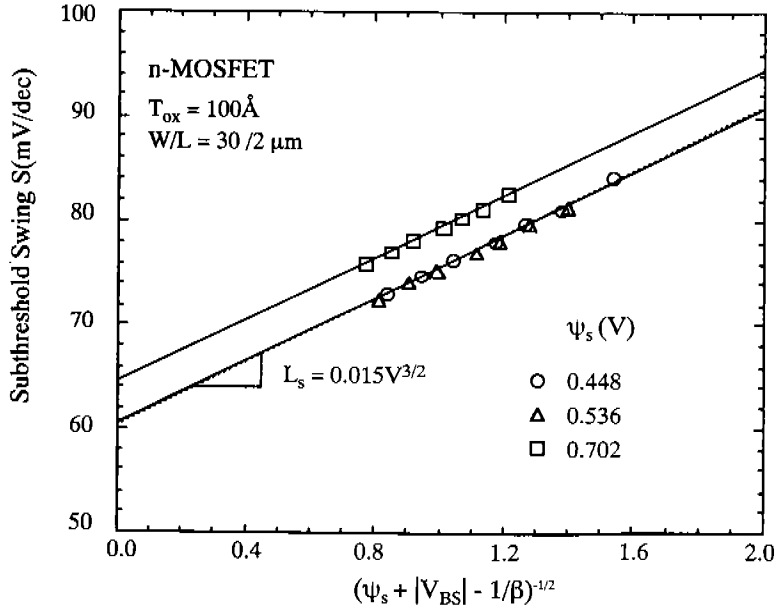

Fig. 5. The subthreshold swing dependence of the n-MOSFET on the substrate bias with the surface potential as a parameter.

sus $(\psi_s + |V_{BS}| - 1/\beta)^{1/2}$ is almost linear, showing the validity of our method. All three L_Ss are nearly equal to 0.015 $V^{3/2}$ and correspond to the effective acceptor concentration of 9.4 x 10^{16} cm^{-3}, which is in good agreement with the result obtained through the body effect measurement. S_o (≡ (kT/q) ln 10), under the condition where C_{it} is nearly zero or negligible compared with C_{ox}, is 58.5 mV/decade at room temperature (25°C). Since very small drain current flow through the channel of MOSFET in the subthreshold region, there may be negligible rising of the temperature in the channel region. The measured S_∞ is 60.36 mV/decade for the surface potential of 0.536 V, so that D_{it} calculated by eq. (6) is 6.8 x 10^{10} $eV^{-1}cm^{-2}$. D_{it}s are nearly constant near the midgap, indicating a uniform distribution of interface traps.

Figure 6 shows the body effect of the p^+ polysilicon gate p-MOSFET with the gate oxide of 70 Å and W/L of 24 μm/5 μm. Effective channel donor concentration, N_D, was assumed to be 2 x 10^{17} cm^{-3} through the SUPREM simulation and V_{FB} to be 0.9 V, for the calculation of the surface potential. Although this p-MOSFET was also ion-implanted prior to the thermal oxidation for the gate oxide, the threshold voltage shift is almost linear with respect to $(2|\phi_F| + V_{BS})^{1/2}$ up to the substrate bias of 5 V. This confirms that the effective donor concentration can be regarded as nearly uniform. The measured γ is about 0.576 $V^{1/2}$ so that the calculated N_D is about 2.4 x 10^{17} cm^{-3}. The value at the intersection of the line extrapolated to the V_T-axis is 0.023 V, so that V_{FB} is calculated as about 0.87 V, which is nearly the same as the

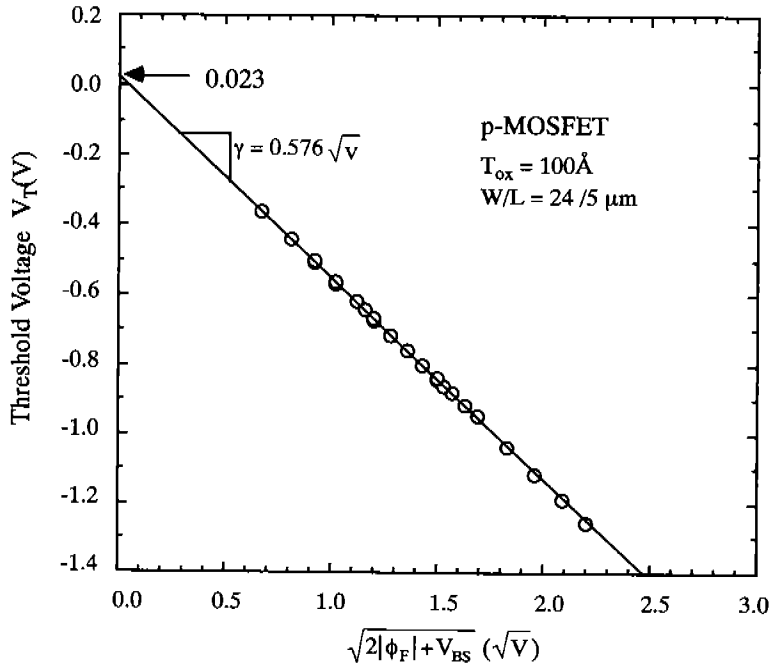

Fig. 6. Body effect of the surface-channel p-MOSFET with p^+ polysilicon gate.

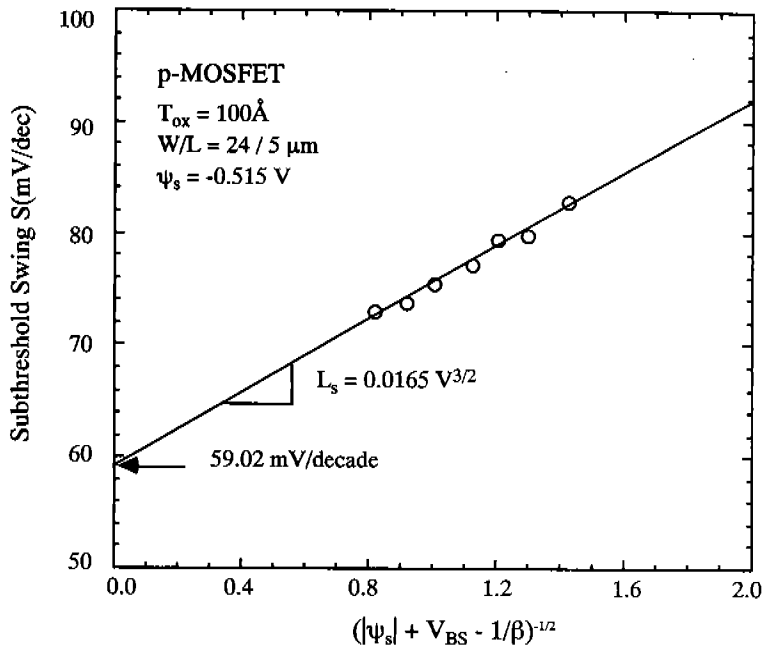

Fig. 7. The subthreshold swing dependence of the p-MOSFET on the substrate bias at the surface potential of -0.515 V.

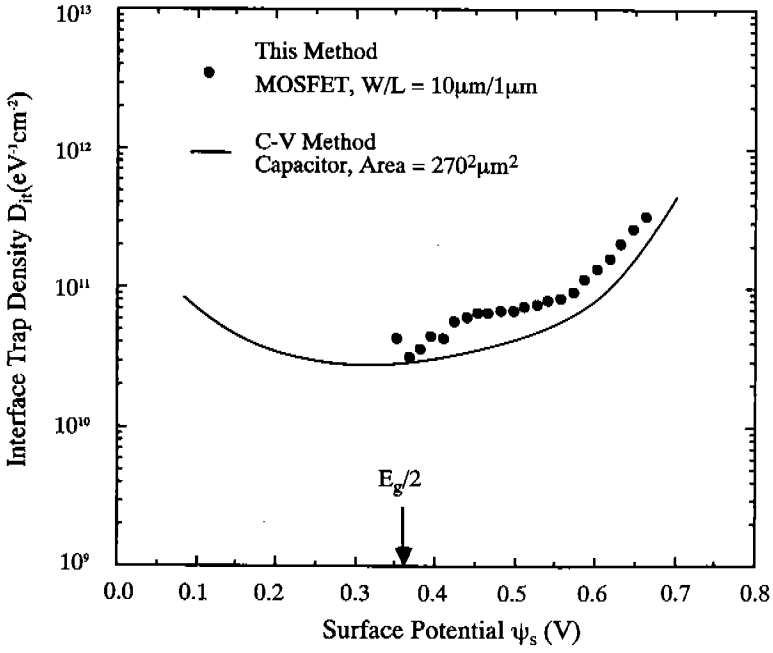

Fig. 8. The energy distribution of interface traps in the band gap for the n-MOSFET through the subthreshold slope measurement (•) and that for a capacitor through the C-V method (–).

assumed value.

The determination of D_{it} for the surface potential of -0.515 V in the p-MOSFET (Fig. 6) is shown in Fig. 7. The subthreshold shift versus $(|\psi_s| + V_{BS} - 1/\beta)^{-1/2}$ is nearly linear. L_S is approximately equal to 0.0165 $V^{3/2}$ and corresponds to the effective donor concentration of 2.3 x 10^{17} cm^{-3}, which is in good agreement with the result obtained through the body effect measurement. The measured S_∞ is 59.02 mV/decade, so that D_{it} calculated by eq. (6) is 2.63 x 10^{10} $eV^{-1}cm^{-2}$.

Figure 8 shows the comparison between the energy distribution of the interface traps in the band gap for an n-MOSFET, obtained through the subthreshold slope measurement, and that for a capacitor, obtained through the high-frequency/quasi-static C-V method. In n-MOSFETs, only interface traps in the upper half of the band gap are detectable by the subthreshold slope measurement. The difference in D_{it}s between the two is slight, although D_{it}s of the MOSFET are somewhat larger than those of the capacitor. D_{it}s are nearly constant near the midgap, indicating a uniform distribution of interface traps. As ψ_s approaches $2\phi_F$ toward the conduction band, D_{it} increases gradually, showing the same behaviour as that obtained through the high-frequency/quasi-static C-V measurement.

Another example is shown in Fig. 9, where an n-MOSFET was gate-bias stressed at a V_G of 19.6 V with a common-grounded source and drain for various periods. In this measurement, ψ_s was also

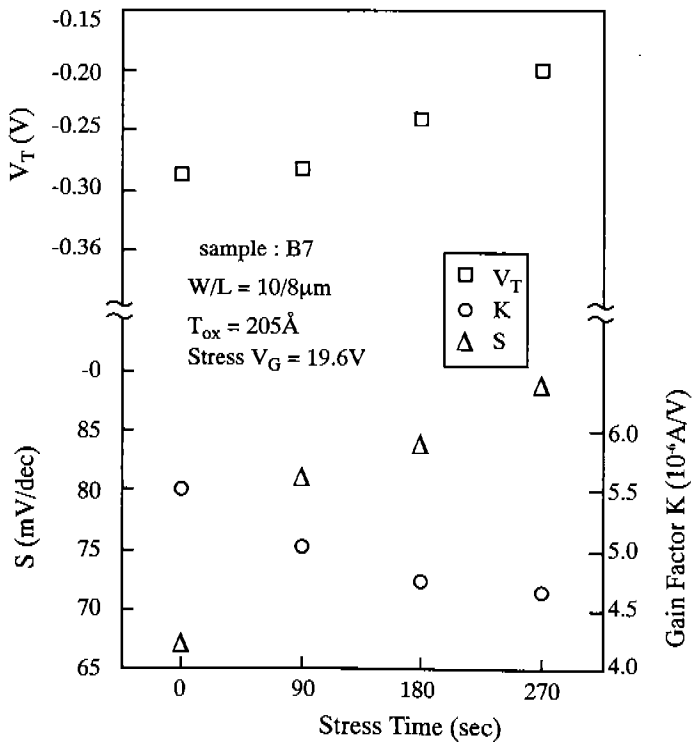

Fig. 9. Degradation of the threshold voltage, subthreshold swing and gain factor of the n-MOSFET as a function of the stress time.

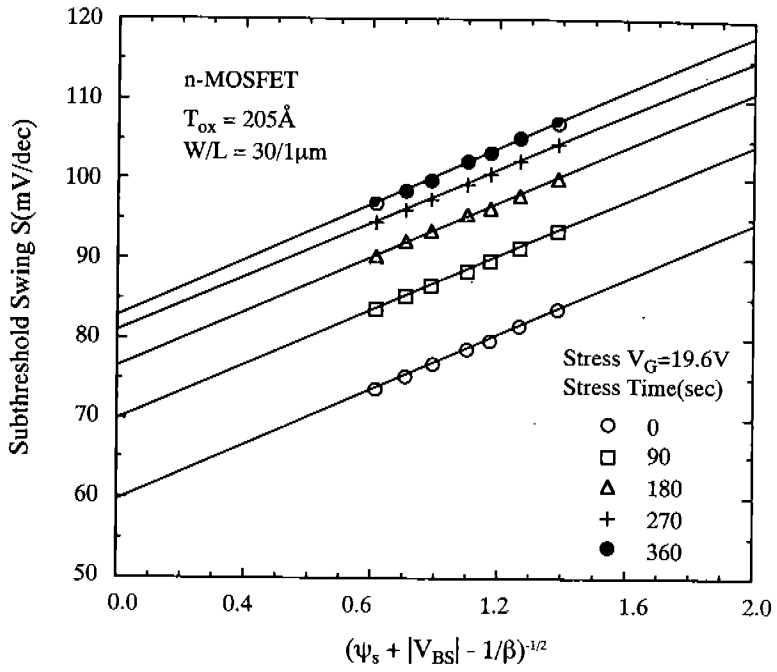

Fig. 10. Increase of the subthreshold swing by the high gate-bias stress (V_G = 19.6 V), with the stress time as a parameter.

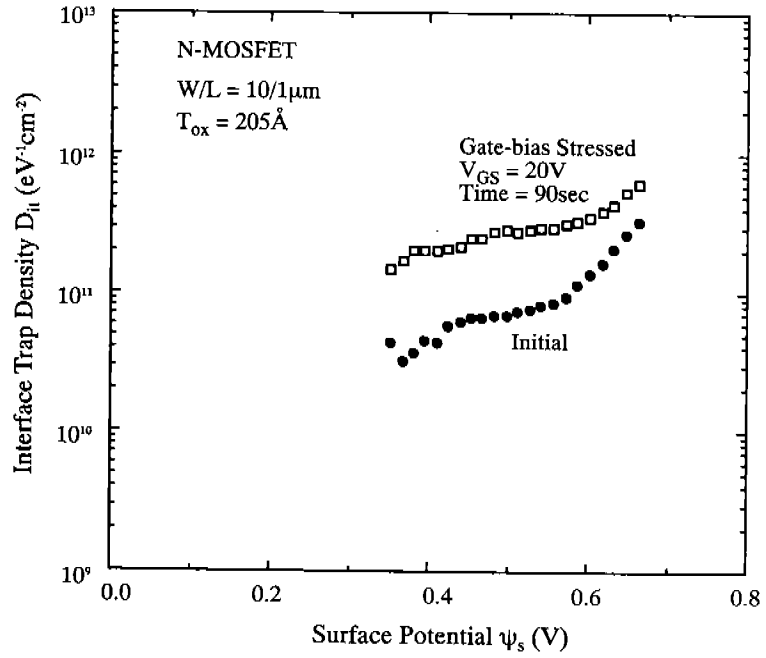

Fig. 11. The energy distribution of interface traps in the band gap for the initial (•) and the gate-bias stressed (□) n-MOSFET.

selected to be $1.5\phi_F$. As the stress goes on, the threshold voltage increases, the transistor gain factor decreases, and the subthreshold swing increases, thus degrading device performance. Increase of S_∞ with the stress time is shown in Fig. 10. S_∞ becomes larger with increasing the stress time, due to the increase of the interface trap charge. However, D_{it} is proportional not to the stress time, but rather to the logarithm of the stress time, in accordance with usual TDDB experimental results [17]. The measured S_∞ is 73.3 mV/decade for the stress time of 90 seconds so that D_{it} calculated by eq. (6) is 2.06×10^{11} $eV^{-1}cm^{-2}$.

Figure 11 shows the energy distribution of the interface trap densities in the Si band gap of a MOSFET, which is similar to that shown in Fig. 8, obtained through the subthreshold slope measurement, before and after the gate-bias stress. The stress was applied at a V_G of 20 V with a common-grounded source and drain. After stressing for 90 seconds, the average interface trap density in the gap was increased as much as 2×10^{11} $eV^{-1}cm^{-2}$ compared with the original value of about 7×10^{10} $eV^{-1}cm^{-2}$.

IV. Discussion

As mentioned above, our method for the determination of interface trap density is very useful for small size (short-channel) MOSFETs. As for the sensitivity of this method, the lowest value of D_{it} that this method can reliably determine is as follows. In eq. (6), the ratio of C_{it}/C_{ox} comprises the S_∞ value. For an oxide thickness of 100 Å, assuming a precision of 0.2 mV/decade in the measurement of S, a rough calculation based on eq. (6) shows that the resolution limit of D_{it} is about 2×10^9 $eV^{-1}cm^{-2}$. For a thinner oxide, the resolution limit becomes even larger. This is one of the limitations of our method.

Other limitations of our method are as follows. Since DIBL increases the surface potential, this also restricts the application of this method for very short-channel MOSFETs. Still, however, relative increase of the interface trap density due to charge injection in the TDDB test can be accurately estimated even for devices with appreciable DIBL effects. The effective channel dopant concentration was assumed to be constant in this analysis, whereas channels in conventional MOSFETs are nonuniformly doped due to channel ion-implantation. Step profiling is commonly used to model the threshold voltage or the body effect parameter, as shown in Fig. 12 [18]. If the depletion layer edge exists within the step profile, the average dopant concentration of the step profile may be considered to be N_A. However, if the depletion layer edge exceeds the step profile, L_S can not be defined. This also restricts the applicability of this method to MOSFETs with nonuniformly doped channels. In MOSFETs where depletion layer edges reside within the step profiles, N_As can be defined as uniform and thus effective dopant concentrations can be determined through the body effect or the subthreshold slope measurement.

In addition, the dependence of the surface mobility on the effective surface electric field and the dependence of the effective inversion layer thickness on the substrate bias were neglected in this analysis. Since, however, the subthreshold current depends exponentially on the surface potential, while the dependence of the surface mobility and the effective channel thickness is very weak, our assumption of same current at same surface potential is quite acceptable. This was confirmed by the fact that L_Ss of the MOSFETs in these experiments are nearly equal and

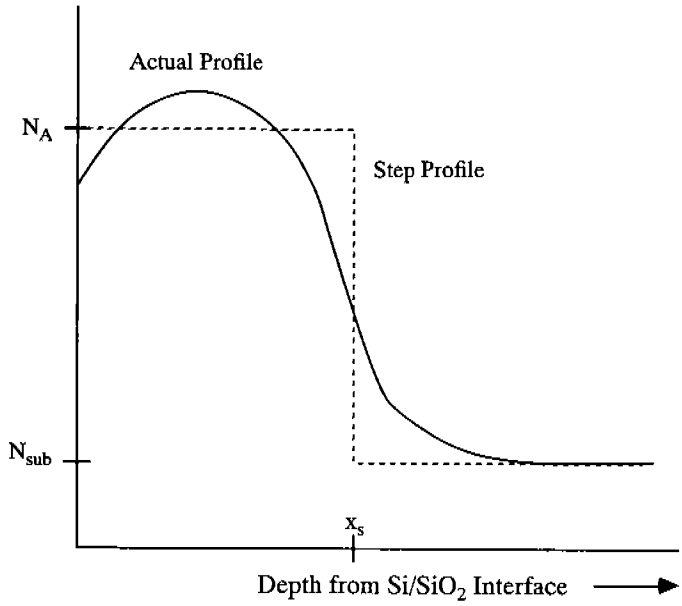

Fig. 12. Distribution of the implanted dopants (solid line) passed through activating anneal and diffusions. The dotted box curve shows the approximated distribution used to calculate the surface potential and threshold voltage.

independent of the surface potential.

V. Conclusions

Interface trap densities at SiO_2/Si interfaces of MOSFETs were determined through the measurement of the substrate bias dependence of the subthreshold slope. With this method, we can analyze SiO_2/Si interfaces of small-size MOSFETs fabricated using special process technologies or stressed by high electric fields. For calculating the surface potential, effective channel dopant concentrations were estimated using the SUPREM simulation and flat-band voltages from the work function difference. Assumed effective dopant concentrations were compared with the experimental results obtained through the body effect and subthreshold slope measurements. The subthreshold slope technique was proven to yield reasonable results for short-channel MOSFETs. The result of the application of this technique to a large MOSFET showed good agreement with the result obtained through the high-frequency/quasi-static C-V technique for a MOS capacitor. The accuracy in this measurement of the interface trap density is higher compared with the conventional subthreshold slope measurement, because the depletion layer capacitance is eliminated from the analysis and the trap density is determined using S_∞. Furthermore, the effective substrate dopant concentration can also be obtained as a by-product through the subthreshold slope measurement and showed good agreement with the result obtained through the body effect measurement. Therefore, the gate oxide quality, passing through full processing

steps, gamma irradiation or TDDB test, can be easily monitored. However, the D_{it} increase due to hot carrier stresses is not simply monitored by this method, in which degradations may be confined to the oxide near the polysilicon edge.

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