# Channel Protection Layer Effect on the Performance of Oxide TFTs

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**We have investigated the channel protection layer (PL) effect on the performance of an oxide thin film transistor (TFT) with a staggered top gate ZnO TFT and Al-doped zinc tin oxide (AZTO) TFT. Deposition of an ultra-thin PL on oxide semiconductor films enables TFTs to behave well by protecting the channel from a photo-resist (PR) stripper which removes the depleted surface of the active layer and increases the carrier amount in the channel. In addition, adopting a PL prevents channel contamination from the organic PR and results in high mobility and small subthreshold swings. The PL process plays a critical role in the performance of oxide TFTs. When a plasma process is introduced on the surface of an active layer during the PL process, and as the plasma power is increased, the TFT characteristics degrade, resulting in lower mobility and higher threshold voltage. Therefore, it is very important to form an interface using a minimized plasma process.**

**Keywords: ZnO TFT, AZTO TFT, channel protection layer, ALD, bias stability.**

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## I. Introduction

Since the release of reports on a transparent amorphous InGaZnO thin film transistor (TFT) by Hosono and others [1] and a polycrystalline ZnO TFT by Wager and others [2], oxide semiconductors have attracted an astonishing amount of attention [3]. These are currently the subject of intensive material research, as they have diverse applications in displays, memory devices, and other electronics, such as ring oscillators [4]-[6]. The main concern in the area of displays is the application of oxide TFTs to the backplane of active matrix organic light emitting diodes (AM-OLEDs) [7], TFT-LCDs [8], and electronic paper (e-paper) [9]. Oxide TFTs, which can be fabricated uniformly on a large substrate, have both high mobility and good stability. Therefore, we believe that oxide TFTs are the best candidate, especially for OLED driving devices.

Most oxide TFTs are comprised of sputtered zinc oxide [10], indium gallium zinc oxide (IGZO) [11], zinc tin oxide (ZTO)-based oxide [12], [13], or indium zinc oxide (IZO) [14], and several ZnO TFTs fabricated by atomic layer deposition have also been reported [15], [16]. Some of them have shown promising performance for application in an AM-OLED in terms of mobility. However, most of the research has focused on the composition of an oxide semiconductor, process parameters, thermal annealing conditions, semiconductor deposition methods, and electrical analyses, such as bias stability. Very few experimental works have been reported on the process effects on device performance [17].

It has been well established that the gate insulator/semiconductor interface has played the most important role in TFT performance [18], [19]. In this study, we report on how the gate insulator/semiconductor interface

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formation process affects oxide TFT performance in a staggered top gate structure with the adoption of an ultra-thin channel protection layer (PL). In addition, we investigate the effects of the PL process on the ZnO TFT characteristics.

## II. Experiment

A transparent ZnO TFT and an Al-doped ZnSnO (AZTO) TFT were fabricated on a glass substrate by means of plasma-enhanced atomic layer deposition (PEALD) and sputtering, respectively, with the structure shown in Fig. 1. For the fabrication of ZnO TFT, 150 nm thick Sn-doped indium oxide (ITO) was deposited on the glass as source/drain (S/D) electrodes by sputtering and was then patterned using a wet etching process. ZnO film was deposited via PEALD [20] at a substrate temperature of 150°C using diethylzinc (DEZ) and in situ generated oxygen plasma as a Zn and oxygen precursor at an RF power of 60 W. The reactor pressure was kept at 3 Torr. In the PEALD method, the precursors were alternatively injected into the reactor using Ar as a carrier gas with a flow rate of 80 sccm. The pulsing times were 2.5 s for the DEZ, 1.5 s for oxygen plasma, and 4 s for Ar purge. A radio frequency pulse was applied at 60 W during the injection of $O_2$ gas for 1.5 s to generate oxygen plasma in situ. After 20 nm thick ZnO film deposition, 9 nm thick alumina, as a ZnO PL that also acts as a first gate insulator, was deposited at 150°C using PEALD at RF powers of 60 W, 100 W, or 130 W [21]. For PL growth, trimethylaluminum (TMA), and oxygen plasma were used as Al and O precursors, respectively. The active layer of ZnO and alumina (PL) was patterned via wet etching using a diluted HF solution. For comparison, another ZnO film was directly patterned without a PL, followed by deposition of a gate insulator, alumina. The gate insulator, a second alumina, was deposited with a thickness of 176 nm at a temperature of 150°C by means of ALD using TMA and water, followed by S/D pad opening by wet etching of the alumina using concentrated $H_3PO_4$. A sputtered ITO was used as a gate electrode. For the fabrication of an AZTO TFT, a 20 nm thick AZTO layer was formed by the co-sputtering of an $Al_2O_3$-ZnO (ZnO:Al) target and an $SnO_2$ target using an off-axis type RF magnetron sputter at room temperature [22]. The sputtering was performed in a mixed atmosphere of Ar and $O_2$ with a chamber pressure of 0.2 Pa. We deposited alumina as a PL using TMA and water as Al and O precursors, respectively, via ALD at 200°C [23]. AZTO and $Al_2O_3$ films were also patterned, and the following processes were each the same as those of the ZnO TFT. Here again, we fabricated a comparison device that does not adopt a PL, and a gate insulator, alumina, was directly deposited onto a patterned AZTO film. After fabrication of the TFTs, we carried out post annealing at 200°C for 2 hours for the ZnO TFT and at 300°C for 2 hours for the AZTO TFT.

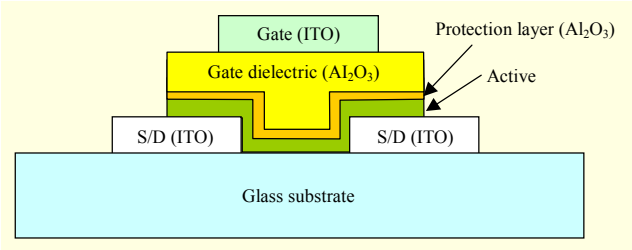


Fig. 1. Cross-sectional view of a top gate oxide TFT with an oxide semiconductor protection layer.

Measurement of the characteristics of the TFT was conducted using an HP 4156 semiconductor parameter analyzer. A dielectric constant of 7.4 was obtained for alumina grown by ALD at 150°C by measuring the capacitance of a capacitor made using ITO as electrodes. The mobility ($\mu$) and threshold voltage ($V_{th}$) of the TFT were calculated using the saturation current equation of a field-effect transistor. The $V_{th}$ was extracted according to the square root $I_d$ vs. gate voltage ($V_g$) plot.

## III. Results and Discussion

Polycrystalline ZnO, especially deposited using ALD or PEALD, is easily attacked even by a weak base such as a photo-resist (PR) stripper. Therefore, lithography process damage causes serious performance degradation of a ZnO TFT with a thin active layer. This led us to use an ultra-thin PL for ZnO, which covers the ZnO simply for protection during the patterning process. We had to be very careful in the selection of ZnO PL, which practically acts as a first gate insulator, as most gate insulators such as $SiN_x$, or $SiO_2$ deposited on an active layer using the plasma enhanced chemical vapor deposition (PECVD) method can make ZnO film conductive due to the H incorporation [24]. A shallow donor level generated by hydrogen can be formed in ZnO during the gate dielectric process to increase the carrier amounts in the active layer. Instead of gate insulators by PECVD, we adopted an alumina grown using PEALD at 150°C with an RF power of 60 W. The thickness of the PL, alumina, was optimized to 9 nm so that the ZnO could be protected from the PR and PR stripper.

Figure 2 shows the characteristics of ZnO TFTs with and without a PL. We could not even determine the $V_{on}$ [25] of the ZnO TFT without PL because the drain current as a function of the gate voltage is almost linear within the general gate voltage range. We attributed this to the high carrier amount in the active layer and lots of charge trap site in the interface. On the contrary, adopting a PL of only 9 nm changed the TFT performance dramatically. It behaved in enhanced mode with a mobility of 2.4 $cm^2/V \cdot s$ and a $V_{th}$ of 22.7 V.

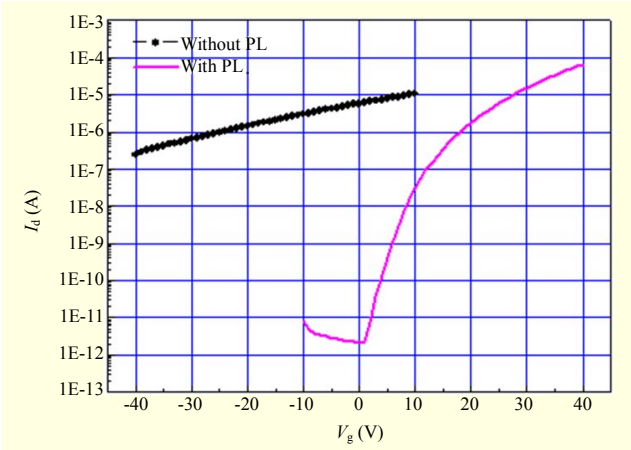


Fig. 2. $I_{ds}$–$V_{gs}$ transfer curves of ZnO TFTs with and without an alumina PL at $V_{ds}$=15.5 V (W=40 μm, L=20 μm).

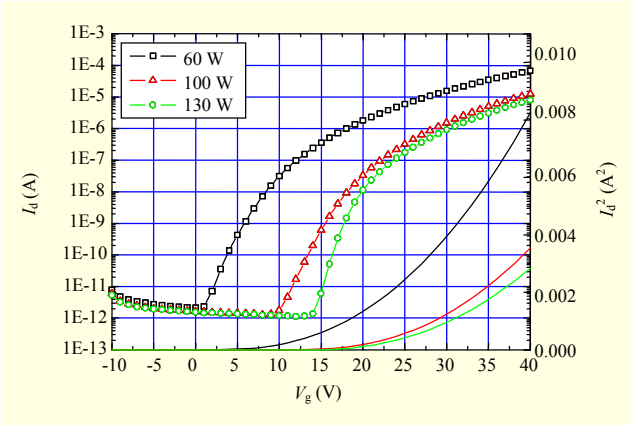


Fig. 3. $I_{ds}$–$V_{gs}$ transfer curves of ZnO TFTs with a PL deposited at various plasma powers of 60 W, 100 W, and 130 W ($V_{ds}$=15.5 V, W=40 μm, L=20 μm).

When the ZnO film is exposed to a wet process, two possibilities should be considered. One is the exposure to water. It is known that water can be chemically adsorbed into an oxide film to generate an extra electron on the surface [26]. In the case of polycrystalline ZnO, water can penetrate into the active layer to generate electrons not only at the surface but also in the bulk film. Therefore, we have to apply a much higher negative voltage to deplete the whole channel as shown in Fig. 2. The other possibility to be considered is the PR stripper effect. A ZnO surface can also be exposed to oxygen in air, and adsorbed oxygen can form peroxide ($O^{2-}$) or $O^-$ that depletes the back channel [27]. However, a PR stripper, the base, gets rid of the surface of the depleted ZnO film, again increasing electrons in a channel and making ZnO too conductive. The increased carrier from both effects and defects generated in both the channel and bulk film degrade the TFT behavior as shown in Fig. 2.

To investigate the effects of the PL process, we changed the plasma power during alumina deposition from 60 W to 130 W. Figure 3 shows the transfer curves of TFTs that have ZnO film deposited with an RF power of 60 W and a PL deposited with RF powers of 60 W, 100 W, or 130 W. The mobility of the ZnO TFT with a PL deposited at 60 W, 100 W, and 130 W of plasma power are 0.94 cm$^2$/V·s, 0.63 cm$^2$/V·s, and 0.64 cm$^2$/V·s, respectively. Since the mobility of a ZnO TFT is quite dependent on the applied electrical field [28], we calculated the mobility at a position of 25 V higher at the turn-on voltage ($V_{on}$) to compare the device performance fairly.

While the subthreshold swings (SSs) of devices with a PL deposited at 60 W, 100 W, and 130 W are 1.7, 1.8, and 1.2 V/decade, the threshold voltages are 22.7 V, 26.4 V, and 26.9 V, respectively. Increased plasma power during alumina growth resulted in increased hysteresis as well. It seems that a high plasma power for the growth of a PL (the first gate insulator) induces charge trap sites in the interface to cause the hysteresis of TFTs and shift of $V_{th}$ to the higher voltage. Although the SSs are decreased due to the effect of reducing oxygen vacancy in the ZnO film with the help of oxygen plasma as the RF power for the PL process increases, most of the device performance is degraded with the increased RF power. This suggests that a minimization of plasma damage during the gate insulator process will be important for improving device performance.

To investigate the PL effect on other oxide semiconductors, particularly those that are relatively inert to a PR stripper, we fabricated top gate AZTO TFTs with and without a PL. In the case of the AZTO TFT, we adopted an alumina PL deposited with a water precursor instead of oxygen plasma since we discovered that the plasma process for the interface induces severe damage to the device [7]. When alumina is deposited with water, only a surface chemical reaction occurs between the chemisorbed TMA and water, and other side effects caused by plasma are not a concern.

Figure 4 shows the transfer characteristics of AZTO TFTs. Contrary to the ZnO TFT which has a semiconductor film that is very sensitive to the water and base solution of PR stripper, the semiconductor film of the AZTO TFT is relatively inert to these chemicals and shows typical TFT performance without a PL. It has a mobility of 4.8 cm$^2$/V·s, $V_{th}$ of 0.98 V, and SS of 1.0 V/decade, while those of a TFT with a PL are 10.9 cm$^2$/V·s, 4.05 V, and 0.26 V/decade. One notable thing is the hysteresis of an AZTO TFT without a PL compared to that with a PL. A large hysteresis may originate from the organic residue of PR in the interface. To get rid of this kind of residue completely, we can use oxygen plasma. This, however, induces more severe plasma damage to the interface, resulting in a larger hysteresis than in an AZTO TFT without a PL (the transfer curve is not shown here). The lower mobility and higher SS of an AZTO without a PL also indicate that there is serious

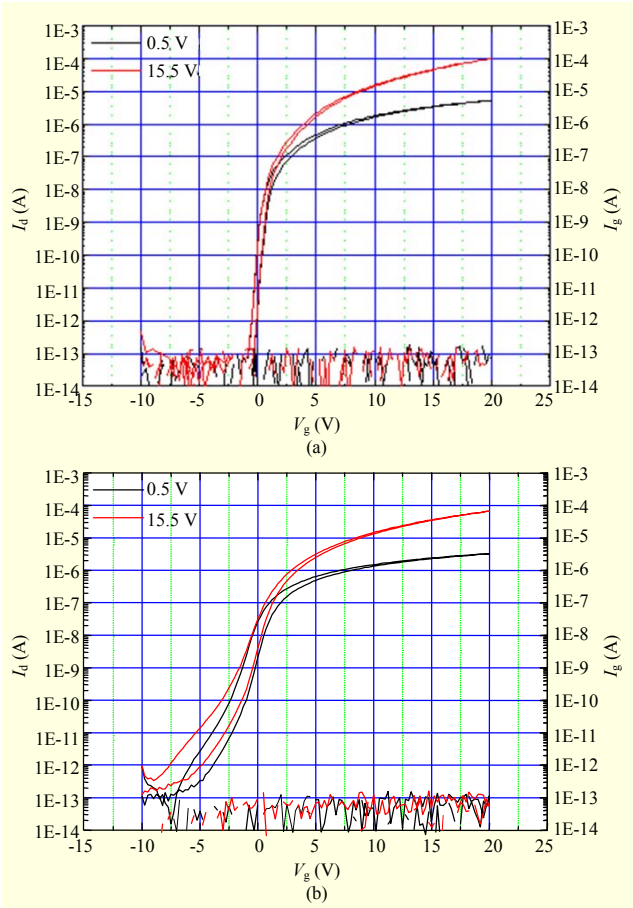


Fig. 4. $I_{ds}$–$V_{gs}$ transfer curves of AZTO TFTs (a) with and (b) without a PL (W=40 μm, L=20 μm).

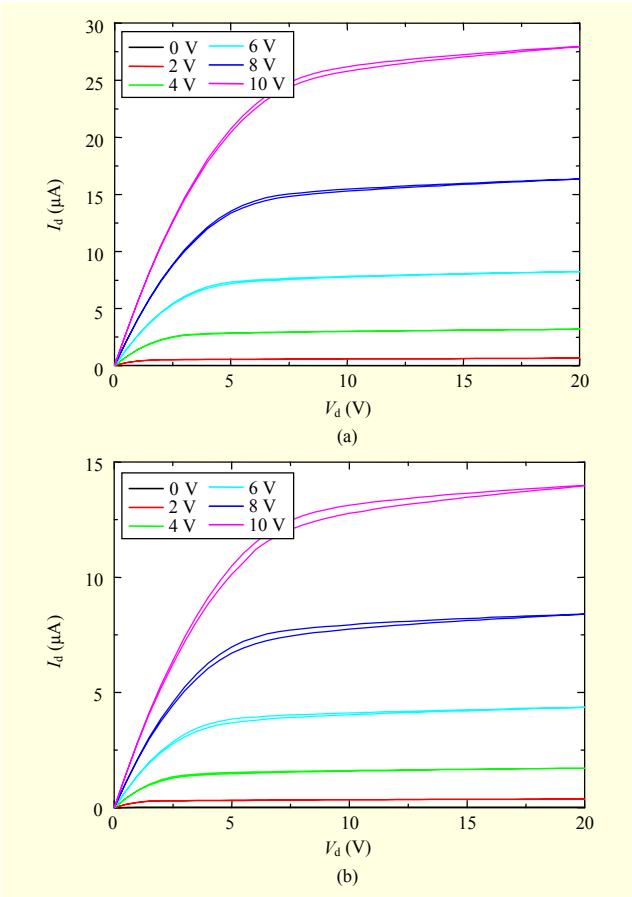


Fig. 5. $I_{ds}$–$V_{ds}$ output curves of AZTO TFTs (a) with and (b) without a PL (W=40 μm, L=20 μm).

interface degradation during the active patterning process. When we fabricated the AZTO TFT, the sputtered AZTO film was exposed to air in order to deposit a PL in a PEALD chamber. This means that the main role of a PL in an oxide TFT is not to protect the oxide layer from water in air, but to protect the channel from damage during the photolithography process. The AZTO TFT without a PL also shows a smaller $V_{th}$ than that with a PL as in the ZnO TFT. This supports the behavior of a PR stripper, which removes the depleted surface even though the active layer is not dissolved by the stripper well. Figures 5(a) and (b) show the drain current-drain voltage ($I_D$-$V_D$) output curves of AZTO TFTs with and without a PL, respectively. They show typical TFT characteristics, although the AZTO TFT without a PL shows a lower $I_D$ than the other AZTO TFT with a PL.

We investigated the bias stability of the AZTO TFT without and with a PL as shown in Fig. 6. When we applied a $V_{gs}$ of 20 V during 7,200 s, the $V_{th}$ of the AZTO TFT with a PL shifted only 0.33 V. Most of the $V_{th}$ shift occurred within the first 1,000 s, and it became saturated after 1,000 s at 0.33 V. Meanwhile, under a negative bias stress of -20 V, the $V_{th}$ shift was almost negligible (the data is not shown here). Although the SS is not good, even the AZTO TFT without a PL shows relatively stable behavior under gate bias stress. This is mostly due to the high chemical stability of the AZTO film and plasma free interface formation with the bulk alumina gate insulator grown using water precursor. The AZTO TFT with a PL is pretty stable with a good transfer curve under bias stress. This means that channel protection using a PL is very important, and, in particular, a plasma damage free process for the PL is necessary to obtain a highly stable oxide TFT.

## IV. Conclusion

We investigated the channel protection layer effect on the performance of oxide TFTs using a top gate ZnO TFT and AZTO TFT. Deposition of an ultra-thin PL on the oxide films enables TFTs to behave well by protecting the channel from the PR stripper, which removes the depleted surface of the active layer. In addition, adopting a PL prevents channel contamination from an organic PR and results in high mobility and a small SS. The PL process plays a critical role in the

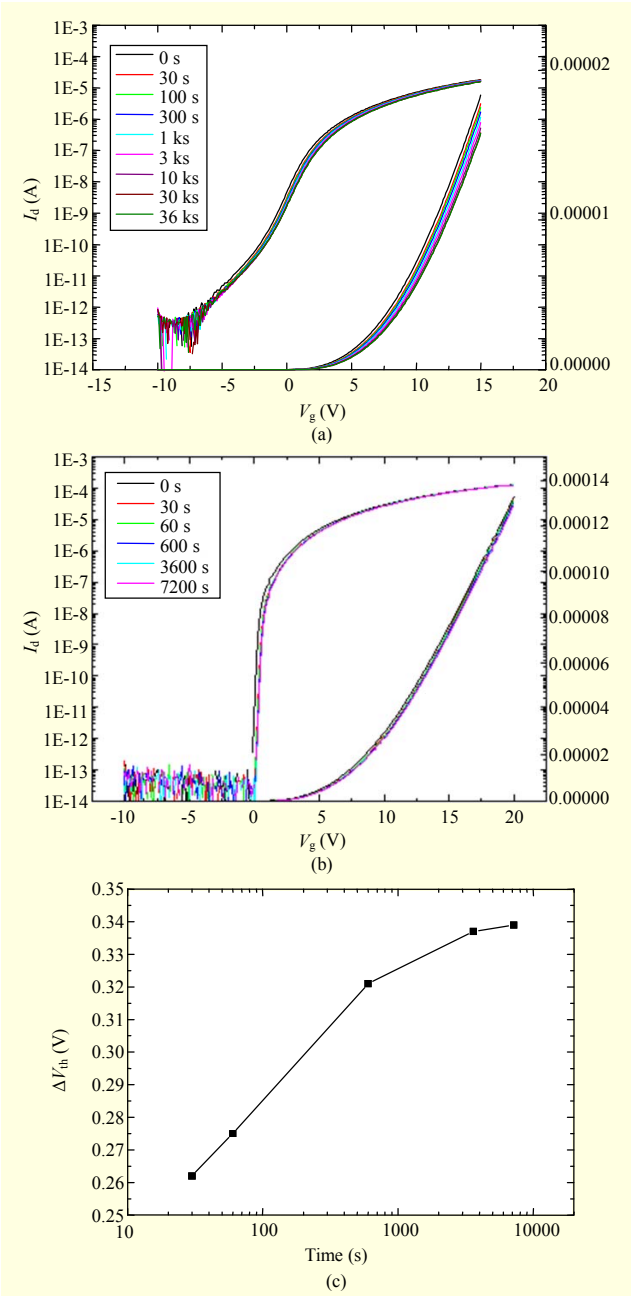


Fig. 6. Change of transfer curve of AZTO TFT (a) without PL, (b) with PL, and (c) $\Delta V_{th}$ under a positive bias stress of 20 V for up to 7200 s.

performance of oxide TFTs. When plasma damage is induced on the surface of an active layer during the PL process, the TFT characteristics are degraded, resulting in lower mobility, and higher threshold voltage. Therefore, it is very important to form an interface without plasma damage during the PL process.

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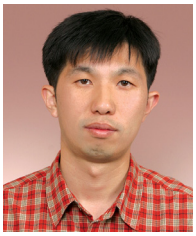

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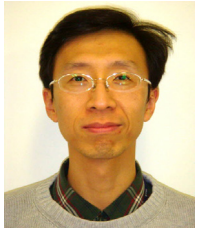

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