Highly Linear and Efficient Microwave GaN HEMT Doherty Amplifier for WCDMA

Yong-Sub Lee, Mun-Woo Lee, and Yoon-Ha Jeong

ABSTRACT—A highly linear and efficient GaN HEMT Doherty amplifier for wideband code division multiple access (WCDMA) repeaters is presented. For better performance, the adaptive gate bias control of the peaking amplifier using the power tracking circuit and the shunt capacitors is employed. The measured one-carrier WCDMA results show an adjacent channel leakage ratio of -43.2 dBc at ±2.5-MHz offset with a power added efficiency of 40.1% at an average output power of 37 dBm, which is a 7.5 dB back-off power from the saturated output power.

Keywords—Doherty amplifier, efficiency, gallium nitride (GaN), wideband code division multiple access (WCDMA).

I. Introduction

Current higher data rate modulation and multi-carrier application systems require high-linearity and high-efficiency power amplifiers which depend on power transistors with high compression points, excellent thermal stability, and increasingly high frequency response. The gallium nitride (GaN) high mobility electron transistor (HEMT) is a promising candidate for high power RF applications because GaN HEMT transistors exhibit very high power densities, high electron saturation velocity, high operating temperature, and high cutoff frequency compared to other technologies [1], [2].

In this letter, we report a highly linear and efficient GaN HEMT Doherty power amplifier (DPA). To improve linearity without extra linearization techniques, derivative superposition linearization (DSL) is employed with adaptive gate bias control of the peaking amplifier ($V_{gs,p}$), using the power tracking circuit and the shunt capacitor. For verification, a two-way GaN HEMT DPA is implemented and tested using one-carrier wideband code division multiple access (WCDMA) signals at 2.14 GHz. The measured results show a highly linear and efficient GaN HEMT DPA.

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II. Linearity Improvement of GaN HEMT DPA

1. Derivative Superposition

DSL has emerged as a useful circuit-level linearization technique, being conceptually simple, requiring no significant increase in circuit complexity or precise circuit tuning, and achieving good performance. As DSL is constructed by placing two or more devices in parallel, which may have different gate biases, this technique can be easily applied to the Doherty configuration [3].

Figure 1 shows the schematic diagram of a GaN HEMT DPA, which consists of a carrier amplifier and a peaking amplifier. Two amplifiers are simply modeled by voltage-controlled nonlinear current sources, where each current source

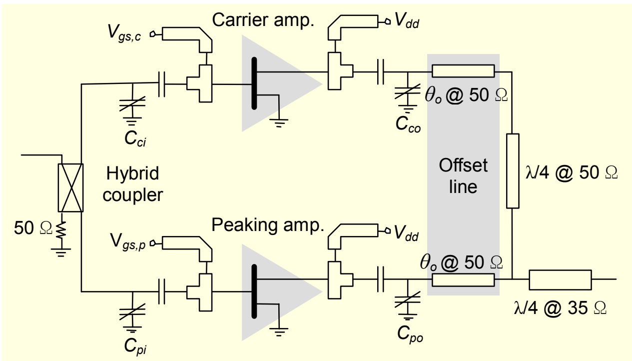

Fig. 1. Schematic of the GaN HEMT DPA.

is represented by a Taylor-series expansion to the third-order, as given in [4] as

$$I_D(v_{GS}) = \frac{\partial I_D}{\partial v_{GS}} v_{GS} + \frac{1}{2}\frac{\partial^2 I_D}{\partial v_{GS}^2} v_{GS}^2 + \frac{1}{6}\frac{\partial^3 I_D}{\partial v_{GS}^3} v_{GS}^3 + \cdots \quad (1)$$
$$= G_m v_{GS} + G_{m2} v_{GS}^2 + G_{m3} v_{GS}^3 + \cdots,$$

where G_m is the transfer function derivative.

The carrier and peaking amplifiers are at different bias conditions, so the coefficients in the Taylor-series polynomials will be different for each amplifier. Here, we apply a two-tone input signal to the carrier and peaking amplifiers of the DPA:

$$v_{GS} = V_S(\cos\omega_1 t + \cos\omega_2 t), \quad (2)$$

where V_s is magnitude of the input signal. The upper-band third-order intermodulation (IM3) components of the carrier and peaking amplifiers at the output of the DPA can be respectively expressed as

$$I_{D,c}(2\omega_2 - \omega_1) = \frac{3}{4} \cdot G_{m3,c} \cdot V_s^3 \cdot e^{j\phi_c}, \quad (3)$$

$$I_{D,p}(2\omega_2 - \omega_1) = \frac{3}{4} \cdot G_{m3,p} \cdot V_s^3 \cdot e^{j\phi_p}, \quad (4)$$

where ϕ_c and ϕ_p are phases of the carrier and peaking amplifier, respectively, which depend on the gate bias voltage. Thus, (3) and (4) can be used for the IM3 cancellation using the derivative superposition because the significant cancellation of the IM3 components can be obtained when two amplifiers are biased on opposite sides of the IM3 null.

2. Adaptive Gate Bias Supply Using Power Tracking

The adaptive bias supply circuit is constructed by using the power tracking circuit, which does not track the actual envelope of the signal, but changes the supply voltage based on the average power level. Thus, the power supply circuit does not need to be fast-switching or wide bandwidth. Moreover, there are no delay mismatch limitations because a delay line is unnecessary [5].

Figure 2 shows the schematic of the proposed power tracking circuit with power detection and bias supply circuits. The input signal extracted by a directional coupler is transformed to the constant voltage value through the power detection circuit, which consists of a logarithmic detector and a rectifier. A logarithmic detector using Analog Device's AD8326 has a measurement range of over 60 dB and a resolution of about 0.05 V/dBm. The rectifier comprises a Schottky diode, a resistor, and a capacitor. The gate bias supply circuit modulates the detected voltage (V_{det}) to adaptively control $V_{gs,p}$ in the DPA. The circuit consists of an inverting op-amp with a dc-offset voltage and a limiting circuit. Figure 3 shows the V_{det} and optimum gate bias voltage traces according to output power levels. When the gate bias of the carrier amplifier ($V_{gs,c}$) is fixed to -1.43 V, the $V_{gs,p}$ is set to constant in the low power region by the limiting circuit, but decreases according to output power levels.

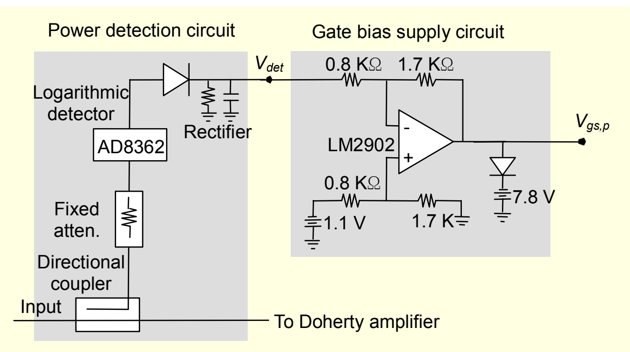

Fig. 2. Adaptive bias supply circuit using power tracking method.

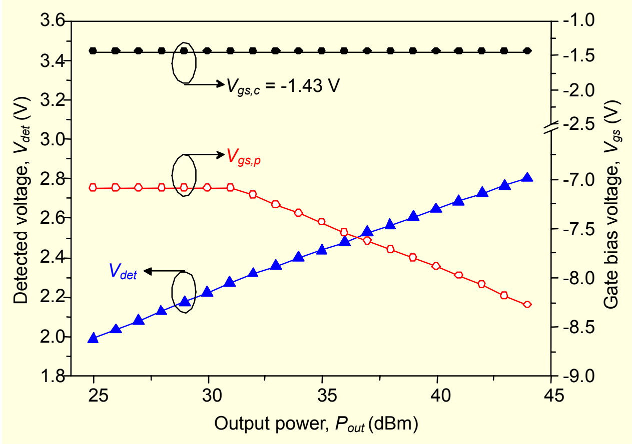

Fig. 3. Detected voltage and optimum gate bias voltage traces.

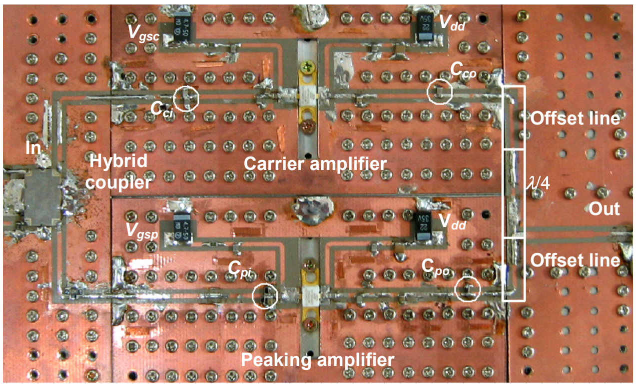

Fig. 4. Photograph of the fabricated GaN HEMT DPA.

III. Implementation and Experimental Results

The DPA was implemented using Nitronex NPTB00025 GaN HEMTs and an RF35 (H=0.5 mm, ε_r=3.5) circuit board at 2.14 GHz. In the process of determining the optimum length of the offset line, the output impedance of 15.7+j×20 Ω was

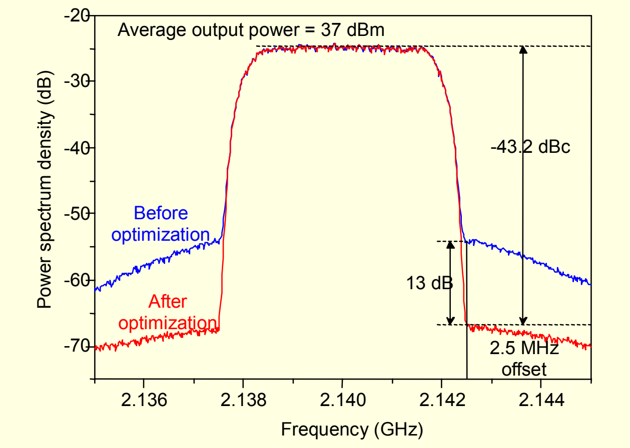

Fig. 5. Measured power spectrum densities at a P_{out} of 37 dBm.

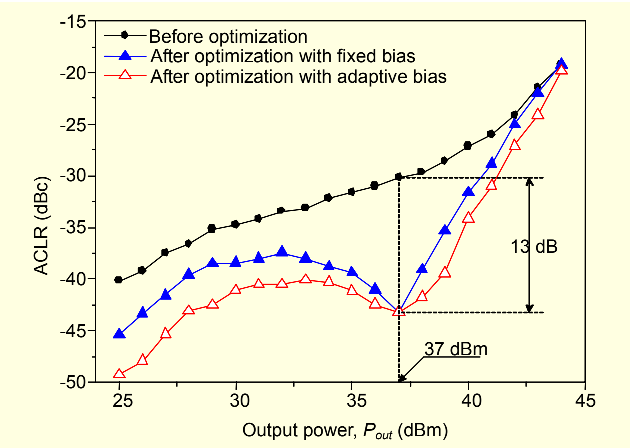

Fig. 6. Measured ACLR characteristics for various conditions.

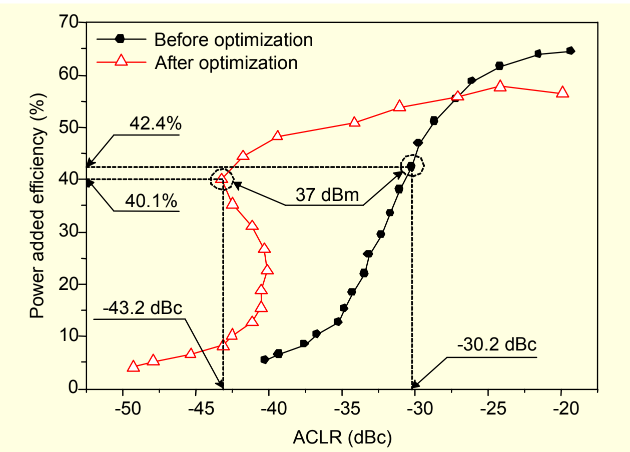

Fig. 7. Measured PAE vs. ACLR characteristics.

transformed to 189 Ω by the 0.18λ-long 50 Ω offset line. To reduce memory effects, the drain bias circuit incorporated a λ/4 bias line and several tantalum decoupling capacitors. The shunt capacitors were optimized to improve linearity at a P_{out} of 37 dBm, and the capacitances of C_{ci}, C_{co}, C_{pi}, and C_{po} were 0.9 pF, 0.5 pF, 0.4 pF, and 1.3 pF, respectively. For comparison, the DPA before optimization was biased to the $V_{gs,c}$ of -1.51 V and $V_{gs,p}$ of -5.4 V with a V_{dd} of 28 V. The DPA after optimization had an adaptive $V_{gs,p}$ control with a fixed $V_{gs,c}$ of -1.43 V and V_{dd} of 28 V at each output power level. Figure 4 is a photograph of the fabricated GaN HEMT DPA.

Figure 5 shows the measured power spectrum densities of a GaN HEMT DPA for a one-carrier WCDMA signal at a P_{out} of 37 dBm. After optimization with a $V_{gs,p}$ of -7.63 V, an ACLR of -43.2 dBc was achieved at ±2.5-MHz offset, which is an improvement of 13 dB over a GaN HEMT DPA before optimization. Figure 6 shows the measured ACLR characteristics according to output power levels. When the $V_{gs,p}$ was adaptively controlled by the power tracking circuit with the gate bias traces, as shown in Fig. 3, a good ACLR performance was achieved over a wide output power range. Figure 7 shows that the GaN HEMT DPA can deliver an ACLR of -43.2 dBc with a PAE of 40.1%.

IV. Conclusion

We proposed a highly linear and efficient GaN HEMT DPA for WCDMA repeaters. To improve the linearity of a GaN HEMT DPA with high efficiency, DSL is employed with an adaptive gate bias control of the peaking amplifier using a power tracking circuit and additional shunt capacitors in each matching circuit. A DPA was designed and implemented using Nitronex NPTB00025 GaN HEMTs and tested using a one-carrier WCDMA signal at 2.14 GHz. At a P_{out} of 37 dBm, the GaN HEMT DPA delivered an ACLR of -43.2 dBc with a PAE of 40.1%.

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