A 6 Gbps/pin Low-Power Half-Duplex Active Cross-Coupled LVDS Transceiver with Switched Termination

Sua Kim, Bai-Sun Kong, Chilgee Lee, Changhyun Kim, and Young-Hyun Jun

ABSTRACT—A novel linear switched termination active cross-coupled low-voltage differential signaling (LVDS) transceiver operating at 1.5 GHz clock frequency is presented. On the transmitter side, an active cross-coupled linear output driver and a switched termination scheme are applied to achieve high speed with low current. On the receiver side, a shared pre-amplifier scheme is employed to reduce power consumption. The proposed LVDS transceiver implemented in an 80 nm CMOS process is successfully demonstrated to provide a data rate of 6 Gbps/pin, an output data window of 147 ps peak-to-peak, and a data swing of 196 mV. The power consumption is measured to be 4.2 mW/pin at 1.2 V.

Keywords—LVDS, half-duplex, transceiver, DRAM, I/O.

I. Introduction

The full-duplex low-voltage differential signaling (LVDS) interface has been a choice in wireless mobile systems due to low power consumption. However, it is becoming harder to achieve low power consumption with the emergence of new applications requiring higher data transfer rates [1]. The full-duplex current-mode logic signaling, which has been widely used in desktop systems with little bandwidth restriction, is unsuitable for wireless systems due to its high power consumption. To cope with these problems, a high-bandwidth half-duplex LVDS interface has been proposed for applications requiring large-scale graphic data transfer, low power consumption, and large-scale integration [2].

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II. Circuit Implementation

1. Active Cross-Coupled (ACC) LVDS

For the conventional LVDS interface shown in Fig. 1(a) [3], the transmitter requires an input with a wide high-speed swing. It is very difficult to provide this with the pre-driver due to wide common-mode operation. To circumvent this drawback, an active cross-coupled (ACC) driver can be adopted to reduce the input swing. The proposed ACC LVDS transmitter is improved by sharing the pre-amplifier of the receiver as the fully differential amplifier for the transmitter in a half-duplex signaling system as shown in Fig. 1(b). By sharing a part of the circuit in the transmitter and the receiver, the static power dissipation and the chip size overhead could be effectively minimized.

2. Half-Duplex Linear LVDS with Switched Termination

Current flow models for four different LVDS interfaces

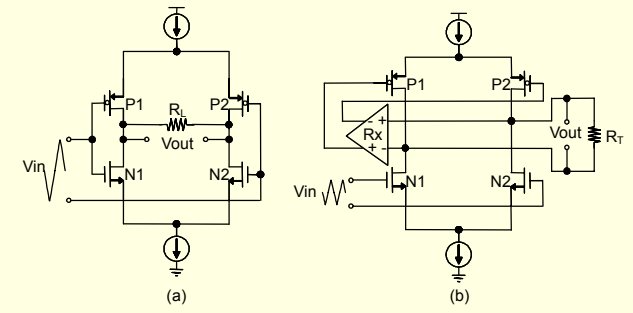

Fig. 1. (a) Conventional LVDS and (b) shared ACC LVDS.

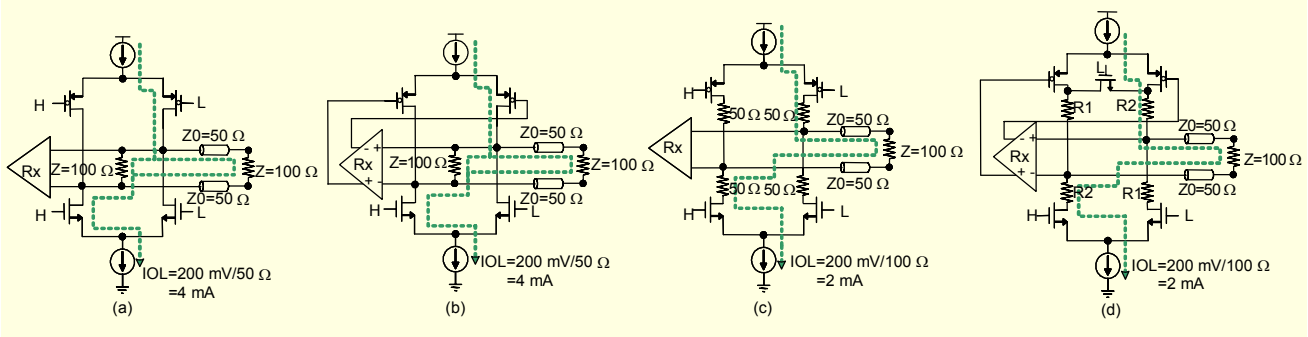

Fig. 2. (a) Conventional LVDS, (b) ACC LVDS, (c) linear LVDS, and (d) linear switched termination ACC LVDS.

are shown in Fig. 2. The conventional LVDS shown in Fig. 2(a) has a termination on each side of the transceiver, showing the advantage of a high-speed channel environment. However, the interface still suffers from speed limitation due to rail-to-rail swing of pre-driver outputs. As explained in the previous section, this dilemma can be overcome by using a shared ACC LVDS as shown in Fig. 2(b). Although the reduction of input common-mode range allows high-speed operation, the interface dissipates a lot of current (4 mA) due to termination on both sides. A linear LVDS interface with external termination only on the receiver side and a linear driver with serially connected passive resistors on the transmitter side, whose total impedance is well matched to the line impedance, can reduce current consumption to 2 mA as shown in Fig. 2(c). Finally, as shown in Fig. 2(d), the switched termination is added to the linear LVDS driver, where it can be turned on to maintain AC termination on the receiver side while receiving data, and turned off to guarantee the driver linearity while sending data.

3. Half-Duplex Linear Active Cross-Coupled LVDS with Switched Termination

Figure 3 shows the detailed architecture of the proposed half-duplex linear switched termination ACC LVDS transceiver. The transmitter (Tx) consists of a MUX, a 2-to-1 pre-driver, and a linear LVDS output driver. The receiver (Rx) has a pre-amplifier and four latched sense amplifiers. The outputs of the receiver pre-amplifier are fed into the PMOS output drivers to use the pre-amplifier as the differential amplifier for active cross-coupling. The linear switched termination driver with passive resistors is adopted to reduce static power consumption and to improve signaling bandwidth. The pre-driver of the transmitter has a two-tapped structure for input data multiplexing. High-speed operation of pre-driver outputs, *q* and *qb*, is realized by making effective use of a common-mode control explained in the next sub-section. Since data is separately delivered to PMOS and NMOS drivers for their

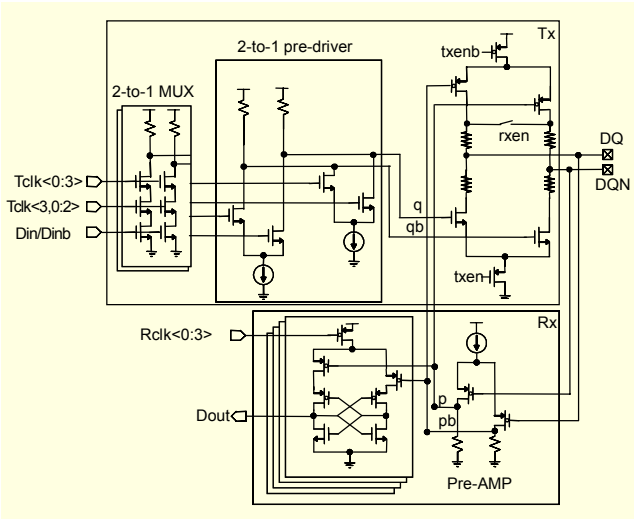

Fig. 3. Proposed linear switched termination ACC LVDS transceiver architecture.

independent common-mode control, a small overhead is incurred in the MUX, pre-driver, and bias circuitry with transmitter jitter a little worse due to data flow along different paths. The pre-amplifier in the receiver, which receives channel data *DQ* and *DQN* as inputs, can work so fast that possible detrimental effects can be suppressed.

4. Calibration Control

A current and impedance calibration scheme is incorporated in our work. Figure 4 shows a simplified block diagram of the control loop of the bias current and the common-mode level of the PMOS and NMOS output drivers. In the circuit, the replica current sources of the drivers are segmented into several binary-weighted groups. The target current and the common-mode level can be adjusted by the closed-loop control. The linearity and impedance of the driver can also be regulated by a dual-loop calibration loop similar to that for driver current control. In the calibration loop, PMOS and NMOS driver replicas with previously adjusted currents are used instead of

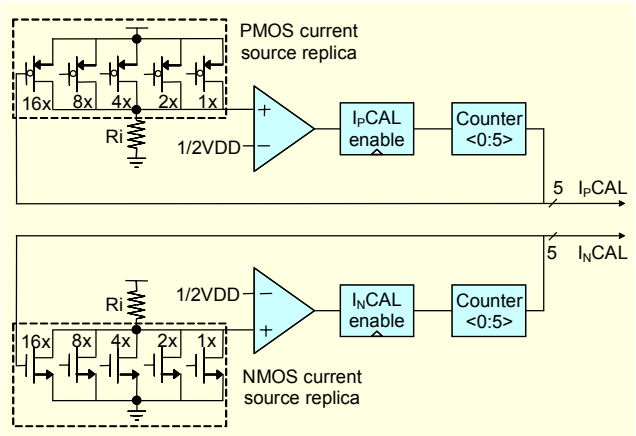

Fig. 4. Driver current calibration control loop.

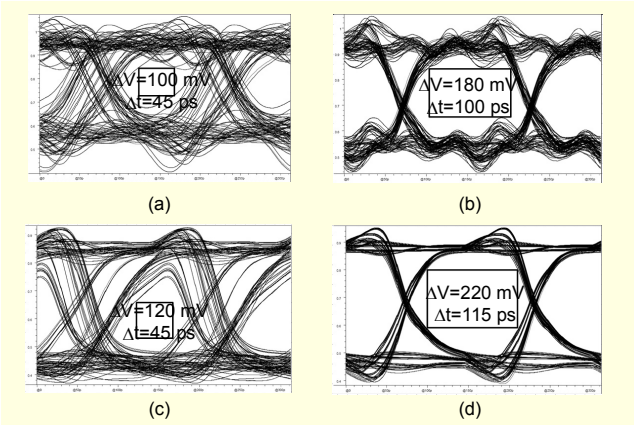

Fig. 5. (a) Conventional LVDS, (b) ACC LVDS, (c) linear LVDS, and (d) linear switched termination ACC LVDS.

current source replicas. Calibration of the output impedance and common-mode level should be finished before the system is ready to transmit and receive data. In our work, the driver nonlinearity is successfully suppressed to less than 10% of its full operating range, yielding a much lower switching current.

III. Test Results

Figure 5 shows the simulated channel eye-diagram for the four types of LVDS interfaces shown in Fig. 2. For conventional and linear LVDSs, the frequency limitation caused by an incomplete pre-driver output swing is observed as shown in Figs. 5(a) and (c). For the ACC LVDS, the channel distortion due to driver nonlinearity is shown in Fig. 5(b). The simulated channel eye-diagram of the proposed LVDS shown in Fig. 5(d) shows a channel performance of 6.4 Gbps. This level of performance was provided by adopting the ACC scheme to reduce the pre-driver output swing and by using a linear switched termination driver to guarantee driver linearity and exact termination resistance.

Fig. 6. Output eye-diagram at 6 Gbps/pin.

Table 1. Performance summary.

Supply volatge	1.8 V, 1.65 V minimum
I/O voltage	1.2 V, 1.05 minimum
Technology	80 nm DRAM process
Output voltage eye-open	196 mV pk-pk
On-chip termination value	50 ± 5 ohm
Clock frequency	1.5 GHz
Maximum data rate	6.0 Gbps/pin
DQ power/pin @ 6 Gbps	4.2 mW @ Tx mode
Transmit jitter @ 6 Gbps	25.65 ps rms, 47.31 ps pk-pk
Output data window @ 6 Gbps	153 ps rms, 147 ps pk-pk

A prototype interface using the proposed switched-termination linear ACC LVDS transceiver was designed and fabricated in an 80 nm DRAM technology. The interface was located in the peripheral area of DRAM, so the transceiver could be easily affected by the noise generated in DRAM cell array. Even under this unfavorable condition, our work can provide a relatively wide output data window. The eye-diagram for the interface is shown in Fig. 6, and the performance of the proposed LVDS transceiver is summarized in Table 1. As these results demonstrate, the proposed LVDS transceiver achieves a maximum data rate of 6.0 Gbps/pin with a 153 ps rms output data window. The measured power per pin is approximately 4.2 mW at 1.2 V.

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