A Ka-Band 6-W High Power MMIC Amplifier with High Linearity for VSAT Applications

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A Ka-band 6-W high power microwave monolithic integrated circuit amplifier for use in a very small aperture terminal system requiring high linearity is designed and fabricated using commercial 0.15-μm GaAs pHEMT technology. This three-stage amplifier, with a chip size of 22.1 mm^2 can achieve a saturated output power of 6 W with a 21% power-added efficiency and 15-dB small signal gain over a frequency range of 28.5 GHz to 30.5 GHz. To obtain high linearity, the amplifier employs a class-A bias and demonstrates an output third-order intercept point of greater than 43.5 dBm over the above-mentioned frequency range.

Keywords: Ka-band, microwave monolithic integrated circuit (MMIC), high power amplifier (HPA), linearity, output third-order intercept point (OIP3), very small aperture terminal (VSAT).

I. Introduction

A high power amplifier (HPA) is a key component of a very small aperture terminal (VSAT) transmitter for Ka-band satellite communications. Owing to the distortion caused by an HPA in the transmit path, an HPA typically uses a 6-dB to 10-dB back-off from the 1-dB compression point (P1dB) output power to achieve the necessary level of an output third-order intercept point (OIP3) [1]. If the required linearity can be achieved with an HPA module at a lower back-off from the P1dB point, several advantages, such as less DC power consumption, can be achieved.

Many VSAT applications require HPA modules with power levels of as high as 10 W with high linearity to provide the proper link margin. From a linearity point of view, Hittite

HMC906 [2] provides an attractive performance. Its OIP3 is as high as 42 dBm, but its maximum output power level is only 2 W. To realize a 10-W HPA module, as many as eight chips may be required. A microwave monolithic integrated circuit (MMIC) HPA with the highest maximum power is currently a TriQuint TGA4916 [3] at 7 W. However, this chip has an OIP3 of lower than 40 dBm, which is too low to comply with the linearity requirement of HPA modules. A comparison of the results [2]-[7] reported to date for Ka-band HPAs is shown in Table 1.

In this letter, a Ka-band 6-W HPA with a high linearity is designed based on commercial 0.15-μm GaAs technology. To improve the linearity, we adopt a class-A bias point. Additionally, an active bias circuit is used for compensating the threshold voltage and temperature variations, along with an independent bias of supply voltage variations, which we previously reported for the Ku-band [8]. A three-stage amplifier demonstrates a saturated output power of 6 W with 21% power-added efficiency (PAE) and an OIP3 of 43.5 dBm over a frequency range of 28.5 GHz to 30.5 GHz. The 6-W maximum output power and 43.5-dBm OIP3 enable the use of only two chips for a 10-W HPA module while providing sufficient linearity.

II. Power Amplifier Design

A 6-W three-stage cascaded HPA is designed using a commercial foundry based on a WIN-Semiconductor 0.15-μm GaAs pHEMT [9] with a 50-μm thick substrate. The process provides two terminal HEMTs with a gate-to-drain breakdown voltage of −10 V, a transconductance of 495 mS/mm, and a maximum current density of 650 mA/mm. A simplified block diagram for the 6-W HPA is shown in Fig. 1. The 6-W HPA is

Table 1. Comparison of Ka-band power amplifier MMICs.

Reference	Process	Operating frequency (GHz)	V_{DS} (V)	Gain (dB)	P_{out} (W)	PAE (%)	P1dB (dBm)	OIP3 (dBm)	Chip area (mm²)
This work	0.15-GaAs pHEMT	28.5 to 30.5	5.2	15	6	21	37.5	43.5	22.1
[2]	0.25-GaAs pHEMT	27.3 to 33.5	6	23	2	22	32.5	42	8.7
[3]	0.15-GaAs pHEMT	29 to 31	6	21	7	18	38	40	22
[4]	0.15-GaAs pHEMT	28 to 31	6	24	4	21	36	39	8.6
[5]	0.25-GaAs pHEMT	28 to 32	6.5	30	5.5	25	37	-	25.1
[6]	0.15-GaAs pHMET	26 to 32	6	20	4	25	36	-	8.6
[7]	0.15-GaAs pHMET	28 to 31	5	30	6	-	37.5	-	21

Fig. 1. Functional block diagram of Ka-band MMIC HPA.

Fig. 2. Schematic diagram of single-cell amplifier and active bias circuit.

realized using two 4-W HPAs in parallel, combined using Lange couplers, which provide an improved voltage standing wave ratio performance at the input and output ports of the HPA chip.

The 4-W HPA employs 1:2:4 gate periphery ratios to provide sufficient power margins between stages. The peripheries of the pHEMTs are 1.6 mm (4×4f100), 3.2 mm (8×4f100), and 6.4 mm (16×4f100) for the first, second, and power stages, respectively. Loadpull measurements show a power density of 0.75 W/mm at an optimum bias of 5.0 V and 250 mA/mm. The loadpull/sourcepull simulation of a 400-μm HEMT cell (4f100) reveals a maximum output power of 24 dBm with 43% PAE under a drain voltage of 5.0 V and a gate voltage of −0.8 V at 30 GHz.

To achieve a stability factor of $K > 1$ over a wide frequency band, two parallel-combined resistors (R1, R2) and a capacitor (C1) are connected to an input of a 4f100 HEMT, as shown in Fig. 2. The values of the resistors and capacitor are carefully selected to provide no degradation with a maximum output power, sacrificing some gain decrease. All HEMT cells shown
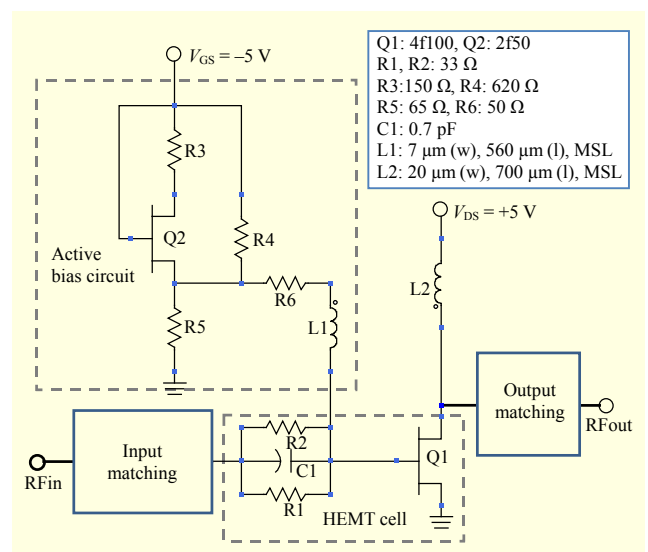
in Fig. 1 include a stability circuit to guarantee sufficient stability for the HPA.

The functions of an active gate bias circuit include the DC gate bias of the amplifiers, compensating threshold voltage, and temperature variations. A bias circuit is composed of resistors (R3 to R5) and transistors (Q2), as shown in Fig. 2. The proper values of the components provide a suitable gate bias of −0.8 V with an external input bias (VG) of −5 V. The R6 resistor is used for blocking RF leakage into the bias circuit [8].

The MMIC HPA is designed using a simple process, as shown in Fig. 3. To improve the linearity, we adopted a class-A bias point. Figure 3(a) shows the simulation results of the I-V curve for the 4f100 HEMT, which reveal that a breakdown occurs at 10-V drain-to-source voltage (V_{DS}). The optimum bias points for the maximum output power were determined as −0.8-V gate-to-source voltage (V_{GS}), +5-V V_{DS}, and 72-mA drain-to-source current (I_{DS}). The input-matching and two inter-

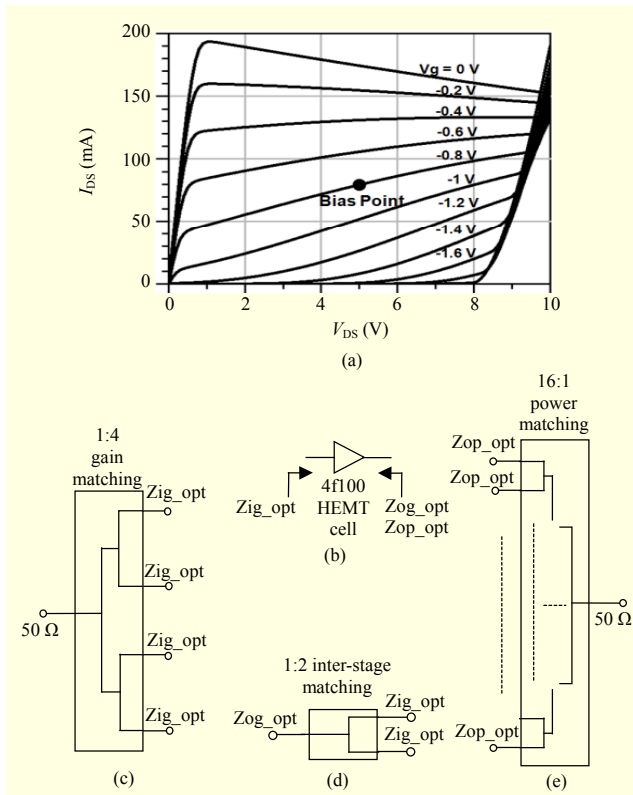Fig. 3. Design procedure of Ka-band MMIC HPA.

Fig. 4. Microphotograph of fabricated Ka-band 6-W MMIC HPA. Chip size is 4.7 mm × 4.7 mm.

stage matching networks are optimized for high gain, while the output matching network is optimized to obtain a higher output power based on the loadpull/sourcepull simulation. All microstrip lines are fully optimized through the EM simulation.

The MMIC HPA design starts from extracting the optimum input (Zig_opt) and output (Zog_opt) impedances for the maximum gain and optimum output (Zop_opt) impedance for the maximum output power for the HEMT cell, as shown in Fig. 3(b). To achieve a compact design, we adopt a proper matching topology using shunt capacitors instead of open stubs using microstrip lines. To design a 1:4 gain matching circuit, the impedances of the input and output ports are set to 50 Ω and Zig_opt, respectively, as shown in Fig. 3(c). For the 1:2 inter-stage matching circuit, the input and output port impedances are set to Zog_opt and Zig_opt, respectively, as shown in Fig. 3(d). For the 16:1 power matching circuit, the input port impedances are set to the optimum power impedance, Zop_opt, while the output port impedance is set to 50 Ω, as shown in Fig. 3(e). The matching circuits are designed for each circuit to provide desirable input and output return losses over a wide frequency band, considering a compact chip size.

III. Measured Results and Comparison
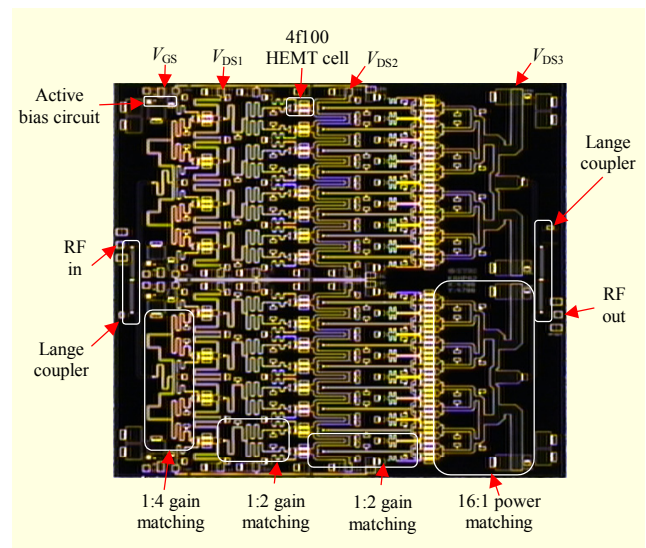
Figure 4 shows a microphotograph of the fabricated Ka-band

6-W MMIC HPA. The size of the chip is 4.7 mm × 4.7 mm with a thickness of 0.05 mm. There are many biasing pads for two 4-W HPAs combined in this chip. Three stages of the 4-W HPA share the same gate bias pads through the active bias circuit, while drain biasing must be supplied to each stage and both sides of the 4-W HPA to stay below the rated current limits of the bias lines and to preserve the signal balance between parallel combined HEMT cells.

All tests are done based on the CW measurement at ambient temperature. Each MMIC PA is mounted in a CuW test fixture with 2.9-mm k-connectors, which is mounted on a heat sinking plane with a fan for effective thermal dissipation. Following measured data of the MMIC PA is compensated according to the measured loss of the test fixture. The small signal gain, as well as the input and output return losses versus frequency, is measured. The DC voltages, V_{DS} and V_{GS}, are set to +5.2 V and −5 V, respectively, and a 4.3-A quiescent DC current is supplied. The small signal gain is normally 15 dB, while the input and output return losses are lower than −12 dB from 28 GHz to 31 GHz, as shown in Fig. 5.

The output power, gain, and PAE as a function of input power over a frequency range of 28.5 GHz to 30.5 GHz are shown in Fig. 6. It can be seen that the saturated output power (P_{sat}) is normally 38 dBm (6 W), and the PAE varies between 21% and 24% at the saturated output. At an input power of 24 dBm, the output power variation is less than 0.25 dB over the frequency range. At the saturation level, the DC current is measured as 5.3 A for the same DC voltage setting as a small signal measurement.

The measured OIP3, as well as the P_{sat} and P1dB as a function of frequency, is depicted in Fig. 7. To obtain the OIP3,
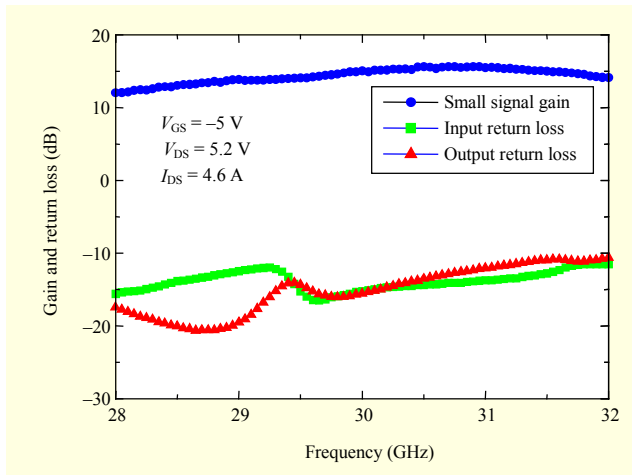
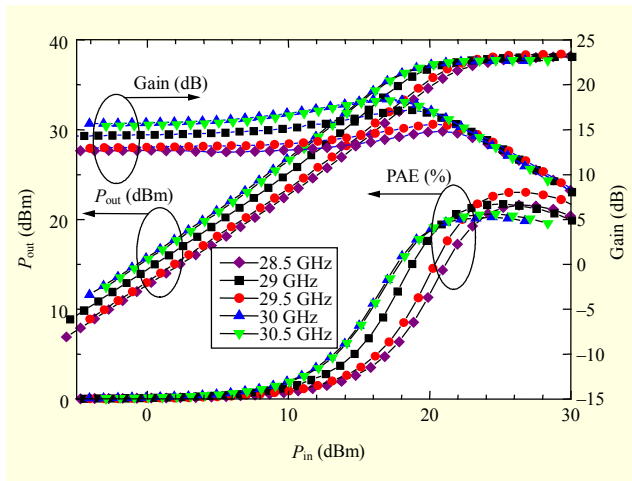Fig. 5. Measured small-signal gain, input return loss, and output return loss vs. frequency of Ka-band HPA.

Fig. 6. Measured CW output power, PAE, and gain of Ka-band HPA; $V_{DS} = 5.2$ V and I_{DS} (quiescent) $= 4.6$ A.
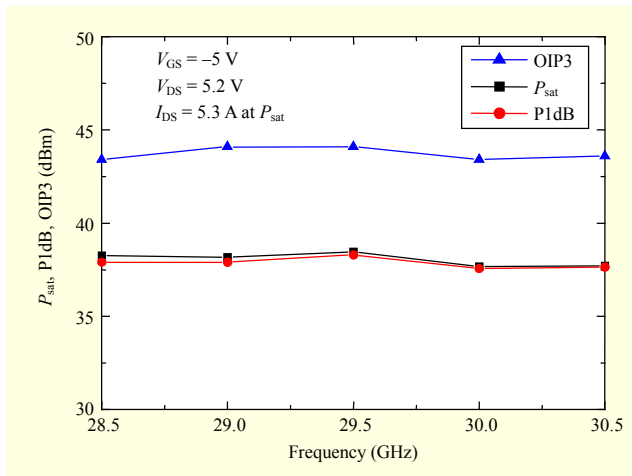

Fig. 7. Measured P_{sat}, P1dB, and OIP3 vs. frequency; $V_{DS} = 5.2$ V and $I_{DS} = 5.3$ A at P_{sat}.

the third-order inter-modulation distortion (IMD3) is measured at the input of two-tone signals with 10-MHz spacing. The amplifier demonstrates an OIP3 of more than 43.5 dBm and a P_{sat} of 38 dBm. The difference between the P_{sat} and P1dB is less than 0.5 dB over a frequency range of 28.5 GHz to 30.5 GHz. The 6-W MMIC HPA characteristics are summarized in Table 1. From a performance comparison with the reported results, it can be observed that the OIP3 and maximum output power of our works are better than in other designs.

IV. Conclusion

In this letter, we presented a highly linear monolithic high power amplifier operating from 28.5 GHz to 30.5 GHz for VSAT applications. The amplifier demonstrated a saturation output power of 38 dBm (6 W) and an OIP3 of greater than 43.5 dBm with a peak power-added efficiency of 21%. We believe that this chip with high power and high OIP3 will be a suitable candidate for realizing a highly linear transmitter module for Ka-band VSAT systems.

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