# Binary Power Amplifier with 2-Bit Sigma-Delta Modulation Method for EER Transmitter

Jiyoun Lim, Sanghoon Cheon, Kyeong-Hak Kim, Songcheol Hong, and Dong-Wook Kim

**A novel power amplifier for a polar transmitter is proposed to achieve better spectral performance for a wideband envelope signal. In the proposed scheme, 2-bit sigma-delta (ΣΔ) modulation of the envelope signal is introduced, and the power amplifier configuration is modified in a binary form to accommodate the 2-bit digitized envelope signals. The 2-bit ΣΔ modulator lowers the noise of the envelope signal by fine quantization and thus enhances the spectral property of the RF signal. The Ptolemy simulation results of the proposed structure show that the spectral noise is reduced by 10 dB in a full transmit band of the EDGE system. The dynamic range is also enhanced. Since the performance is improved without increasing the over-sampling ratio, this technique is best suited for wireless communication with high data rates.**

**Keywords: Power amplifier, envelope elimination and restoration (EER), sigma-delta (ΣΔ) modulator, polar transmitter.**

## I. Introduction

High performance transmitters are a key component for next generation mobile communication systems. Two important specifications of transmitters are efficiency and linearity, which are mainly determined by a power amplifier. Recently, many advanced power amplifiers and transmitters have been studied and developed for practical applications [1]. Among a variety of the transmitter architectures, Kahn's polar structure using the envelope elimination and restoration (EER) method [2] has attracted much attention from researchers. The architecture enhances linearity by separating an input signal into envelope and phase signals. Efficiency is maintained using an efficient switching mode power amplifier. To improve the performance of the EER transmitter, a sigma-delta (ΣΔ) modulation technique has been applied to digitize the envelope signal [3]-[5]. The ΣΔ modulator improves signal quality by pushing the quantization noise away from the interested frequency band. This is achieved by the over-sampling technique. The importance of the EER architecture is that it is an example of the systems digitizing the envelope signals. How to implement a digital transmitter is one of the most important issues in mobile communication systems. The EER method can be used by the digital transmitter and combined with the schemes using digital PLL or a digital frequency synthesizer [6].

In this paper, we discuss ΣΔ modulation of the envelope signal in an EER transmitter and propose a new 2-bit ΣΔ modulation technique. To handle the 2-bit digitized envelope signals, a new power amplifier configuration is introduced. After investigating effects of the order and over-sampling ratio (OSR) of the ΣΔ modulator on the output signal, we discuss the proposed 2-bit ΣΔ modulation scheme and the binary power amplifier.

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## II. Sigma-Delta (ΣΔ) Modulation of Envelope Signal

### 1. EER Transmitter with ΣΔ Modulator

We analyze the ΣΔ modulation of the envelope signal through Agilent ADS Ptolemy simulation. Figure 1 shows the architecture of the EER transmitter, which mainly consists of two paths for the envelope and phase signals. Some works [3], [4] use a band-pass filter at the power amplifier output instead of a low-pass filter as in conventional EER architecture. However, the architecture with the band-pass filter has difficulty in removing quantization noise in the transmit band because it is impractical to implement a band selectable band-pass filter [5]. Therefore, the low-pass filter is utilized in our architecture as in a conventional EER transmitter.

In the envelope path, a ΣΔ modulator converts the analog envelope signal to a digital one to drive the Class-S amplifier. The low-pass filter following the amplifier should be carefully chosen, because it significantly affects the signal property, especially in the transmit band outside a channel. Since the frequency-dependent group delay does not affect the performance of the transmitter [5], we choose a simple third-order Butterworth filter with maximally flat magnitude. The delay difference between the envelope and phase signals is adjusted in the phase path before RF signal is restored. The delay is 0.4 μsec, which is caused mainly by the low-pass filter. The RF power amplifier combines the envelope and phase signals and then amplifies the restored RF signal. To focus on the performance with various ΣΔ modulators, an ideal switching-mode power amplifier is assumed.

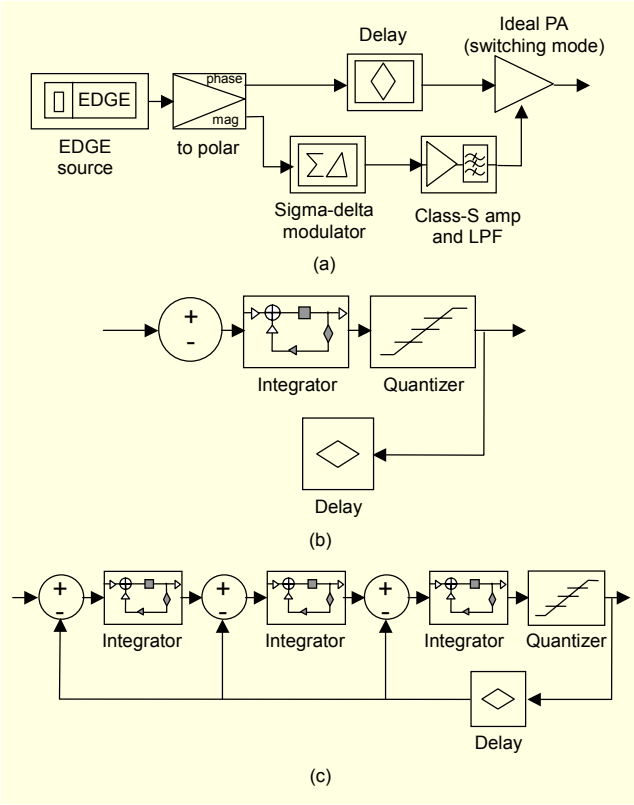


Fig. 1. EER transmitter architecture and ΣΔ modulators: (a) EER transmitter architecture with ΣΔ modulator, (b) first-order ΣΔ modulator, and (c) third-order ΣΔ modulator.

Figures 1(b) and (c) show block diagrams of first-order and third-order ΣΔ modulators, respectively. The first-order ΣΔ modulator consists of an integrator, quantizer, and delay component in a feedback path. In a high-order ΣΔ modulator, the two compensation functions of feedforward and feedback can be applied for high frequency stability [7]. Since both techniques provide the same noise transfer function, we use the simple feedback method in our simulation. Figure 1(c) shows the third-order ΣΔ modulator including three series-connected integrators and a quantizer. There is only one delay component in the feedback path. To study the effect of the ΣΔ modulator order on the transmitter performance, the output of the third-order modulator is 2-level quantized like that of the first-order modulator. We choose the coefficients in reference [8] for our simulations. In our simulation, the EDGE signal with an RF carrier at 897.5 MHz is used as an input signal.

### 2. Order and OSR of ΣΔ Modulator

In a wideband mobile communication system, the EER transmitter needs to reduce the quantization noise of the envelope signal. In the ΣΔ modulation method, signal quality is enhanced by noise shaping and oversampling. The noise shaping property is due to band-pass filtering of the ΣΔ modulation scheme, and the in-band noise is greatly suppressed as the order of the modulator increases [9].

Figure 2 shows output spectra of the first-order and third-order modulators. The OSR of the ΣΔ modulators is 256. With a low signal power of -10 dBm, the output of the transmitter with the first-order ΣΔ modulator fails to meet the EDGE spectral mask requirement, whereas the transmitter with the third-order ΣΔ modulator shows better performance. However, when the input signal power is as high as 5 dBm, the third-order ΣΔ modulator shows worse spectral property than the first-order modulator does. The output signal with the third-order ΣΔ modulator violates the system spectral mask and even fails to restore the input signal. This can be explained by the saturation of the integrator in the high-order ΣΔ modulator as in the time domain waveforms shown in Fig. 3. Accordingly, the dynamic range is reduced as the order of the ΣΔ modulator increases. In the case of the third-order ΣΔ modulator, the maximum allowed input power has a ratio of 0.7 compared to that of the first-order ΣΔ modulator [8]. Therefore, increasing the order of the ΣΔ modulator limits the noise shaping and

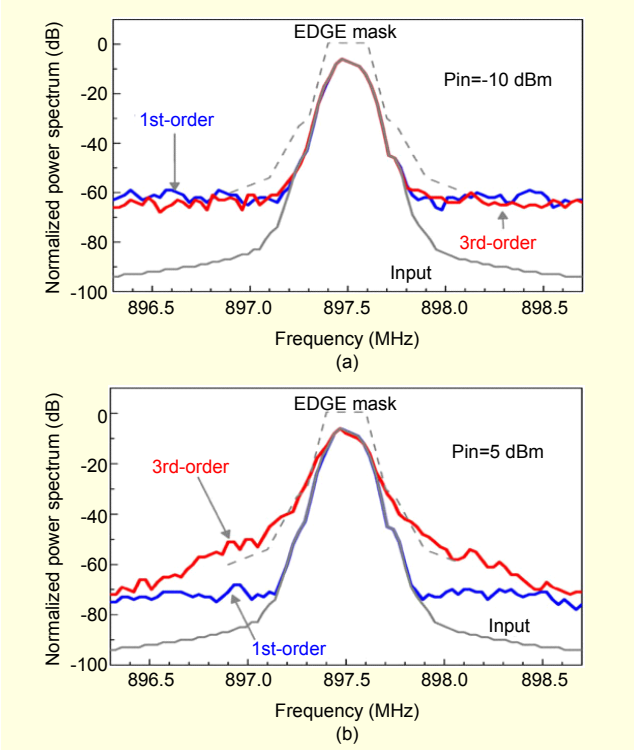


Fig. 2. Output spectra of EER transmitters with first-order and third-order ΣΔ modulators with (a) input power of -10 dBm and (b) input power of 5 dBm.

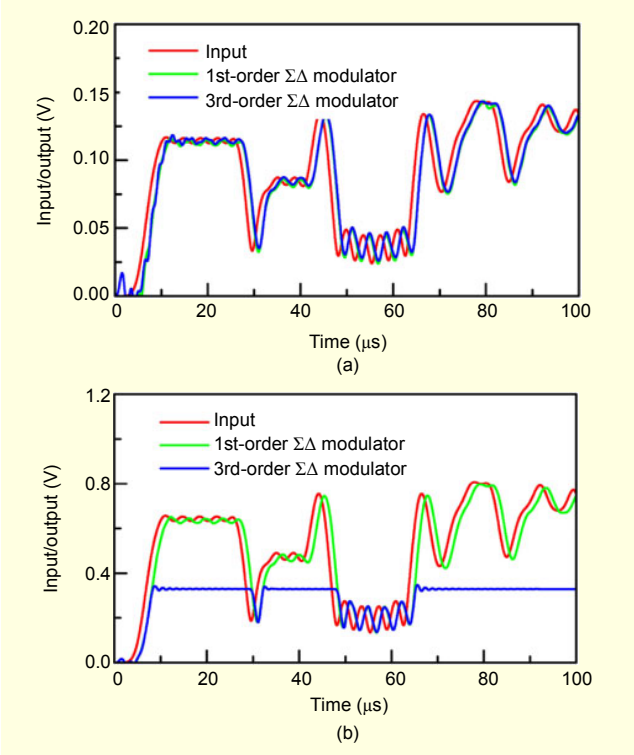


Fig. 3. Time domain waveforms of EER transmitters with first-order and third-order ΣΔ modulators with (a) input power of -10 dBm and (b) input power of 5 dBm.

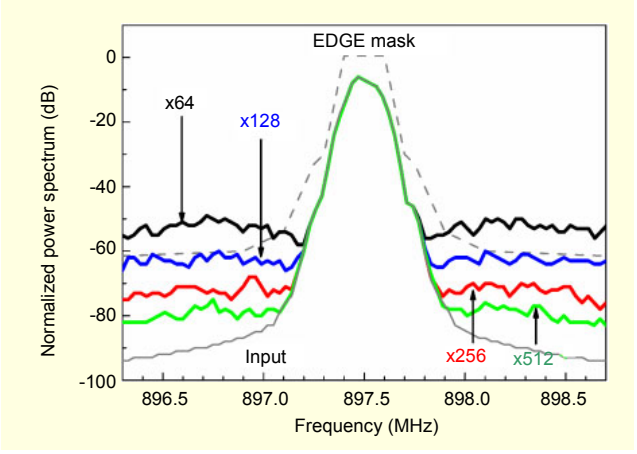


Fig. 4. Output spectra of EER transmitters with different OSRs of ΣΔ modulator.

makes implementation difficult.

The signal quality can be improved by increasing the OSR. Figure 4 shows the signal spectra of the first-order ΣΔ modulator with different OSRs. It shows that the OSR should be at least as high as 256 to satisfy the spectral requirement of the EDGE applications. In the EDGE system, an OSR of 256 corresponds to a clock rate of about 70 MHz. However, a much higher OSR is required in communication systems with high data rates such as WCDMA.

## III. Two-Bit ΣΔ Modulation of Envelope Signal

### 1. Binary Power Amplifier with 2-Bit ΣΔ Modulator

Based on the previous results, we infer that the high-order ΣΔ modulator is not a good solution to choose at the expense of simplicity and system stability. Increasing the OSR is also impractical and ineffective. To resolve these problems, we propose a novel architecture with two unique features: a 2-bit ΣΔ modulator and a binary power amplifier. The 2-bit ΣΔ modulator is a first-order ΣΔ modulator with a four-level quantizer. The basic concept of the structure is to reduce noise by utilizing fine quantization. The four-level output signal is digitally processed by a bit operator to produce 2-bit signals as shown in Fig. 5(b). The bit signals are low-pass filtered and modulated with the phase signal by the combination of two power amplifier cells, which we call the binary power amplifier. The design of the power amplifier cell is crucial for signal restoration. Since the high-bit signal represents high voltage envelope, the power cell output of the high-bit signal should have 3 dB more output power than that of the low-bit signal. The output signals from the two power cells are then combined in the last stage of transmission. Total output power from the two power cells is equal to that from the power amplifier of the conventional structure.

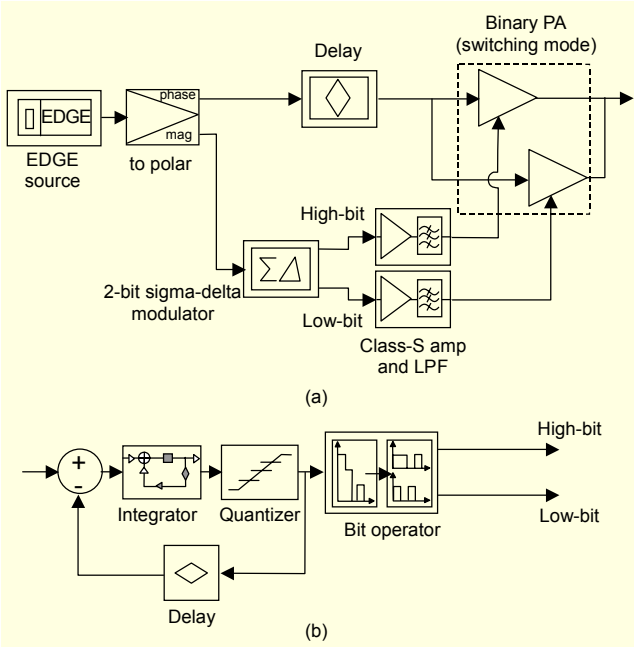


Fig. 5. (a) Proposed transmitter architecture with a binary power amplifier and a 2-bit ΣΔ modulator and (b) 2-bit ΣΔ modulator.

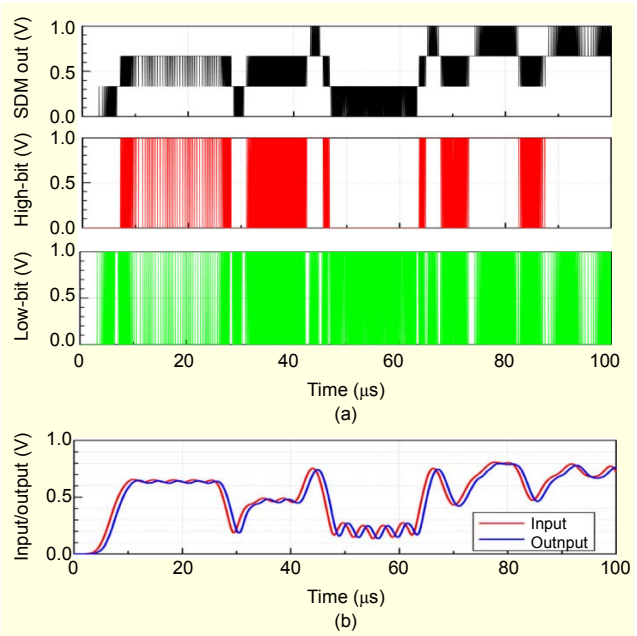


Fig. 6. Time domain signals of the proposed architecture: (a) bit outputs of the ΣΔ modulator and (b) envelope signals of RF input and binary power amplifier output.

## 2. Spectral Property

The operation of the proposed architecture is confirmed by time domain signal waveforms. In Fig. 6, the four-level modulator output signal, high-bit and low-bit waveforms are shown. Figure 6(b) shows the envelope of the output signal, which exactly restores the input EDGE signal.

Figure 7 shows a comparison of the signal spectra of the proposed and conventional structures. Considering the interference between channels, we focus on the noise suppression in the full transmit band of 34.6 MHz from 880.2 to 914.8 MHz as well as in the channel band. The noise of the 128 OSR over-sampled signal of the proposed architecture is almost equal to that of the 256 OSR over-sampled signal of the conventional transmitter. As a result, noise suppression of about 10 dB is achieved without increasing the OSR. The merit of the new architecture is very noticeable in the full transmit band as shown in Fig. 7(b).

## 3. Dynamic Range

In addition to the improvement in the spectral quality, it is worth examining the linear dynamic range. The dynamic range is typically determined by a power amplifier, which often undergoes gain degradation at a low input collector voltage in a switching mode. The binary power amplifier, consisting of the high-bit and low-bit power cells, is compared with the

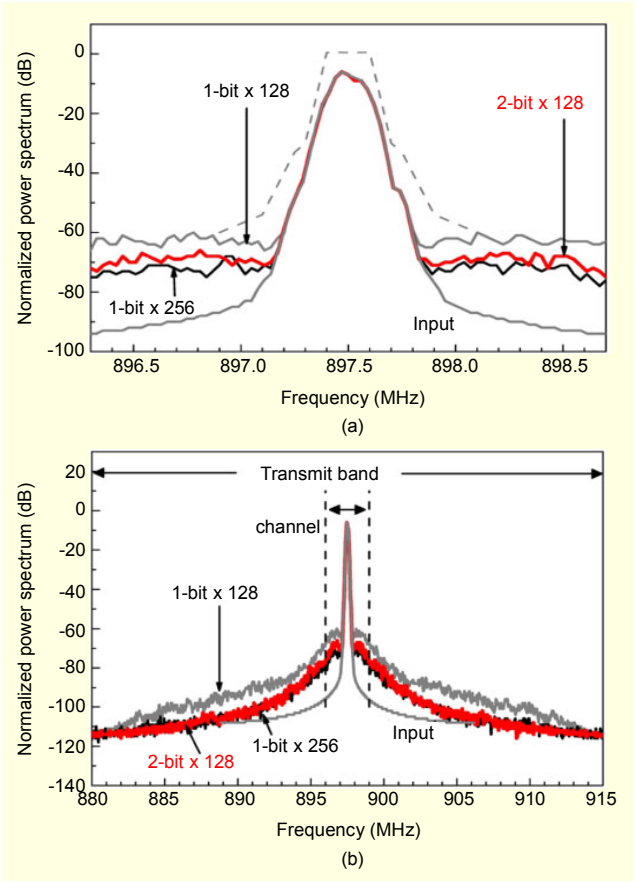


Fig. 7. Output spectra of the proposed and conventional transmitters: (a) output spectra for the channel band and (b) output spectra for the full transmit band.

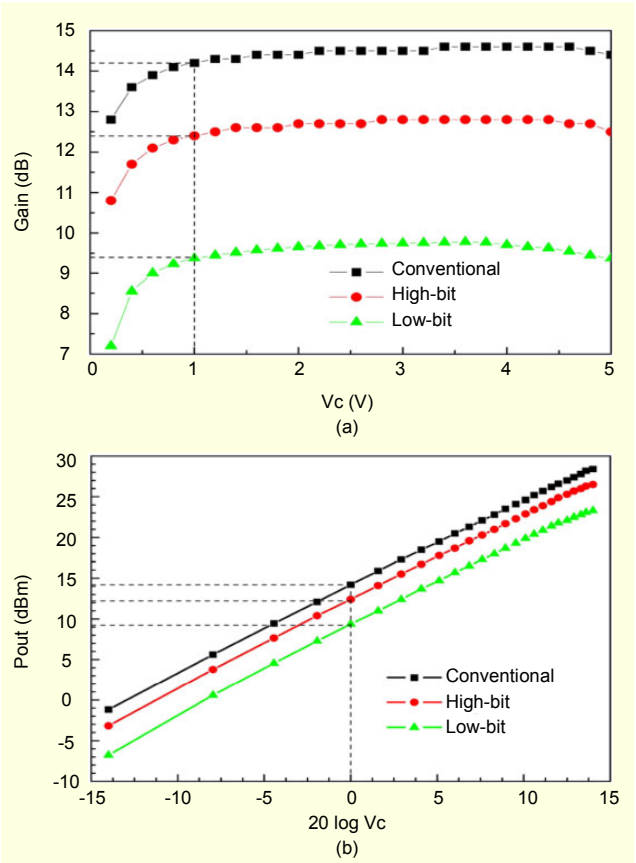


Fig. 8. Gain and output power of class-F power amplifiers with the applied collector voltage: (a) gain characteristic and (b) output power characteristic.

conventional power amplifier through simulations. The power amplifiers are assumed to be class F with a maximum current of 500 mA and a knee voltage of 0.5 V. Total output power of the high-bit and low-bit power cells is chosen to be the same value as the output power of the conventional power amplifier. The output power difference between the high-bit and low-bit power cells is 3 dB according to the principle of operation of the binary power amplifier. Figure 8(a) shows simulation results, in which severe gain compression occurs at a collector voltage lower than 1 V. As shown in Fig. 8(b), the minimum output power without gain suppression is about 5 dB lower in the low-power cell than in the conventional power amplifier. Since only the low-bit cell of the binary power amplifier is used in a low-power operation, the binary power amplifier can handle a lower output power than the conventional power amplifier, without gain suppression. In other words, the lower limit of the dynamic range is enhanced in the proposed architecture. On the contrary, the upper limit of the dynamic range is the same in both cases, because the output powers of the high-bit and low-bit power cells are added in the binary power amplifier.

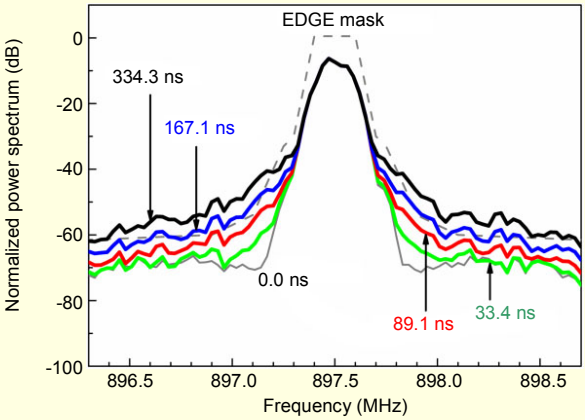


Fig. 9. Output spectra with the envelope signal mismatch. The OSR is 128.

## 4. Synchronization between Power Cells

One more issue to consider is synchronization between power cells because signals with different delays may cause performance degradation. Mismatch occurs at the output of the two power cells, and between the envelope and phase paths. The mismatch at the output of the power cells is not serious for mobile communication systems such as EDGE and W-CDMA because the chip size of the power cells is small enough to ignore the delay at the frequency of operation. Since the phase signal simultaneously drives two power cells integrated on a chip, the delay difference in the envelop signals is a major cause of performance degradation. We simulate the delay mismatch between the envelope signals, assuming that one of them is matched to the phase signal. As shown in Fig. 9, the delay difference of about 89 ns is allowed to satisfy the spectral mask. Such an amount of delay difference between two envelope paths is manageable, since the delay in the envelope path is about 0.4 μsec.

# IV. Conclusion

A novel power amplifier architecture with a 2-bit ΣΔ modulator was proposed to improve the spectral quality of wideband signal. The improvement achieved by the proposed architecture and its feasibility are validated through extensive Agilent ADS Ptolemy simulations. The simulations demonstrated that the new architecture effectively reduces the spectral noise due to the fine quantization of the 2-bit modulation. Noise suppression is improved by about 10 dB in the full transmit band, which can reduce interference between channel bands. In addition, the modified configuration of the power amplifier, that is, the binary power amplifier, enhances the dynamic range by up to 5 dB. Since the improvements are

achieved without an increase in the over-sampling ratio, the proposed architecture is expected to provide a practical solution for mobile communication applications with high data rates.

## References


[1] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Boston, 1999.

[2] L.R. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration," *Proc. IRE*, vol. 40, no. 7, 1952, pp. 803-806.

[3] Y. Wang, "An Improved Kahn Transmitter Architecture Based on Delta-Sigma Modulation," *Proc. IEEE Inter. Microw. Symp.*, vol. 2, 2003, pp. 1327-1330.

[4] A. Dupuy and Y.E. Wang, "A Practical Scheme for Envelope Delta-Sigma Modulated (EDSM) Microwave Power Amplifier," *Microwave and Optical Technology Letters*, vol. 43, no. 6, Dec. 2004, pp. 491-495.

[5] Y. Haung, Y. Wang, and T. Larsen, "Filter Consideration in Polar Transmitters for Multi-mode Wireless Applications," *Proc. IEEE Wireless and Microwave Technology*, 2005, pp. 133-136.

[6] R.B. Staszewski, J.L. Wallberg, S. Rezeq, C. Hung, O.E. Eliezer, S.K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-Digital PLL and Transmitter for Mobile Phones," *IEEE J. of Solid-State Circuits*, vol. 40, no. 12, Dec. 2005, pp. 2469-2482.

[7] L. Breems and J.H. Huijsing, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*, Kluwer Academic Publishers, Boston, 2001.

[8] T. Ritoniemi, T. Karema, and H. Tenhunen, "Design of Stable High Order 1-bit Sigma-Delta Modulators," *Proc. IEEE Int. Symp. Circuits and Systems*, 1990, pp. 3267-3270.

[9 J.C. Candy and G.C. Temes, *Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, New York, 1992.


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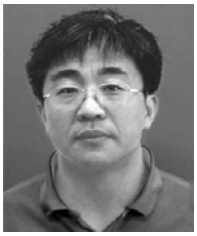

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