Characterization of an Oxidized Porous Silicon Layer by Complex Process Using RTO and the Fabrication of CPW-Type Stubs on an OPSL for RF Application

Jeong-Yong Park and Jong-Hyun Lee

This paper proposes a 10-μm thick oxide layer structure that can be used as a substrate for RF circuits. The structure has been fabricated using an anodic reaction and complex oxidation, which is a combined process of low-temperature thermal oxidation (500 °C, for 1 hr at H_2O/O_2) and a rapid thermal oxidation (RTO) process (1050 °C, for 1 min). The electrical characteristics of the oxidized porous silicon layer (OPSL) were almost the same as those of standard thermal silicon dioxide. The leakage current density through the OPSL of 10 μm was about 10 to 50 nA/cm^2 in the range of 0 to 50 V. The average value of the breakdown field was about 3.9 MV/cm. From the X-ray photo-electron spectroscopy (XPS) analysis, surface and internal oxide films of OPSL prepared by a complex process were confirmed to be completely oxidized. The role of the RTO process was also important for the densification of the porous silicon layer (PSL) oxidized at a lower temperature. The measured working frequency of the coplanar waveguide (CPW) type short stub on an OPSL prepared by the complex oxidation process was 27.5 GHz, and the return loss was 4.2 dB, similar to that of the CPW-type short stub on an OPSL prepared at a temperature of 1050 °C (1 hr at H_2O/O_2). Also, the measured working frequency of the CPW-type open stub on an OPSL prepared by the complex oxidation process was 30.5 GHz, and the return was 15 dB at midband, similar to that of the CPW-type open stub on an OPSL prepared at a temperature of 1050 °C (1 hr at H_2O/O_2).

Keywords: Porous silicon, RTO, stub.

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I. Introduction

Gallium arsenide (GaAs) is a major substrate material for monolithic RF and microwave circuits in virtue of its semi-insulating characteristics and high mobility value. However, GaAs real estate is expensive, particularly when passive circuit elements occupy large areas such as filters, diplexers, antennas, and so on. Therefore, a number of alternative substrates can be considered for a planar millimeter-wave circuit or interconnect design. While GaAs offers a low dielectric constant and compatibility with the metal semiconductor field-effect transistor and the high electron-mobility transistor active device technology, large area GaAs substrates with a low defect density are costly to produce. Although silicon is inexpensive, is a very mature technology, and has a high thermal conductivity, it has not been widely used as a microwave substrate because of its extremely high dielectric loss [1], [2]. The thick oxidized film and the micromachined oxide bridge were each reported to overcome the problem of the high dielectric loss of a low-resistivity silicon substrate [3], [4]. In a conventional process, however, it is difficult to grow thick oxide films in a short time and in low temperature. In order to use Si for monolithic microwave integrated circuit application, we prepared an oxidized porous silicon layer (OPSL) on a silicon substrate by using a complex oxidation process (COP) in which the thickness of the porous silicon layer could be controlled by an anodic reaction [5]. Oxide films were obtained by combining low temperature thermal oxidation (500 °C, 1 hr at H_2O/O_2) and rapid thermal oxidation (RTO) processes (1050 °C, 1 min) [6]-[9]. We investigated the material and electrical characteristics of an OPSL fabricated by anodic reaction and

the COP, and compared them with those of conventional silicon dioxide prepared at a higher temperature [10], [11]. For the RF test of a Si substrate with a thick silicon dioxide layer, we have fabricated high performance passive devices such as a coplanar waveguide (CPW) type short/open shunt stub on an OPSL substrate [10]-[12]. Also, we investigated the working frequency and return loss characteristics of a CPW-type short/open stub fabricated on an OPSL prepared by the COP, and compared them with those of a standard CPW-type short/open stub fabricated on an OPSL prepared at a high temperature.

II. Experimental

A detailed sequence for the fabrication of an OPSL is shown in Fig. 1. The starting material was a <100> p-type boron-doped silicon substrate with a 0.8- to 1.2-Ωcm resistivity. The backside of the wafer was ion implanted (100 keV, $5.0 \times 10^{15}/cm^2$) and the implant driven in to insure an ohmic contact from the secondary electrode to the wafer. 0.15-μm aluminum was deposited as the back-side ohmic contact to provide a uniform current density during the anodic reaction process, as shown in Fig. 1(a). Figure 1(b) shows that the PSL was obtained using an anodic reaction. We carried out the anodization process for 10 minutes at room temperature at 20 mA/cm^2 in 43 wt% HF (49 wt%HF : C_2H_5OH = 8:1). The growth rate of the PSL was 1.4 μm/min. We etched away the aluminum after the anodic reaction process and then removed the remaining material in the PSL into a vacuum chamber. The PSL was preoxidized at 500 °C under the atmospheric pressure of wet oxygen for 1 hour. Low oxidation temperatures were then needed to terminate the dangling silicon bonds with oxygen without an agglomeration of the silicon columns. We densified the preoxidized PSL using

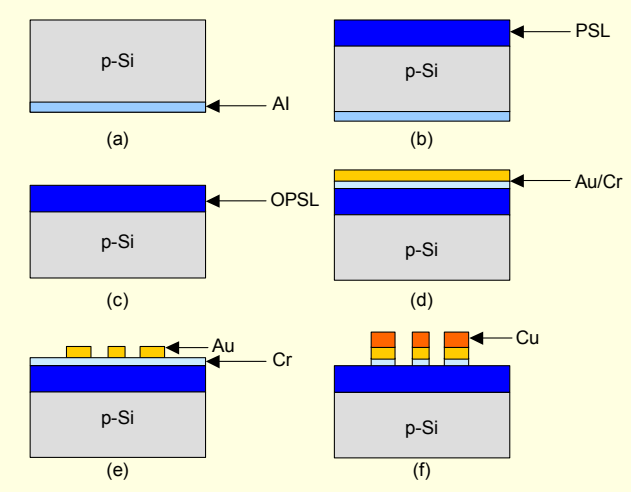

Fig. 1. Sequence of the fabricated structures.

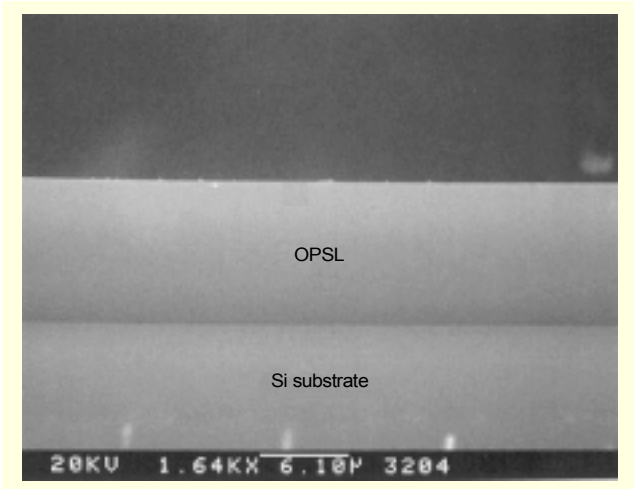

Fig. 2. Cross-sectional SEM image of OPSL surface with newly developed oxidation process.

an RTO process for 1 or 2 minutes at 1050 °C, as shown in Fig. 1(c). Figure 1(d) shows that we deposited 0.25-μm Cr/Au as a metal line on the OPSL using an evaporator. To form the metal pattern, we etched the metal (Au) on the OPSL using a metal etchant, as shown in Fig. 1(e). To reduce the serial resistance, we electroplated the metal line with copper to a total thickness of 2.5 μm and etched away the metal (Cr) after the electroplating, which can be seen in Fig. 1(f).

The resulting material has a porosity of 56 % (determined gravimetrically) and a thickness of approximately 10 μm (determined using the scanning electron micrograph shown in Fig. 2) [5]. We observed the cross section of the OPSL using scanning electron microscopy and analyzed its oxidation characteristics using a Fourier Transform Infrared Resonance (FTIR) spectra (Mattson Galaxy-7020A). The electrical characteristics of the OPSL were investigated using a breakdown field (Sony Tektronix 370A) and leakage current (HP4145) measurements. We measured the surface and internal compositions of the OPSL using X-ray photo-electron spectroscopy (XPS), Fison's System ESCALLAB 200i, with a monochromatic Mg-K source (1253.6 eV energy).

III. Results and Discussion

Figure 3 shows the FTIR spectra of the OPSL as oxidized temperature over time. As shown in Fig. 3, we observed Si-O peaks located at around 1100 cm^{-1}, 805 cm^{-1}, and 450 cm^{-1} and O-H peaks located at around 3500 cm^{-1} and 1600 cm^{-1}. Figure 4 shows the FTIR spectra of the OPSL using an RTO process. As compared with Fig. 3, we know that the O-H peaks located at around 3500 cm^{-1} and 1600 cm^{-1} disappeared completely; this RTO process contributed mainly to the densification of the PSL oxidized at low temperature. Figure 5 shows the breakdown

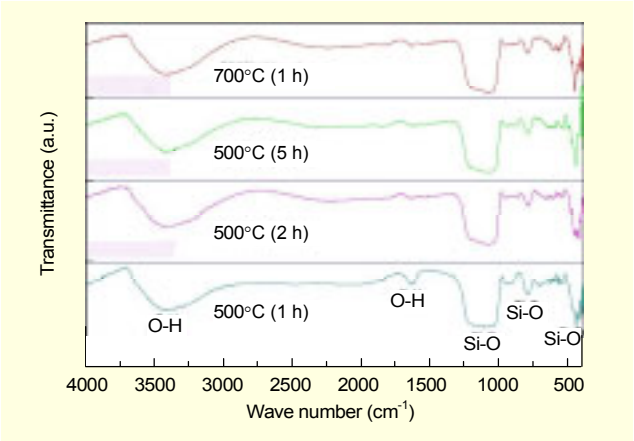

Fig. 3. IR absorption spectra of a low temperature oxidized PSL.

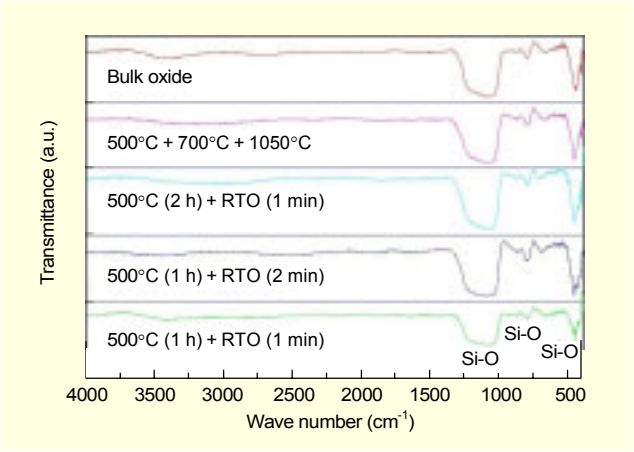

Fig. 4. IR spectra after RTO process.

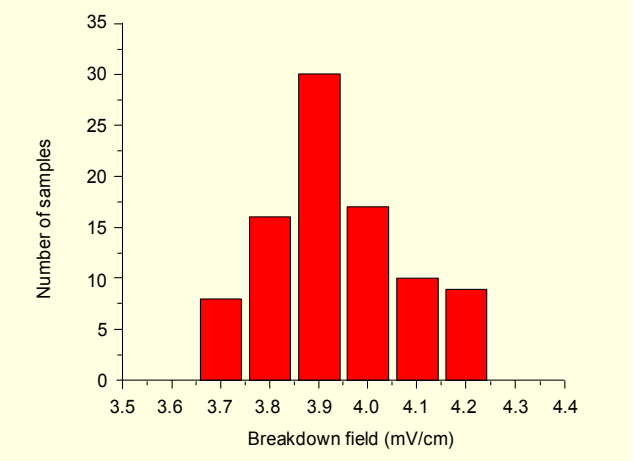

Fig. 5. Breakdown field of a fabricated OPSL.

field of the fabricated capacitor on the OPSL. The capacitor's diameter used for the measurement was 0.3 mm. The values of the breakdown field ranged from 3.7 mV/cm to 4.2 mV/cm, and the average value was about 3.9 mV/cm. These breakdown values of the OPSL were almost the same (4.0 mV/cm) as those of an OPSL prepared at a higher temperature. Figure 6 plots the leakage current density of the OPSL oxidized at 500 °C for 1 hour. When the applied voltage is between 0 and 50 V, the measured leakage current density falls between 59.8 nA/cm^2 to 239 μA/cm^2. If an RTO process is added, the measured leakage current density in the same voltage range lowers to 2.99 nA/cm^2 to 15.1 nA/cm^2 as shown in Fig. 6(b). From these results, we know that the RTO process improves the insulating characteristic of OPSL films. For the surface and internal composition of an OPSL, we performed an XPS analysis. We first prepared 2-μm thick thermal bulk oxide films before comparing the oxidation characteristics of a 10-μm thick OPSL. Figure 7 shows a comparison between the oxidation characteristics of bulk oxide films and those of the OPSL. In the case of bulk oxide films, the Si-2p peak is 105.1 eV and the O-1s peak is 534.8 eV. In the case of the OPSL, the Si-2p peak oxidized at 500 °C is 106.1 eV and the peak oxidized in the added RTO process at 500 °C is 105.2 eV. From these results, the Si-2p peak moved by about -0.9 eV. Also, the O-1s peak oxidized at 500 °C is 535.7 eV and the peak oxidized in the added RTO process at 500 °C is 534.8 eV. This also moved about -0.9 eV. Considering these results, we also know that the peak of the OPSL is closer to the peak of the bulk oxide with the addition of the RTO process than it is to the bulk oxide without this addition. Accordingly, we can identify that the RTO process contributed to the oxidation process of the OPSL. From the XPS results of the surface analysis, we know that the surface of the OPSL oxidized completely. However, we were unable to determine the internal oxidized state of the OPSL oxidized using the complex process. We performed a surface analysis of the OPSL with respect to depth using XPS, which is shown in Fig. 8. Figure 8(a) shows that the silicon binding energies of the OPSL—104.9 eV at the surface, 105.2 eV at a 5-μm depth, and 105.2 eV at a 9-μm depth—are almost the same as that of the bulk oxide film with a peak of 105.0 eV. Figure 8(b) also shows that the oxygen binding energies of the

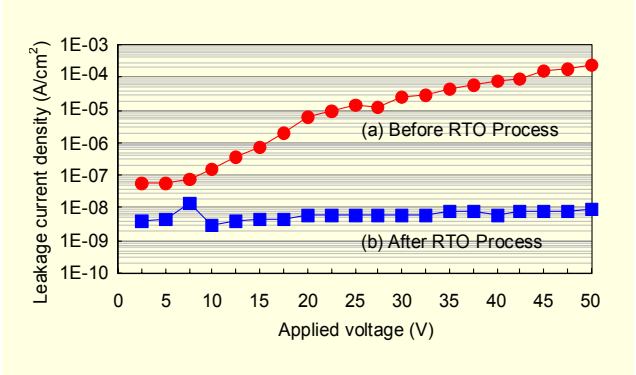

Fig. 6. Leakage current density of an OPSL.

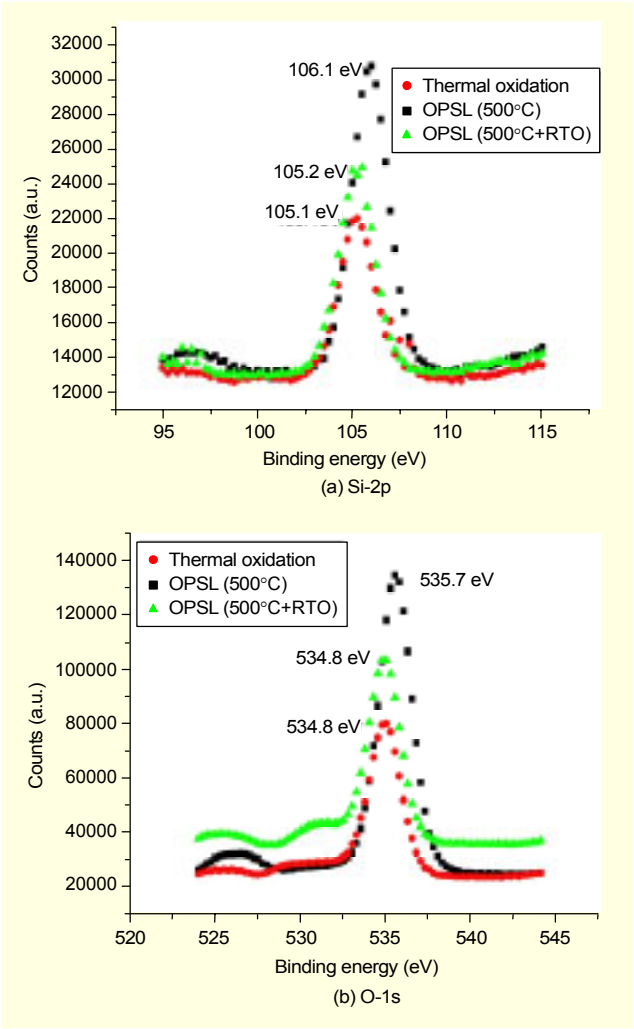

Fig. 7. XPS analysis of an OPSL.

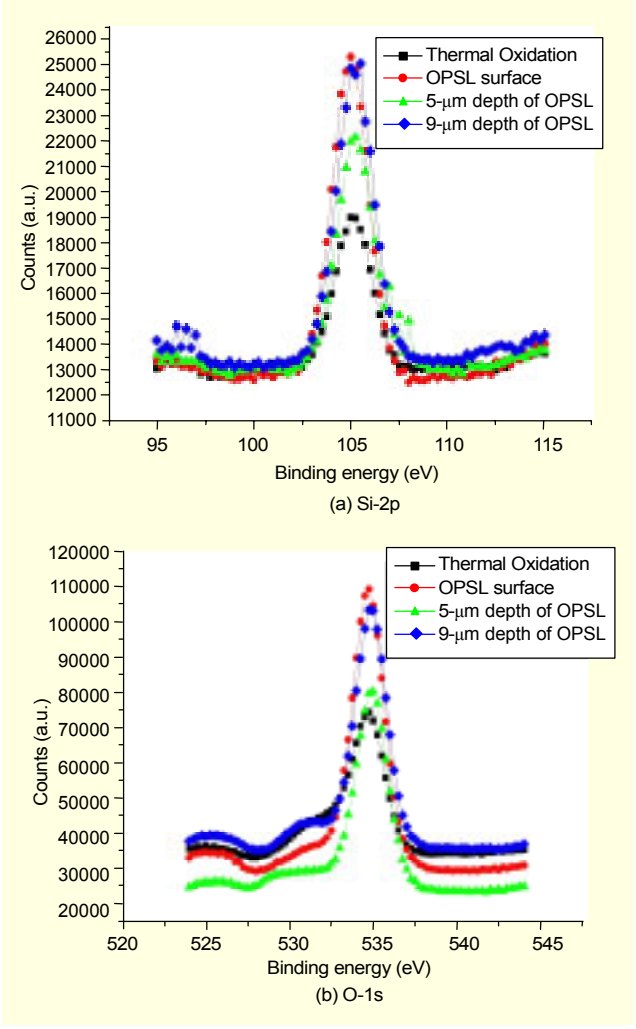

Fig. 8. XPS analysis of an OPSL with respect to depth.

OPSL—534.1 eV at the surface, 534.4 eV at the 5-μm depth, and 534.4 eV at the 9-μm depth —are almost the same as that of the bulk oxide film with a peak of 534.2 eV. Accordingly, we can confirm that the inner part of the OPSL was oxidized.

Figure 9 shows the structure of a CPW-type short/open stub including the important parameters that determine the characteristic impedance and propagation modes. Table 1 indicates the parameter values of a fabricated CPW-type short/open stub. A tilted view of the fabricated CPW-type short/open stub on an OPSL is shown in Fig. 10. The S-parameter measurements were carried out using an HP8510b network analyzer (frequency range of 45 MHz to 40 GHz) and a Cascade Microtech probe (up to 50 GHz). Figure 11 shows the S-parameter of a CPW-type short stub on an OPSL with 10 μm; the return loss calculation equation is -20 log$|S_{11}|$ [8]-[10]. The measured working frequency of a short stub on the OPSL prepared by a complex oxidation process was 27.5 GHz, and the return loss was 4.2 dB, similar to that of a short stub on an

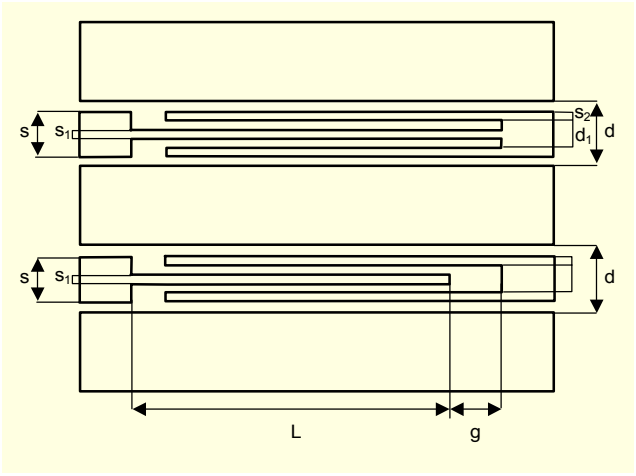

Fig. 9. Parameter of CPW series and shunt stub.

OPSL prepared using a temperature of 1050 °C (1 hr at H_2O/O_2). Figure 12 shows the S-parameter of a CPW-type

Table 1. Parameter values of a CPW-type short/open stub.

Structure / Parameter	Stort stub (μm)	Open stub (μm)
s	140	140
s1	40	40
s2	30	30
g	–	200
d	200	200
d1	80	80
L	1600	1400

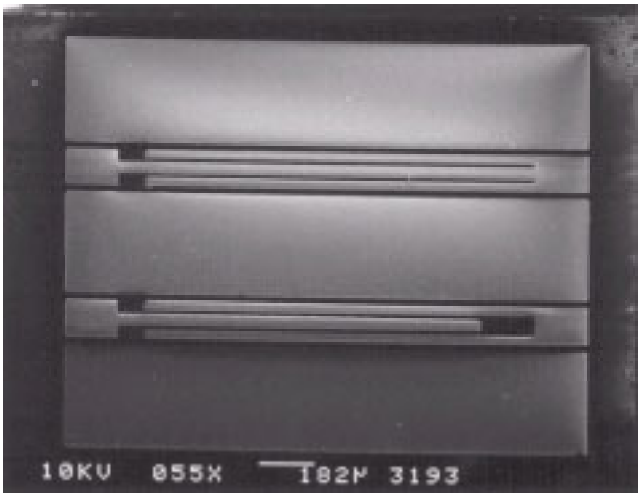

Fig. 10. An SEM image of a fabricated CPW series and short/open on an OPSL.

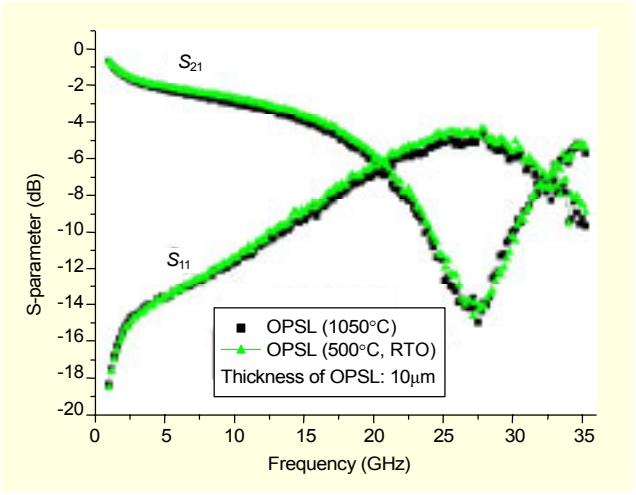

Fig. 11. S-parameter of a short stub on an OPSL as a function of frequency.

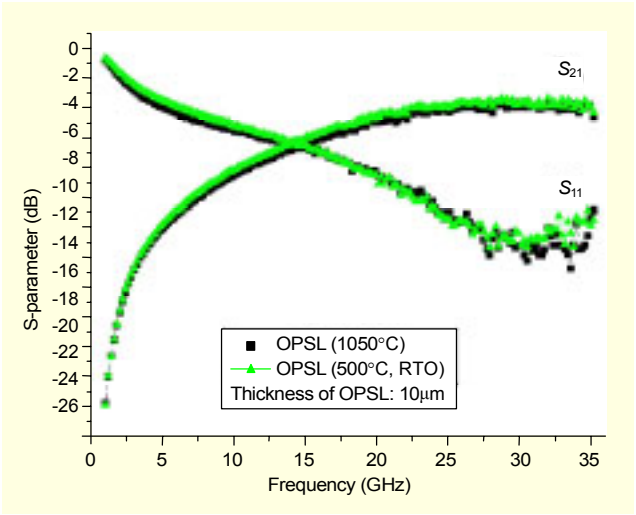

Fig. 12. S-parameter of an open stub on an OPSL as a function of frequency.

open stub on a 10-μm OPSL. The measured working frequency of an open stub on the OPSL prepared using a complex oxidation process was 30.5 GHz, and the return loss was 15 dB at midband, similar to that of an open stub on an OPSL prepared using a temperature of 1050 °C (1 hr at H_2O/O_2).

IV. Conclusion

We successfully formed thick oxide films using an anodic reaction and complex oxidation at 500 °C for 1 hr at H_2O/O_2, accompanied by an RTO process at 1050 °C for 1 min. The electrical characteristics of an OPSL oxidized by a complex process were almost the same as those of thermal silicon dioxide prepared at a higher temperature. Also, the measured working frequency of a CPW-type short/open stub fabricated on an OPSL oxidized by a complex process were almost the same as those of a CPW-type short/open stub fabricated on thermal silicon dioxide prepared at a higher temperature. The importance of the RTO process was mainly due to the densification of the PSL oxidized at a lower temperature. This proposed method can therefore be useful in extending the use of CMOS circuitry to higher RF frequency bands.

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