SANDIA REPORT
SAND2007-6856
Unlimited Release
Printed November 2007

Stable Local Oscillator Module

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Prepared by
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Stable Local Oscillator Module

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Abstract:
This report gives a description of the development of a Stable Local Oscillator (StaLO) multi-chip module (MCM). It is a follow-on report to SAND2006-6414, Stable Local Oscillator Microcircuit. The StaLO accepts a 100MHz input signal and produces output signals at 1.2, 3.3, and 3.6 GHz. The circuit is built as a multi-chip module (MCM), since it makes use of integrated circuit technologies in silicon and lithium niobate as well as discrete passive components. This report describes the development of an MCM-based version of the complete StaLO, fabricated on an alumina thick film hybrid substrate.

Contents

Nomenclature

ADS	-	Agilent Corporation's Advanced Design System software
ASIC	-	Application Specific Integrated Circuit
CMOS	-	Complementary metal oxide semiconductor
COTs	-	Commercial off-the-shelf component
dBm	-	Decibels relative to one milliwatt
DC	-	Direct current
FY	-	Fiscal Year
GSG	-	Ground-signal-ground probe type
GSSG	-	Ground-signal-signal-ground probe type
GHz	-	Giga Hertz (billion cycles/sec)
HP	-	Hewlett Packard Corporation
IBM	-	International Business Machines Corporation
IC	-	Integrated circuit
IDT	-	Interdigital Transducer
IF	-	Intermediate Frequency
IL	-	Insertion loss
ISM	-	Instrumentation, Scientific, and Medical frequency band
LDRD	-	Lab Directed Research and Development
LNA	-	Low Noise Amplifier
MCM	-	Multi-chip module
MHz	-	Mega Hertz (million cycles/sec)
Mm	-	Milli-meters
NPN	-	A type of bipolar transistor
PCB	-	Printed Circuit Board
PMMA	-	Polymethylmethacrylate
PTC	-	Positive temperature coefficient
RF	-	Radio Frequency
SAW	-	Surface Acoustic Wave
SiGe	-	Silicon germanium technology
SFDR	-	Spur free dynamic range
SMA	-	Subminiature type 'A' connector
Slice	-	Frequency specific section of the StaLO at 1.2, 3.3, or 3.6 GHz
StaLO	-	Stable local oscillator

Introduction

This report describes the development of the Stable Local Oscillator (StaLO) multi-chip module (MCM). The StaLO is a circuit that produces low phase-noise oscillator outputs at 1.2, 3.3, and 3.6GHz from a 100MHz reference oscillator input. The StaLO module uses a combination of technologies, all of which had to be developed as completely custom elements.

The StaLO module is based on the concept of a comb generator. A comb generator uses a time periodic sequence of delta-function-like pulses to produce a frequency domain periodic sequence of delta-function-like components. The input reference oscillator is used to produce the time domain pulse train. A series of amplifiers and filters then successively amplify and select the desired frequency components. This is explained in more detail in the Overview section.

The StaLO is assembled using two different integrated circuit technologies and a multi-chip module packaging technology. The comb generator exists in the form of a custom silicon germanium (SiGe) integrated circuit (IC). The chip was designed by the author and produced at IBM using the 0.18µm 7WL SiGe process. The design details of this chip are discussed in a previous report, SAND2006-6414, Stable Local Oscillator Microcircuit. The filters to perform frequency component selection are custom surface acoustic wave (SAW) devices fabricated on lithium niobate or quartz. Details about the SAW filters are briefly reviewed in the SAW Filters section. The amplifiers are also SiGe circuits designed and fabricated in the IBM 7WL process. Amplifier development and testing is also covered in the report SAND2006-6414. All of these different components have been integrated on a single alumina substrate specifically designed for the purpose.

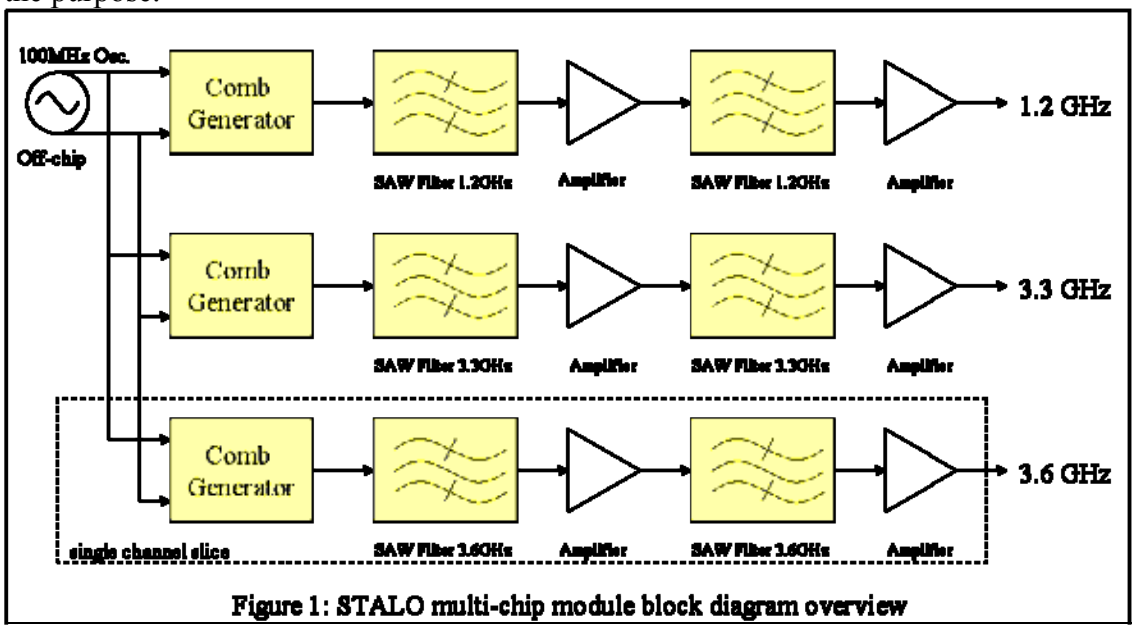

Figure 1: STALO multi-chip module block diagram overview

Overview

A block diagram of the complete StaLO is shown in figure 1. It consists of three mostly identical channels, referred to as "slices", to handle the three different frequency outputs

of the StaLO. Each slice differs primarily in the center frequency of its SAW filters. It is possible to expand the StaLO to produce different frequency outputs merely by adding additional slices.

A block diagram of the 3.6 GHz channel slice is shown in figure 2. It consists of a comb generator with an integrated differential amplifier, two SAW filters, and two amplifiers. The comb generator accepts a 100 MHz signal with an arbitrary wave shape, here assumed to be a sinusoid. It then conditions the signal into a delta function pulse train with a 10 nsec repetition rate. A delta function pulse train in the time domain transforms into a delta function train in the frequency domain when a Fourier transform is applied to the train. A comb function in the time domain can be described by the following equation

$$comb\left[t/T\right] = \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{1}$$

which describes a series of delta functions, each separated by a time interval, T. The Fourier transform of the comb function is

$$F\left\{comb\left[t/T\right]\right\} = T \cdot comb[T \cdot f] \tag{2}$$

indicating that the comb in the time domain produces a comb in the frequency domain with components separated by (1/T). This implies that an input pulse train, generated from a 100 MHz wave, will have a frequency domain spectrum consisting of discrete components separated by 100 MHz.

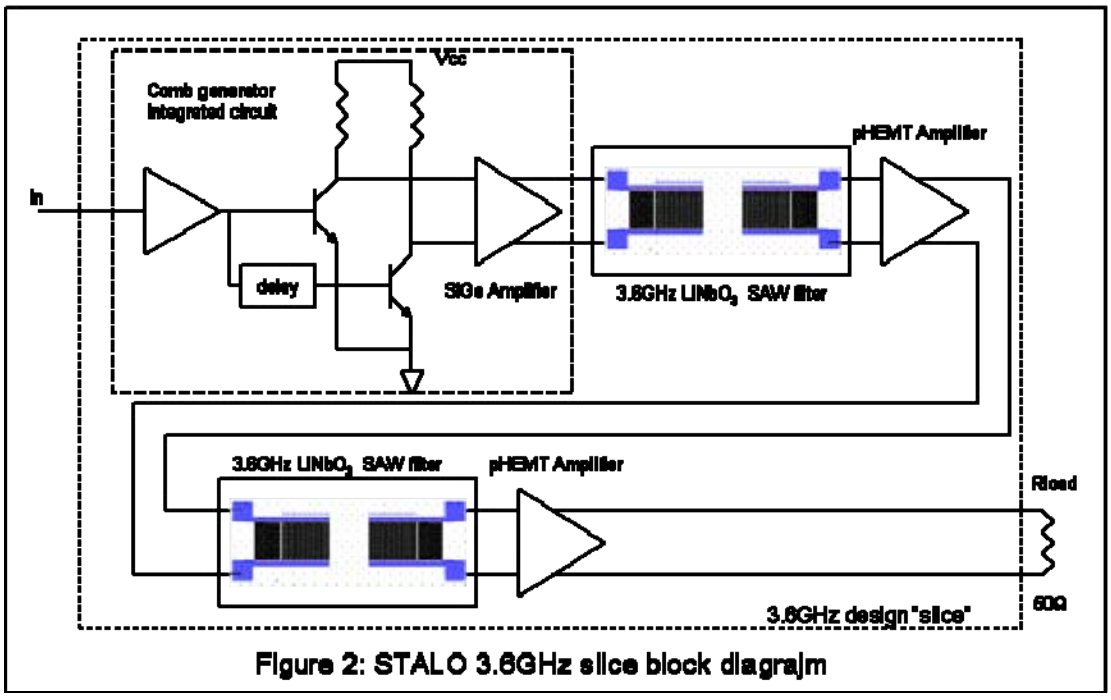

Figure 2: STALO 3.6GHz slice block diagram

These relations hold exactly for perfect delta functions. However, variations from a perfect delta function in the time domain lead to variations in the frequency domain. For

example, if the time domain delta function has a finite rise-time, the maximum bandwidth of the comb function in the frequency domain will be limited.

For the transform operation from time to frequency domain, Parseval's theorem applies. Parseval's theorem states that the energy contained in the signal in the time domain is equal to the energy contained in the signal in the frequency domain. It can be written as

$$\int_{-\infty}^{\infty} |x(t)|^2 \, dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |X(f)|^2 \, df \tag{3}$$

where x(t) is the time domain signal and X(f) is the Fourier transform of that signal. This theorem implies that amplitude limitations in the time domain will limit the amount of power in each spectral component in the frequency domain. For a circuit without inductors, the output amplitude is limited by the power supply voltage. To maximize StaLO output power, it is necessary to obtain output pulses from the comb generator circuit with voltage amplitudes that are as close as possible to the rail voltage. To put as much power as possible into the high order harmonics, the rise and fall times of the pulses need to be as short as possible. The harmonics generated by these pulses are then selected by the SAW filters.

SAW Filters

SAW filter development was discussed in the previous report, SAND2006-6414. However, SAW development and refinement continues to be pertinent to both the effort described in this report and any potential future developments. The current SAWs used in the StaLO are made from Y-Z cut lithium niobate. These devices will exhibit a temperature induced frequency variation of 94 ppm/^{o}C [1]. It is recognized that this variation will not enable the current StaLO design to meet its temperature range specifications. To overcome this shortcoming, the StaLO substrate has been designed to incorporate quartz versions of these SAW filters. SAW filters made from ST-cut quartz possess a zero temperature coefficient at room temperature. The quartz SAW filters will be considerably longer than the lithium niobate filters due to differences in material coupling coefficient and acoustic velocity.

The design and processing procedures for producing the SAW filters are highly specialized. Sandia uses a process that is designed to give the highest performance possible in terms of insertion loss and center frequency accuracy. This process is optimized for small scale production only, and the procedure described here is in all likelihood unique in the SAW fabrication business. Each one-by-one inch wafer produced via the Sandia process contains 140 blocks with 1 each, 1.2 GHz SAW and 2 each, 3.3 GHz and 3.6 GHz SAWs. The Sandia process is suitable to small scale production.

There are three SAW parameters that need to be simultaneously optimized during the design and fabrication of the filters used for the StaLO. These are insertion loss, sideband attenuation, and center frequency. The insertion loss is the S_{21} wave attenuation from input to output. It is minimized in order to maximize StaLO output power. It is also a function of the substrate material coupling coefficient, the straightness and line-

edge roughness of the transducer fingers, and the number of finger pairs in the electrical to acoustic transducers.

The center frequency of the SAW filter is a coarse function of the transducer finger spacing, or pitch. Because the minimum metal width of the 3.6 GHz filters is only 80nm, a change of 1 nm in metal width will change the frequency by 1.25%, or about 45 MHz. For our purposes, the StaLO needs to be tuned to within 3 MHz of its design frequency, so mask design alone is unable to provide sufficient precision for the final filter center frequency. The goal of the design of the SAW filter mask is to put the SAW's center frequency as close as possible to but below the desired center frequency. The reason why the SAW filter is designed with a center frequency below its desired frequency is due to the effect of metal loading. The weight of the transducer metal on the surface of the SAW slows the surface wave slightly and lowers its output frequency below the design frequency. By removing some of the metal thickness through etching, the SAW output frequency can be raised to exactly its design frequency. The etching process is like a fine tune dial on a radio receiver. It doesn't give much range of control, but it does provide for a very fine selection of the final frequency.

The SAW lithography is created by generating one optical mask for gold pads and bus-bars and a series of data files for patterning the aluminum fingers. The SAWs are fabricated using a combination of electron beam (e-beam) machine and optical lithographic patterning. First, a one-by-one inch wafer of the desired substrate material in the correct crystallographic orientation is prepared with a coating of e-beam photoresist, polymethylmethacrylate or PMMA (figure 3). The photoresist is then exposed in the e-beam machine using a series of carefully selected dosages geared to the different mask data types in the physical design. The exposed photoresist is processed by dissolving only the exposed portions of the wafer. After this step, a thin layer of aluminum (500Å) is deposited over the processed photoresist (figure 4). The aluminum fingers and bus-bars sit directly on the piezoelectric substrate, while the excess aluminum sits on top of the unexposed photoresist. The aluminum fingers and bus-bars are then removed using a lift-off process to dissolve the unexposed photoresist and remove the aluminum from the wafer field.

The pads and heavy bus-bars are formed next (figure 5). First, a layer of optical photoresist is deposited over the entire wafer, patterned using an optical mask, and developed to expose holes for the pads and bus-bars. A 150Å layer of aluminum is deposited and then a thick 5000Å layer of gold is deposited on top. The combined layers are patterned using a lift-off procedure of the optical photoresist. At this point the SAW is ready for frequency testing and etch adjusting of frequency, if necessary.

After the final etch, the SAW is ready for mounting and wire-bonding. The SAW is typically attached using a non-conductive epoxy with low out-gassing properties. This is required to prevent the surface of the SAW from being contaminated. Electrical connections are then made to the SAW using 3-mil gold ribbon wire that is thermo-sonically bonded.

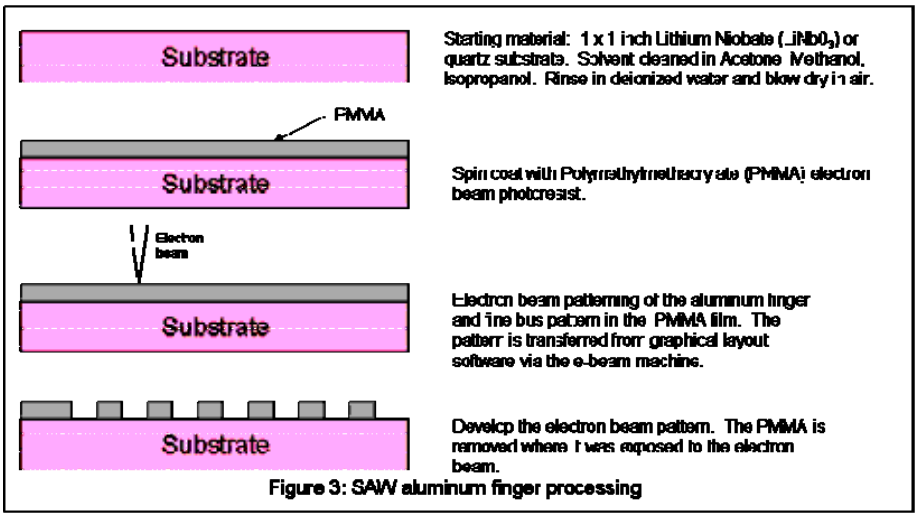

Figure 3: SAW aluminum finger processing

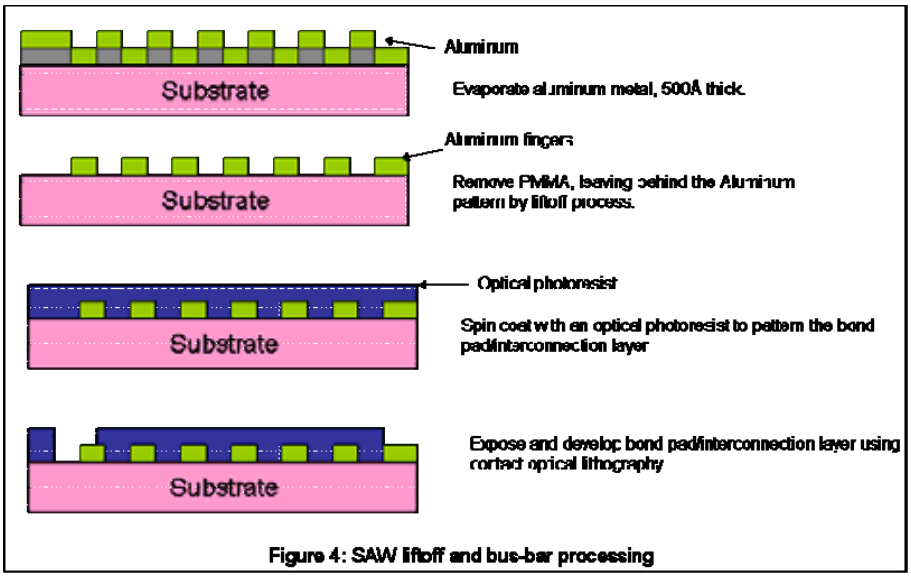

Figure 4: SAW liftoff and bus-bar processing

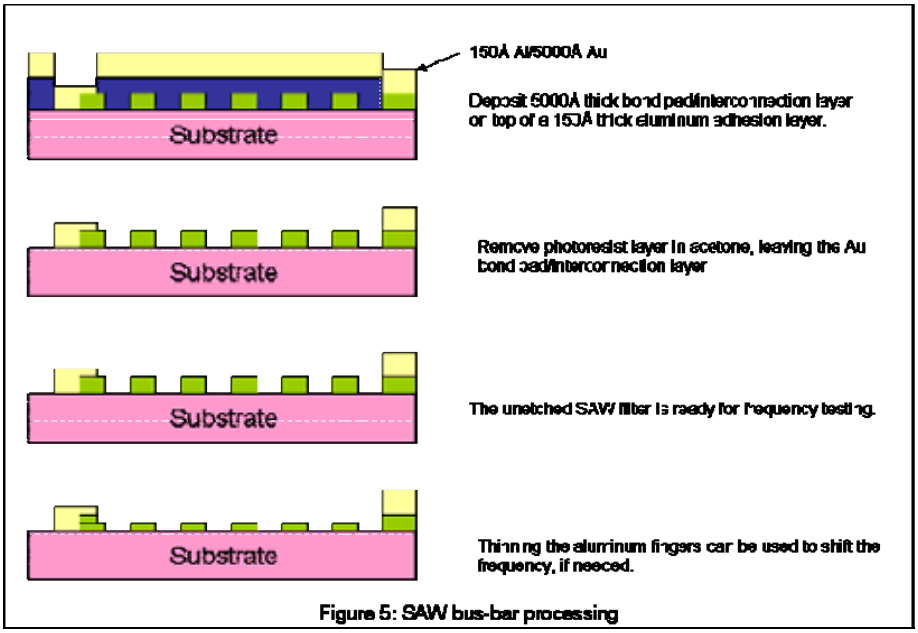

Figure 5: SAW bus-bar processing

Amplifiers

The amplifiers used in the StaLO slice are custom designed SiGe-based differential circuits. The amplifiers are differential rather than single-ended to mitigate problems with ground or power rail referencing, since a differential signal provides a relative, rather than an absolute reference. This approach is made simpler by the differential design of the SAW. All SAW filters are built on an insulating substrate and are intrinsically differential devices. They can serve as either a single-ended or a differential device or as a balun transformer between a single-ended device on one end and a differential device on the other.

The StaLO amplifier uses an emitter-coupled pair with a simple input matching circuit (figure 6). The complete amplifier consists of the emitter-coupled pair, dual input matching circuits, dual bias circuits, a tail-current source, and power supply bypassing filters. The amplifier is designed using a standard-sized SiGe bipolar NPN transistor. This standard sized transistor is a device that IBM gives detailed performance data for, and, more importantly, it is a device that we collected transistor model parameters for via direct measurements conducted at Sandia.

Multiple versions of this standard-sized transistor are used in the emitter-coupled pair to increase total collector current and transconductance (g_m). This is accomplished while still using a device with trusted model parameters. The input to the differential pair is matched using a series inductor-capacitor tank circuit. The tank provides a good match at both 3.3 and 3.6 GHz. At 1.2 GHz, the amplifier has excessive gain, and the gain detuning provided by the matching network lowers the gain and improves circuit stability. Amplifier gain versus frequency is shown in figure 7.

The amplifier shown in figure 6 is a modification of an earlier design fabricated at IBM. As was discussed in SAND2006-6414, the original amplifier design did not perform in accordance with simulation results, since IBM SiGe transistor performance was below advertised levels. The earlier amplifier version used single 0.48 x 20 μm transistors where doubled devices are shown in figure 6. It also used no input matching networks on the two inputs. The overall amplifier performance for a single differential stage is shown in figure 8 as measured data versus the simulation using extracted parameters. Note that the gain for a single differential amplifier at 3.6 GHz is only 2-3 dB – rather low. The amplifiers are used in blocks of three, so that each block possesses a gain of 6-9 dB at the maximum StaLO frequency of 3.6 GHz. A better approach would have been for IBM to produce transistors that came closer to their stated performance. Nonetheless, adequate performance was obtained using the low gain differential amplifiers, as will be described in the next section.

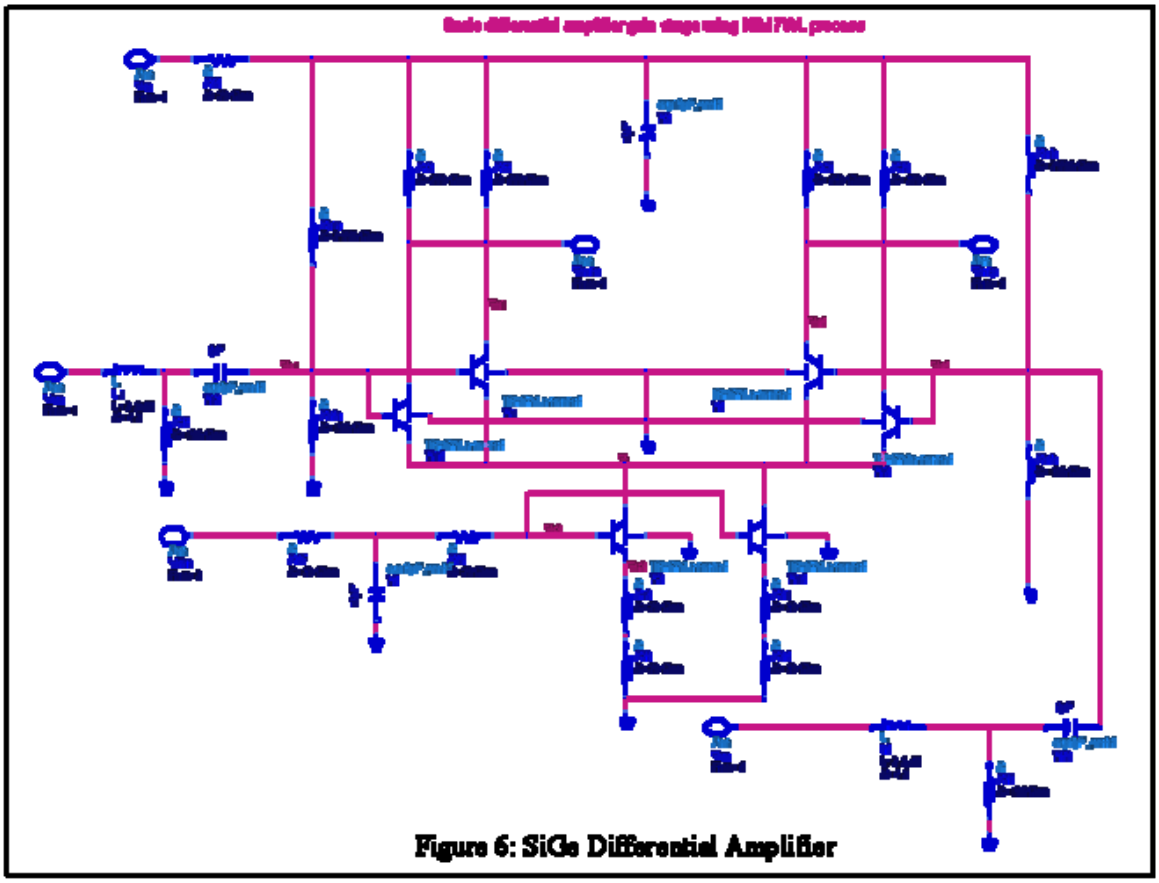

Figure 6: SiGe Differential Amplifier

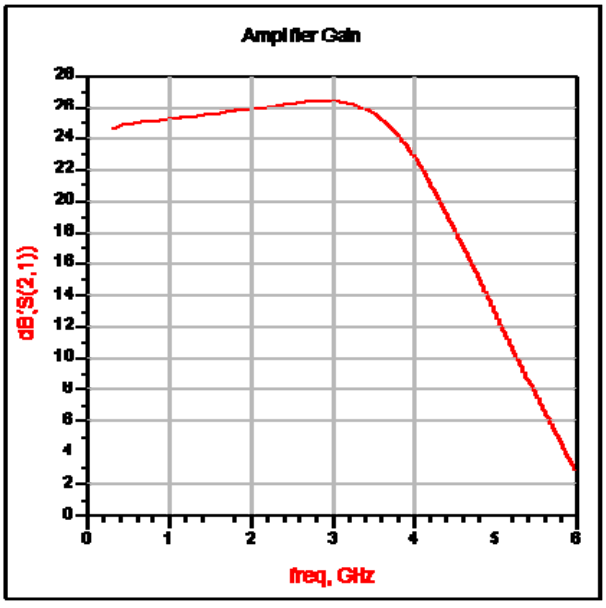

Figure 7: Gain versus frequency response for modified SiGe amplifier

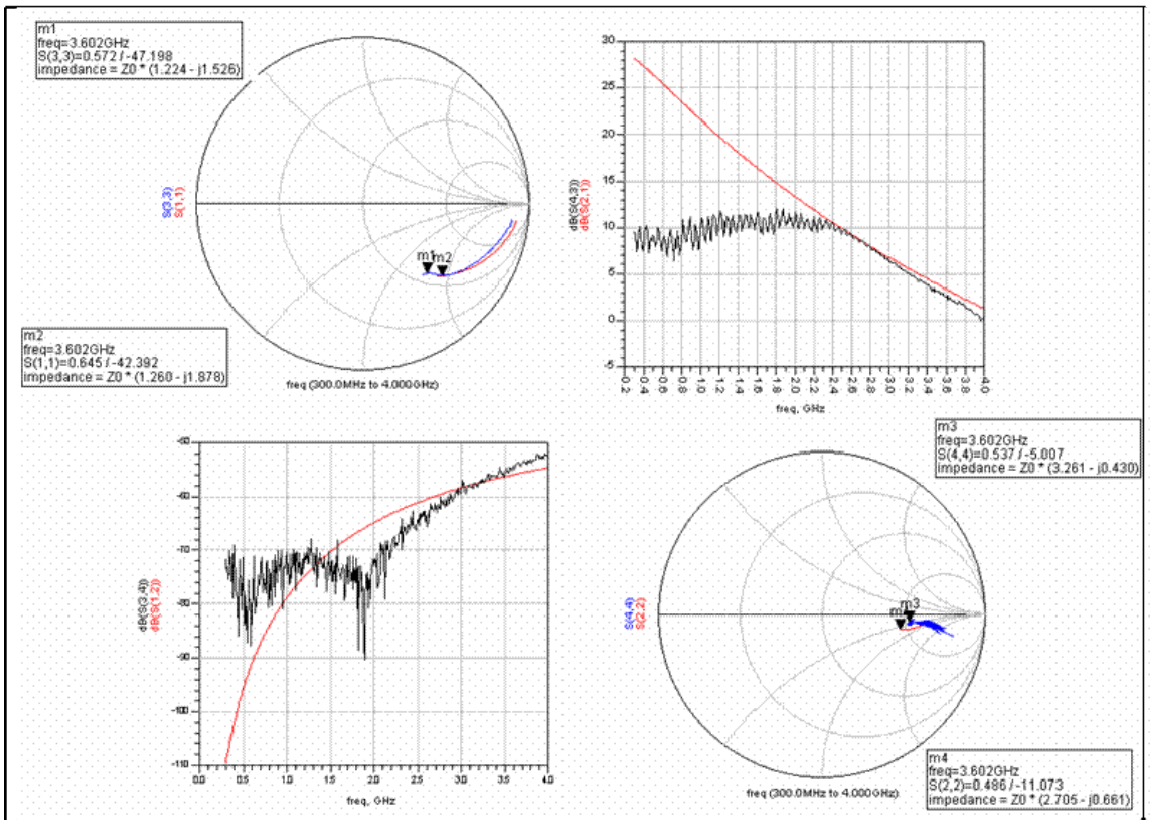

Figure 8: Comparison of SiGe amplifier measurements vs. simulation with extracted NPN model

Substrate

The StaLO multi-chip module (MCM) was designed as a thick film hybrid substrate. It uses a 99.6% alumina substrate that is 25 mils thick. The entire substrate is 2.00 x 0.95 inches. It has traces screen printed on the front and back sides with two separate layers of gold traces separated by a dielectric on the top and a single layer of gold on the back. The substrate with all components mounted on it is shown in figure 9.

The MCM splits into four distinct sections. These are for the 1.2, 3.3 and 3.6 GHz slices and the 100 MHz clock splitter. Each section, except for the clock splitter, is separated from the other sections by the metal walls of a box that fits over the top of the entire MCM substrate. The walls of the box have RF gaskets along the bottom that seal against the substrate. The substrate, in sections along which the box walls fit, has 50mil wide streets of exposed gold ground plane. These extend around the entire perimeter of the substrate and separate the substrate into three main sections, the 1.2 GHz slice with its COTs amplifiers, the 3.3 GHz slice with the 100 MHz clock splitter and the 3.3 GHz COTs amplifiers, and the 3.6 GHz slice with its COTs amplifiers. Each section contains the comb generator, SAW filters, and SiGe amplifiers specific for its frequency. Each section also contains two voltage regulators and two voltage references that have been specifically tuned to provide the optimal voltages and bias levels to maximize gain and minimize spurious signal levels at the frequency of that slice. Finally, each section also

contains COTs amplifiers with sufficient gain to meet StaLO specifications for that frequency.

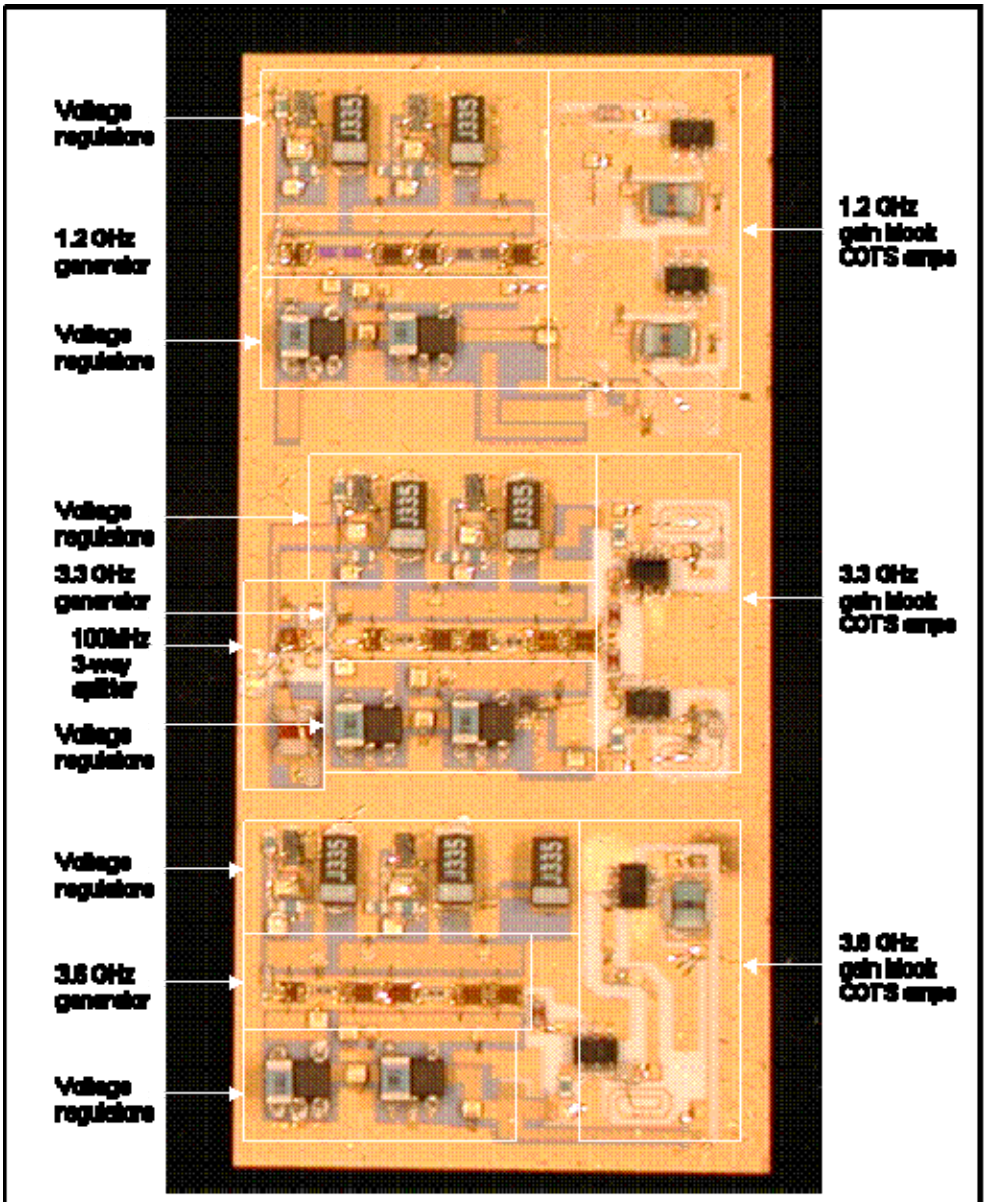

Figure 9: StaLO module substrate

Testing of the COTS Amplifiers

The first step to evaluating the substrate was to build, test, and debug the commercial off-the-shelf (COTS) amplifiers. These are at the output section of each frequency slice. They were evaluated first, since they constitute the only untested portions of the StaLO circuit that operate at microwave frequencies. These amplifiers are used to boost the output signal from the final SiGe stage to the output of the substrate. They also serve to provide an impedance match to 50Ω for devices that use the output of the StaLO. As a

result, it is important that these circuits possess the correct gain, return loss, and isolation to meet StaLO specifications.

The first amplifier set to be evaluated was for the 1.2 GHz channel. The COTs amplifiers need to have a gain (S_{21}) of about 25 dB to be able to lift the output of the 1.2 GHz channel from -10 to -15 dBm at the output of the last SiGe amplifier up to the desired output level of +10 dBm at the output of the StaLO. Furthermore, the desired return loss (S_{22} of the output amplifier) should be less than -15 dB. The design for the COTs output amplifiers was accomplished by using an Agilent 81563 amplifier as a first stage, followed by an Agilent 82563 amplifier to drive the output. The results of testing the output amplifier chain for the 1.2 GHz channel are shown in figure 10. These tests were performed on a network analyzer, an Agilent PNA, while applying V_{cc} = 3.6V. The amplifier performance results appear adequate. The gain (S_{21} = +26 dB) and return loss (S_{22} of the output amplifier = -17dB) meet the requirements stated above. Furthermore, the reverse isolation (S_{12} = -46 dB) should provide adequate reverse leakage protection.

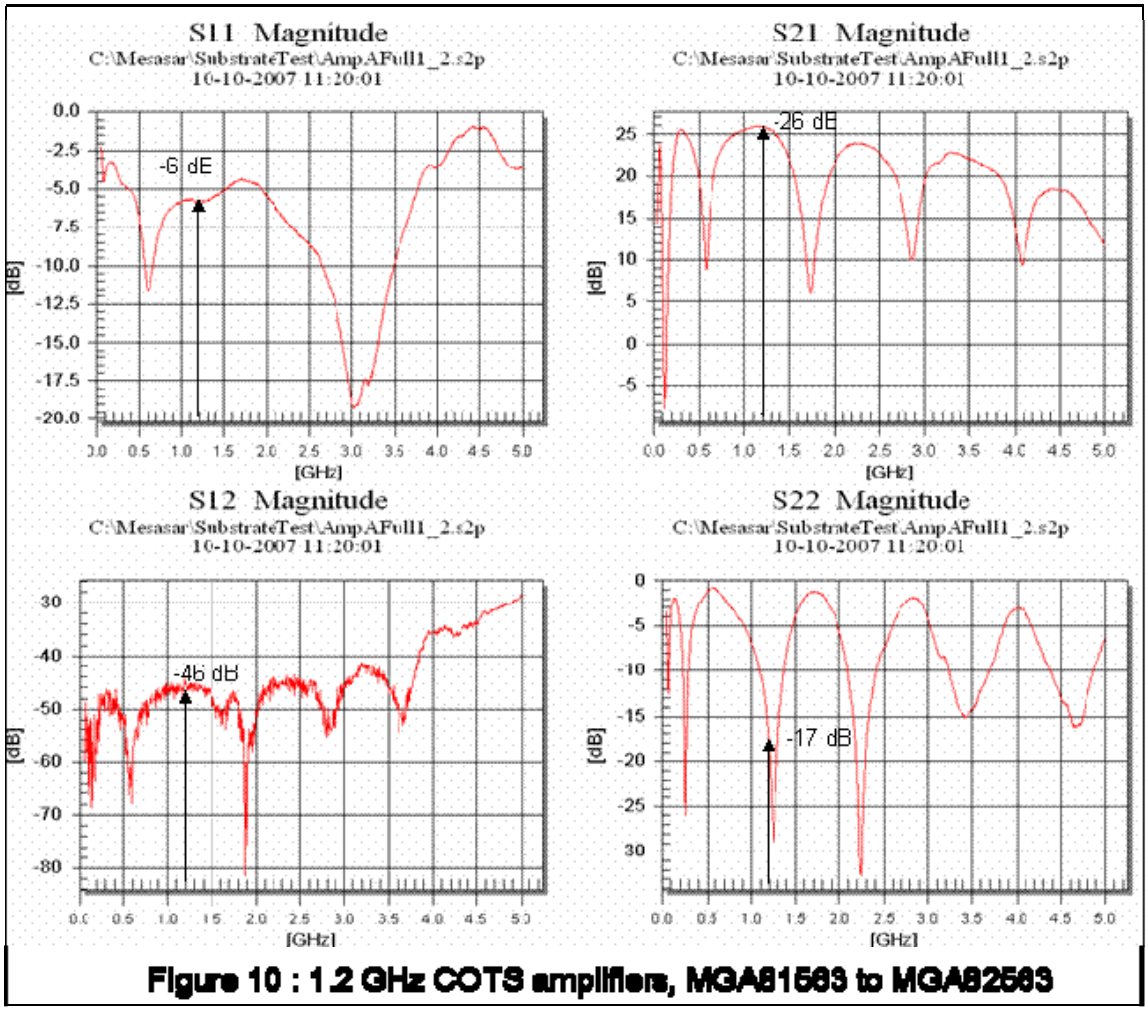

Figure 10 : 1.2 GHz COTS amplifiers, MGA81563 to MGA82563

The second amplifier chain to be evaluated is for the output of the 3.6 GHz channel. This amplifier chain consists of an Agilent 87563 amplifier followed by an Agilent 81563

amplifier. The requirements for this chain are that it be capable of boosting the output of the SiGe amplifier chain from about -16 dBm to +1 dBm at the output of the StaLO. It also needs to provide an output return loss of less than -15 dB. The amplifier chain test results are shown in figure 11. The gain appears to be adequate (S_{21} = +18 dB), but the return loss (S_{22} of the output amplifier = -9dB) is a bit too high. The return loss can be improved in subsequent iterations by the addition of an output matching network or microwave pad. Furthermore, past experience indicates that this is the type of problem that can be solved along with others that may arise in subsequent testing. The reverse isolation (S_{12} = -52 dB) should be adequate to prevent reverse leakage.

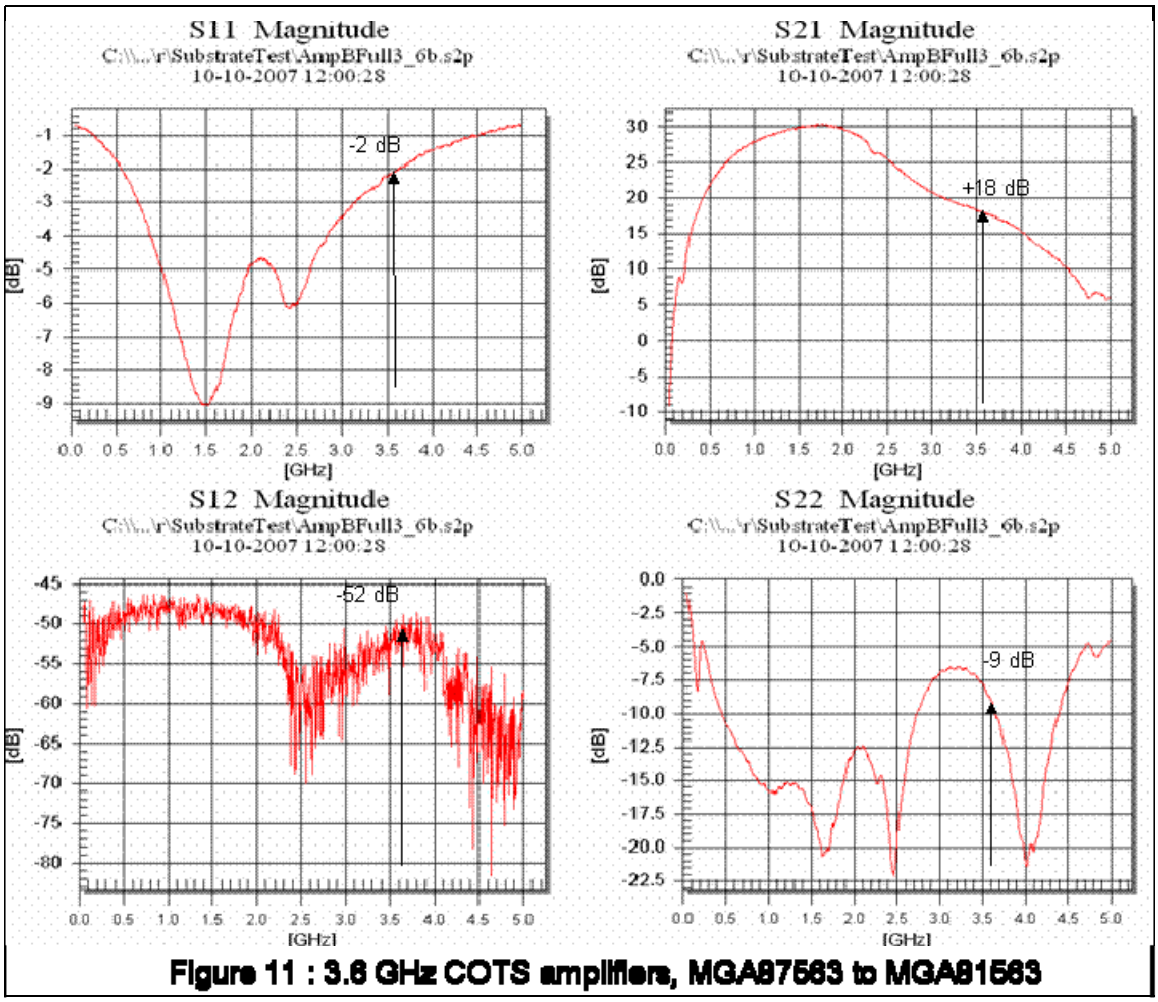

Figure 11 : 3.6 GHz COTS amplifiers, MGA87563 to MGA81563

The third amplifier chain to be evaluated consists of dual COTs amplifiers for the 3.3 GHz StaLO slice. These dual amplifiers are each made from an Agilent 87563 amplifier. The requirements for the 3.3 GHz slice are that it be capable of presenting a pair of outputs at 3.3 GHz. Each output must arise from boosting the output of the SiGe amplifier chain from about -16 dBm up to -8 dBm at each of the two 3.3 GHz outputs of the StaLO. Each output also needs to provide an output return loss of less than -15 dB. The test results from testing one of the duplicate amplifiers in this section (figure 12) indicate that COTs amplifier performance is close to, but a bit below the necessary gain

performance. The gain is low (S_{21} = +7 dB), but the return loss (S_{22} of the output amplifier = -20dB) is excellent. If overall output power of the 3.3 GHz channel proves to be too low to meet specifications, it may be desirable to replace the Agilent 87563 amplifier with an Agilent 81563 or 82563 amplifier to provide higher gain.

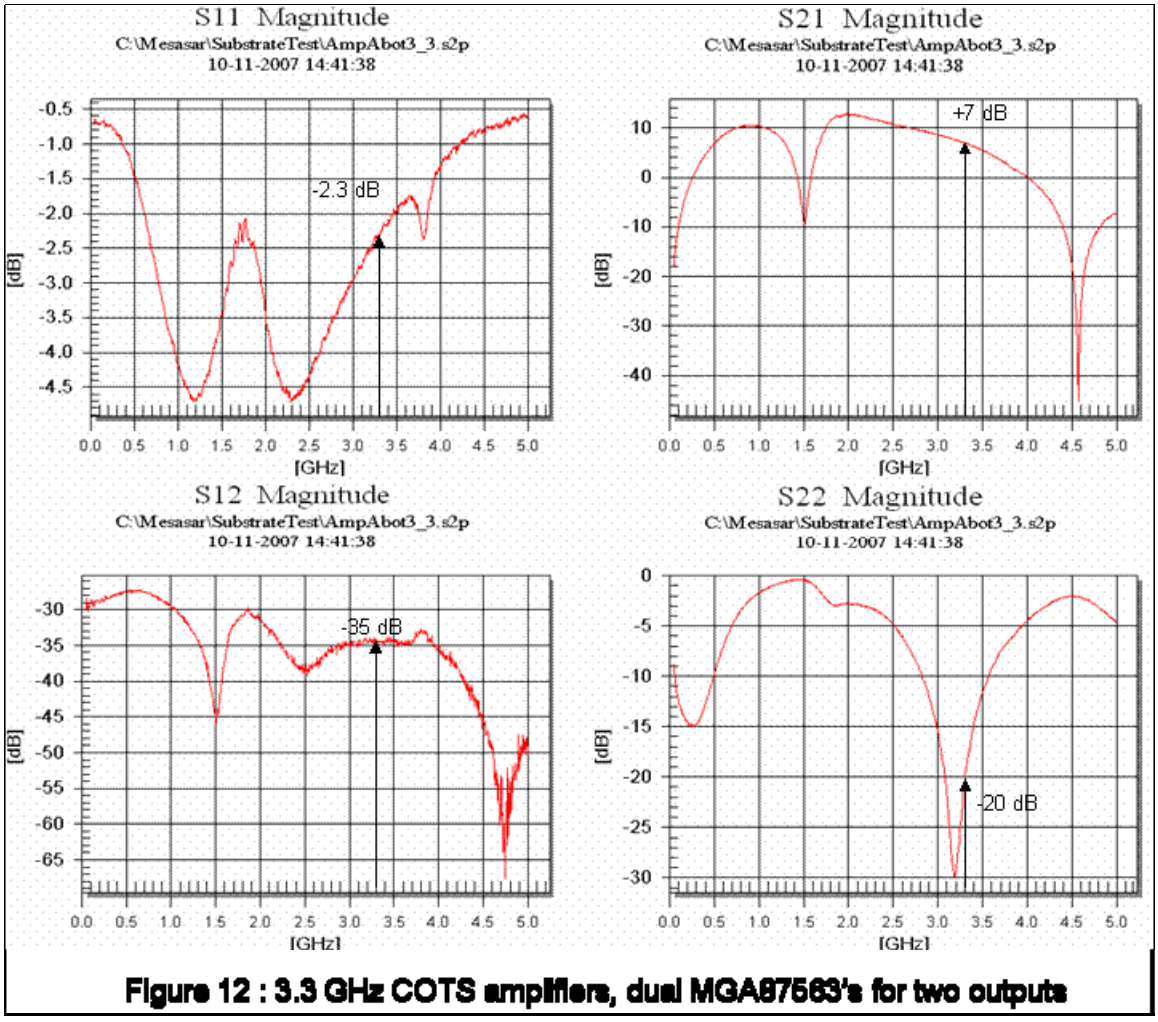

Figure 12 : 3.3 GHz COTS amplifiers, dual MGA87563's for two outputs

Testing of Other Sections

The remaining new, untested addition of RF circuitry to the overall StaLO circuit is the input clock splitter circuit. The clock splitter circuit serves to buffer the input 100 MHz clock signal and to divide the input power into three separate channels with little or no loss in power available to each channel. A passive microwave power splitter will lose 6 dB of signal power when the input is split into four channels. The splitter circuit used for the StaLO is an active integrated circuit that seeks to overcome this disadvantage. The integrated circuit used to accomplish this is a custom SiGe emitter follower with four available outputs. The results of an S-parameter evaluation of this circuit are shown in figure 13. The most significant aspect of the circuit is that the forward transmission path has gain (S_{21} = +2 dB) while preserving reasonable input match (S_{11} = -3.5 dB) and output match (S_{22} = -6.4 dB) parameters. The input match (S_{11} = -3.5 dB) does not meet the requirement for a return loss of -15 dB, however the addition of a simple, narrowband

matching circuit tuned for 100 MHz can be used to improve this. Such an addition might further improve the forward gain of the circuit.

The conclusion of the evaluation of the COTs amplifier sections of the substrate is that all of these sections appear to function with adequate performance to meet overall StaLO specifications given the performance of previously evaluated portions of the StaLO circuit which precede the COTs sections. Gain of each of the COTs amplifiers appears to be marginally adequate for their specific tasks. Return loss of the 1.2 GHz and 3.3 GHz sections also meet specifications. The return loss of the 3.6 GHz output section is slightly out of specification and may need to be improved by the addition of a resonant matching network added to the output of the Agilent 81563 amplifier.

The clock splitter circuit meets StaLO requirements given requirements gleaned from previous test results for subsequent circuitry. The gain of the clock splitter is a benefit, while the input return loss of the clock splitter may need to be improved by the addition of a resonant input matching circuit at 100 MHz.

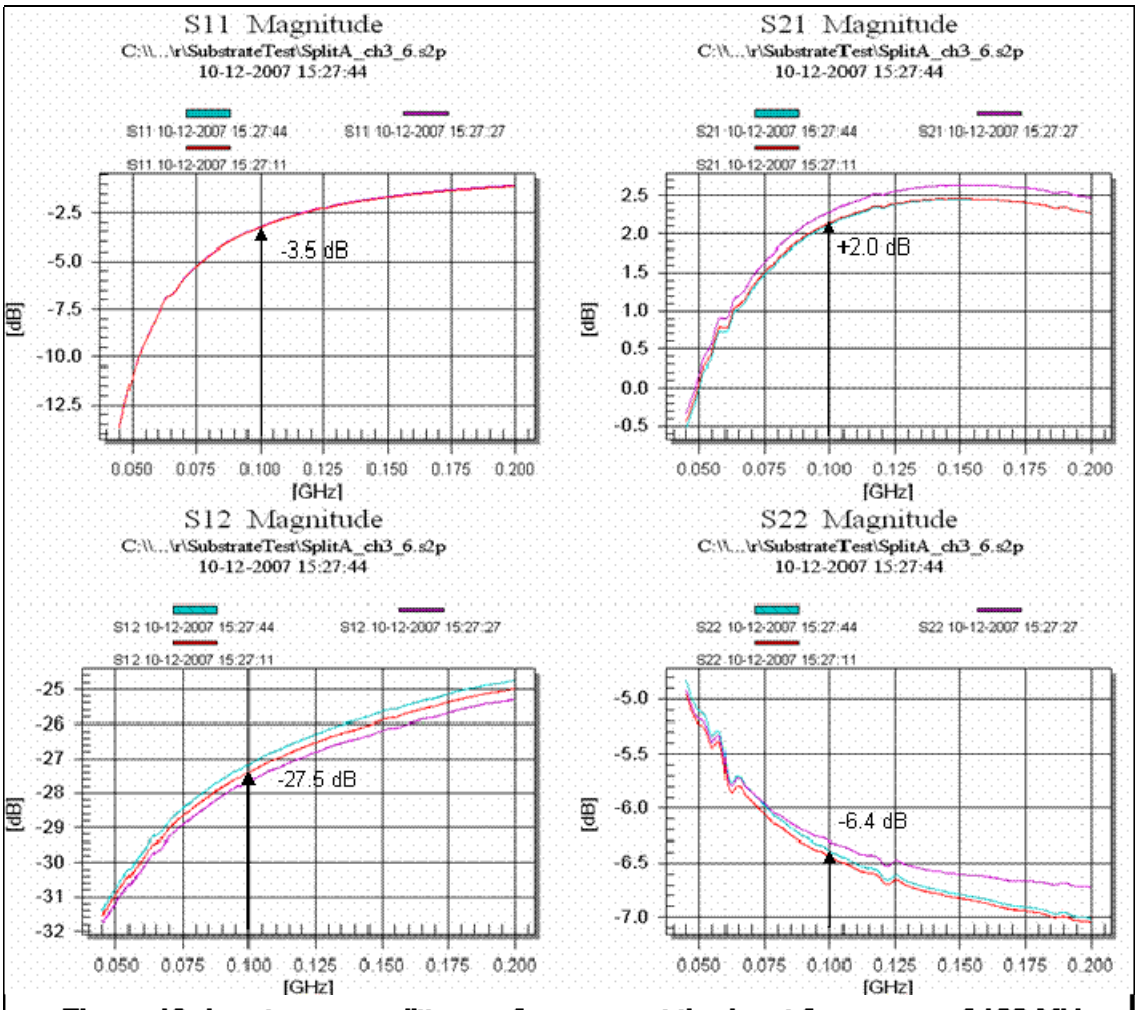

Figure 13: Input power splitter performance at the input frequency of 100 MHz

All twelve voltage regulators and references on the StaLO substrate were fully tested and debugged. Each frequency slice has two voltage references and two voltage regulators. These are required to enable the comb generators and amplifiers to achieve optimal gain and spur suppression at their respective frequencies and to provide isolation from adjacent slice leakage. What are believed to be optimum voltages, determined from previous testing of the StaLO 3.6 GHz slice, are shown in Table 1.

StaLO target voltages	1.2 GHz channel	3.3 GHz channel	3.6 GHz channel
Comb generator Vcc	2.94V @ 87mA	3.01V @ 90mA	2.94V @ 87mA
Comb generator Vbias	1.20V @ 0.1mA	1.20V @ 0.1mA	1.20V @ 0.1mA
Vcenter clock input DC	2.30V @ 0.1mA	2.30V @ 0.1mA	2.30V @ 0.1mA
SiGe amplifier Vcc	3.01V @ 62mA	3.01V @ 62mA	3.17V @ 62mA
SiGe amplifier Vbias	1.20V @ 0.8mA	1.20V @ 0.8mA	1.10V @ 0.8mA

Table 1: StaLO reference and regulator voltages

The last test completed in time to contribute to this report is measurement of the output of the 3.6 GHz slice from the input 100 MHz clock signal through to the output of the final SiGe amplifier. The 3.6 GHz channel is the most challenging from a design and test perspective, since amplifier gains are lowest at that frequency. The output of the 3.6 GHz final SiGe amplifier is shown in figure 14. Signal power out of the SiGe amplifier is about -19 dBm and spur free dynamic range (SFDR) is over 50 dB. This result essentially confirms and repeats the results obtained and reported in SAND2006-6414, in which the 3.6 GHz slice was tested. Routing the signal from the last SiGe amplifier through the final COTs amplifiers in the 3.6 GHz channel should give a final output power of about 0 dBm when the +18 dB gain of the COTs amplifiers is added to the output of the SiGe amplifier. This should render an output at 3.6 GHz that meets specifications with the possible need for an output matching network to improve the return loss.

Conclusion

The StaLO MCM substrate was designed, built, and partially tested to meet the goals set for this fiscal year (FY2007). Two complete StaLO substrates were built to fit into the existing StaLO footprint. New circuitry, including six voltage regulators, six voltage references, three COTs amplifiers, and one SiGe clock power splitter were designed, built, and tested. Testing of the 3.6 GHz slice was performed up to the output of the final SiGe amplifier. Testing of the complete StaLO substrate was not able to be finished in time for this report. In order to be able to test the isolation of the complete StaLO, the new metal lid will also need to be built. Though each of the separate sections of the StaLO has been successfully tested, it is expected that the testing of the integrated system will involve a considerable additional effort beyond what has been finished to date.

References

1) Colin K. Campbell, Surface Acoustic Wave Devices, Academic Press, San Diego, 1998, p. 31.

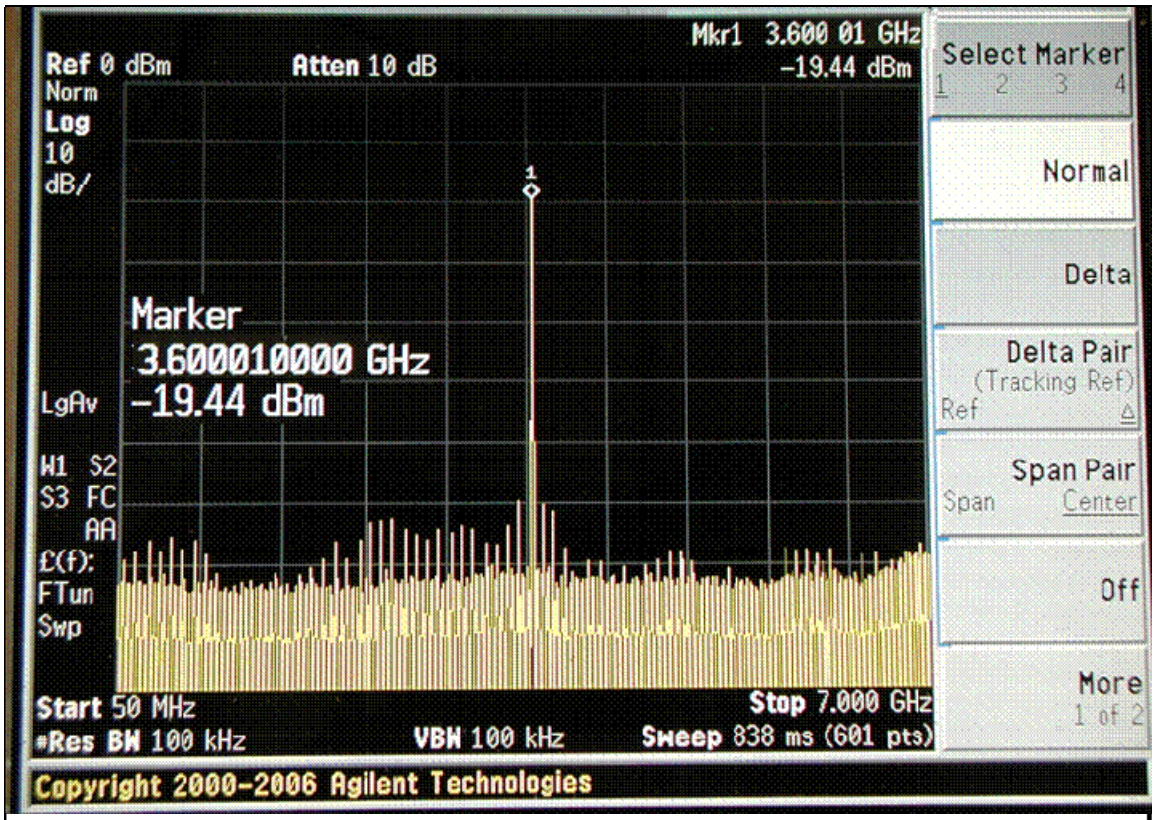

Figure 14: Output of 3.6GHz slice of StaLO, before COTs amps

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