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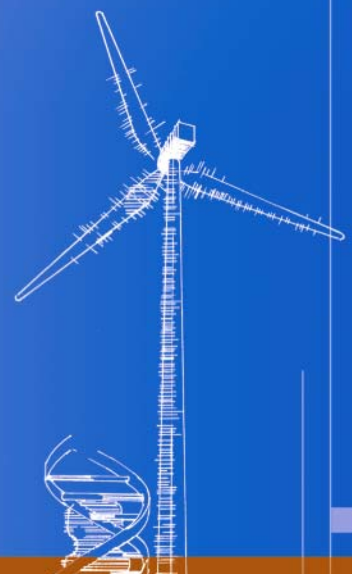
Four-Junction Solar Cell with 40% Target Efficiency Fabricated by Wafer Bonding and Layer Transfer

Final Technical Report
1 January 2005 – 31 December 2007

H.A. Atwater
California Institute of Technology
Pasadena, California

Subcontract Report
NREL/SR-520-44532
November 2008



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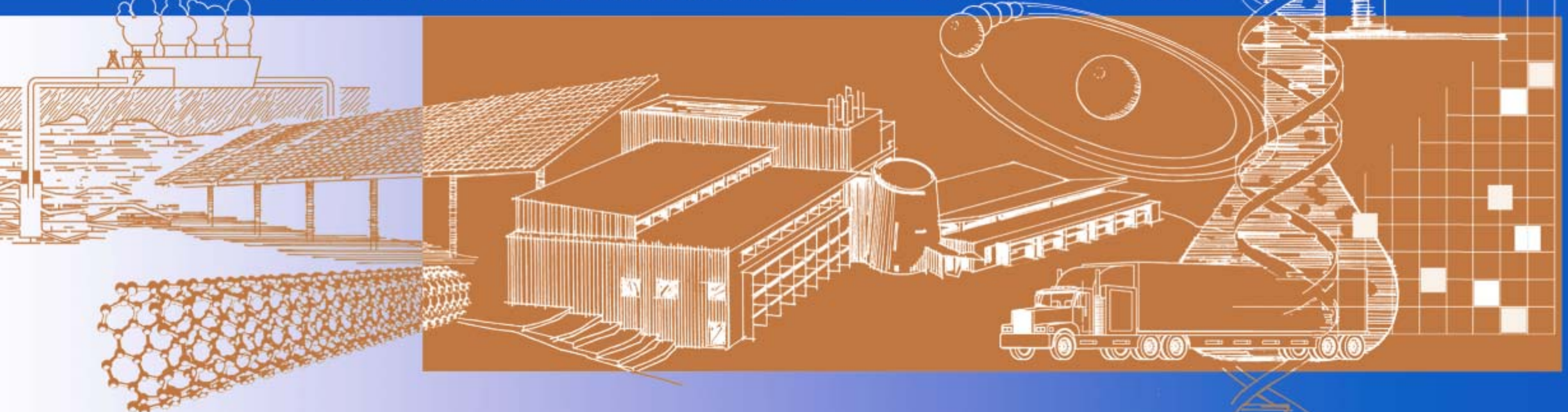

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NREL Technical Monitor: Fannie Posey Eddy

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Summary:

During the grant period 2005-2008, we accomplished the key milestones of the project, which were to realize (i) high quality InGaP/GaAs two junction 'top cells' on Ge/Si templates, (ii) InGaAs/InP 'bottom cells', (iii) direct bond series interconnection of tandem junction solar cells and (iv) modeling of bonded three and four junction solar cell device performance. During the grant period, two graduate students (Katsuaki Tanabe and Melissa Archer) progressed toward their PhD. theses, and both graduated with Ph.D. degrees in 2008. Results from the project were presented at technical meetings (IEEE PVSC, WCPEC, MRS) and disseminated in technical publications. Significant aspects of the project included close industrial collaboration with Spectrolab, Aonex Corporation and Emcore Photovoltaics.

Technical Accomplishments:

GaInP/GaAs Dual Junction Solar Cells on Ge/Si Epitaxial Templates

The Caltech/Spectrolab team achieved a major milestone by demonstrating large area, crack-free GaInP/GaAs double junction solar cells grown by metal organic chemical vapor deposition on Ge/Si templates fabricated using wafer bonding and ion implantation induced layer transfer. The photovoltaic performance of these devices was comparable to those grown on bulk epi-ready Ge, demonstrating the feasibility of alternative substrates fabricated via wafer bonding and layer transfer for growth of active devices on lattice-mismatched substrates.

One of the key milestones of our wafer bonded 4-junction solar cell (GaInP/GaAs/InGaAsP/InGaAs with 1.9eV/1.42eV/1.05eV/0.72eV bandgaps) was the demonstration of layer transfer and wafer bonding to realize GaInP/GaAs dual junction grown on a GaAs or Ge template suitable for integration InGaAsP/InGaAs grown on an InP/Si template. For this structure to be viable, we must have ohmic contacts at the bonded interfaces and good quality epitaxial growth on the bonded templates.

The first step in fabrication of these epitaxial templates was to implant a Ge wafer with H^+ at 180keV and a dose of $1x10^{17}$ cm^{-2}. Next, wet chemical cleaning removed organic and particulate contaminants from both the oxidized Si and Ge wafers. We employed a SiO_2 bonding layer for thermal stability of the transferred film. Just before initiating the

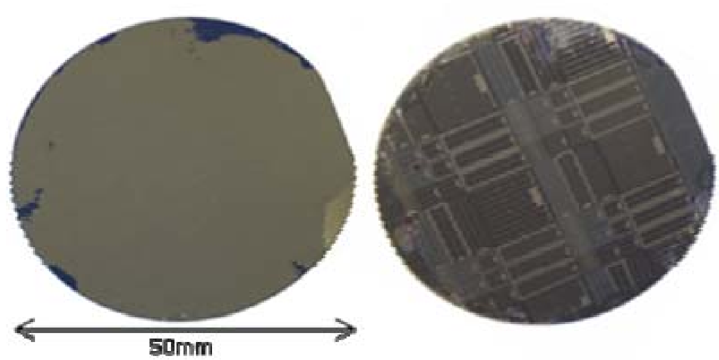


Figure 1. Optical micrographs of a full 50mm Ge/Si template made with layer transfer and wafer bonding (left), and GaInP/GaAs solar cells grown on a Ge/Si template (right).

bond, both substrates were plasma activated. A Suss Microtech SB-6e bonder initiated the bond at a temperature of 200°C. The bonded pair was then annealed at 250-350°C under >1 MPa pressure to induce exfoliation and strengthen the bond between the two wafers. The Ge layer transferred to the Si substrate is approximately 1.4μm thick. Thus far, we have shown up to full 2" wafer layer transfer of Ge on Si as shown in Figure 1.

The RMS roughness of these films after layer transfer was approximately 25nm and the ion implantation induced damaged layer extends approximately 200nm into the film. Removal of the damaged material and abatement of the surface roughness are crucial to enabling high quality epitaxial growth on these substrates. A dilute CP-4 ($HF:HNO_3:CH_3COOH$) wet etch removed the damaged layer. Touch-polishing with a Logitech PM5 chemical mechanical polisher minimized the surface roughness further. Final RMS roughness of the Ge/Si templates is ~0.5nm. Figure 2 shows cross-sectional

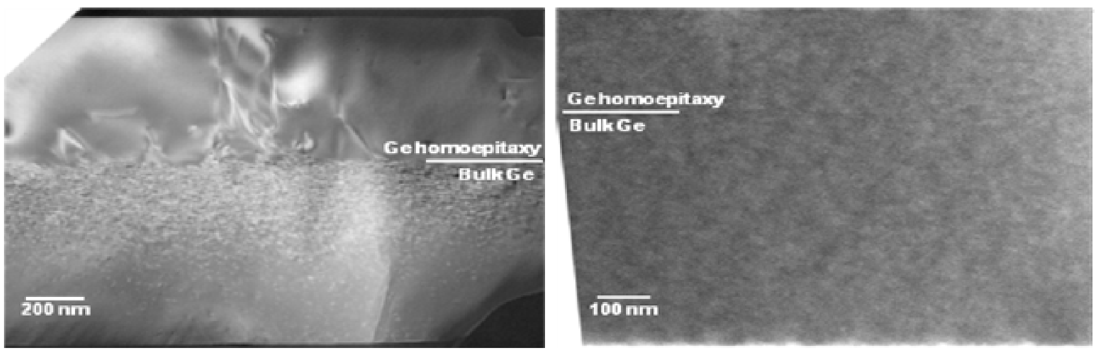


Figure 2. Cross-sectional transmission electron microscopy images of Ge homoepitaxy on a Ge/Si template without damage removal (left) and with damage removal (right). The white line is at the interface of the substrate and the homoepitaxy.

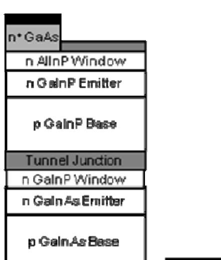


Figure 3. Schematic cross-section of the dual junction solar cell grown and processed by Spectrolab. The bonded interface is shown by a dashed line.

transmission electron microscopy (X-TEM) images of Ge homoepitaxy on Ge/Si templates with and without damage removal. Removal of the ion implantation induced lattice damage produced substrates that are viable for high quality epitaxial growth.

To examine the potential of these substrates for use in heteroepitaxy of high quality III-V materials, dual junction GaInP/GaAs solar cells were grown using Ge/Si epitaxial templates. Figure 3 shows a schematic of the structure. Spectrolab performed all cell growth and processing. Light I-V (current-voltage) performance was measured under AM1.5D illumination (Fig. 4). It should be noted that no anti-reflective coatings were used in these devices. The light I-V data show comparable short circuit current between the control device grown on a bulk Ge substrate and the device grown on a Ge/Si template. However, open circuit voltage is slightly lower (1.97-2.08V vs. 2.16V) in the devices grown on the Ge/Si template. Overall, the device performance is comparable to the control with no loss in fill factor (FF) compared with the control (FF=0.79).

Spectral response measurements (Fig. 4 inset) indicated the GaInP cell band gap has shifted approximately 60meV from ~1.74eV to ~1.8eV. This shift in the band gap is attributed to the observed slight change in GaInP composition. The Ge substrate used for the control sample in these growths was (100) oriented with a miscut of 6° toward the <011> orientation, whereas the Ge wafer used to make the Ge/Si template was (100) oriented with a miscut of 9° toward the <011> orientation. Higher miscut substrates have lower In composition for the same growth conditions.[10] Shown in Figure 5 is the HR-XRD data for the control sample and the Ge/Si template sample. The scan on the control sample shows the top cell to be compressively strained -691 seconds, which corresponds to an indium composition of about 53% indium, assuming it's 100% strained. On the other hand, the Ge/Si sample is lattice matched, which corresponds to an indium composition of 49.5%. Increasing indium composition by 3.5% decreased the band gap by ~64 meV[11], which correlates well with spectral response measurements.

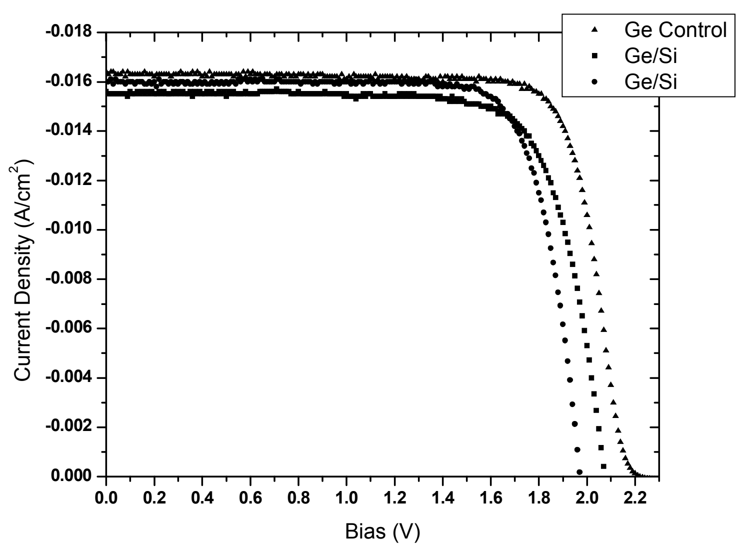


Figure 4. Photovoltaic I-V curves for the GaInP/GaAs solar cells grown on Ge/Si epitaxial templates and on a bulk epi-ready Ge substrate

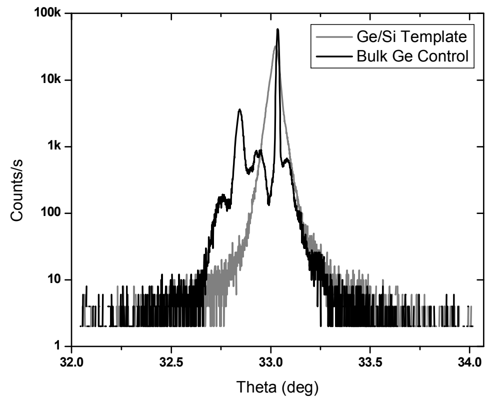
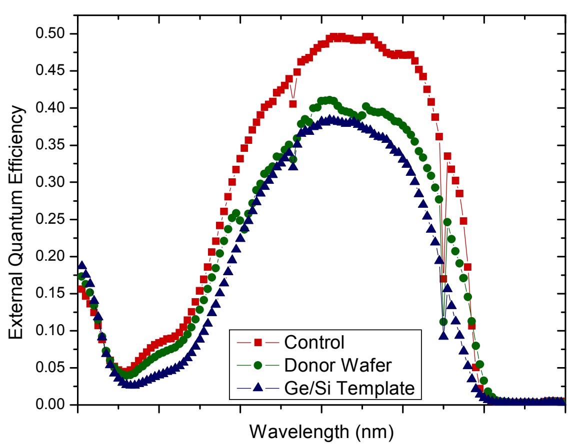


Figure 5. High-resolution X-ray diffraction rocking curves for the GaInP/GaAs solar cells grown on Ge/Si epitaxial templates and on a bulk epi-ready Ge substrate.

Initial Work on Bonding, Double Heterostructures

Early in the project , in 2005-early 2006, effort focused on fabrication of GaAs and GaInP double heterostructures on Ge/Si substrates. After achieving promising results on the GaInP DHs we decided to try to make preliminary solar cells. Spectral response measurements were taken on the GaInP top cell and converted to external quantum efficiency (see Fig. 6). The Ge/Si template shows about the same overall quantum efficiency as the donor wafer giving us further proof that the surface preparation is dominating the performance of these devices, not the CTE-mismatch induced strain. However, there is some red response loss in the template sample denoting a lower diffusion length in the template sample. Initial light IV data shows promise for the template samples as the short circuit current is similar to the donor wafer sample (see Fig. 4).



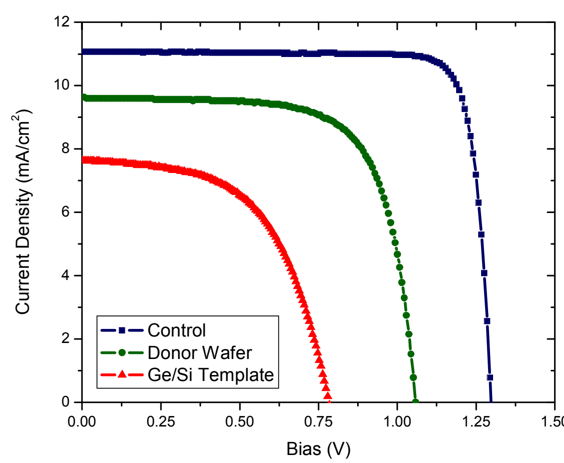


Figure 6. External quantum efficiency and Light IV data for the first GaInP solar cell grown on Ge/Si templates.

Since the surface preparation was dominating the performance of our devices, we investigated chemical-mechanical polishing (CMP) processes for these templates, which ultimately was a key factor that led to the successful top cell process described above. We purchased a CMP system, and work with chemical mechanical polishing with $1cm^2$ Ge donor wafers showed that the roughness of can be drastically reduced by polishing with a silica slurry. The RMS roughness of the samples tested dropped from ~20nm to <1nm. This was a great improvement over the wet chemical etch process we had been using earlier. In addition, there were no etch artifacts left behind in these samples as there were with the wet etch (Fig 7-8).

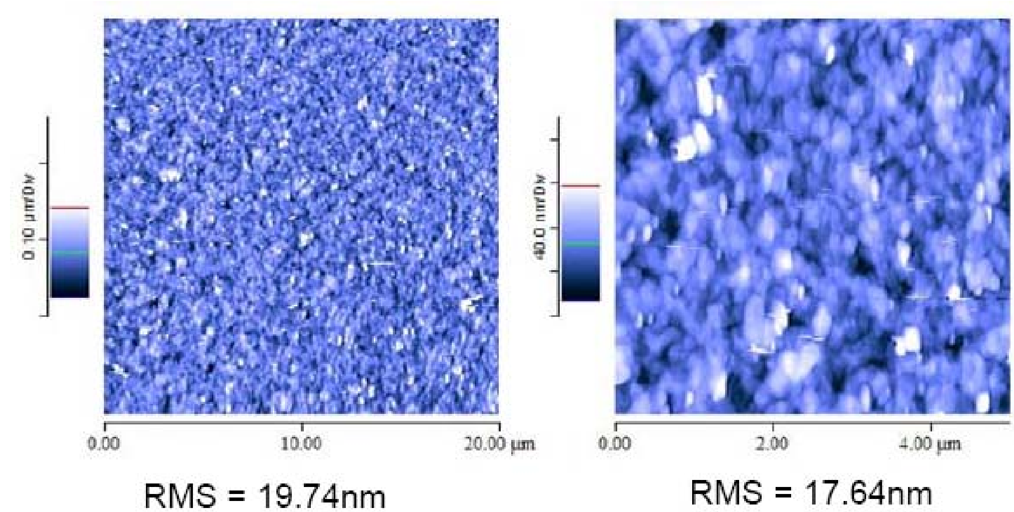


Figure 7. Representative AFM scans of the Ge surface after exfoliation

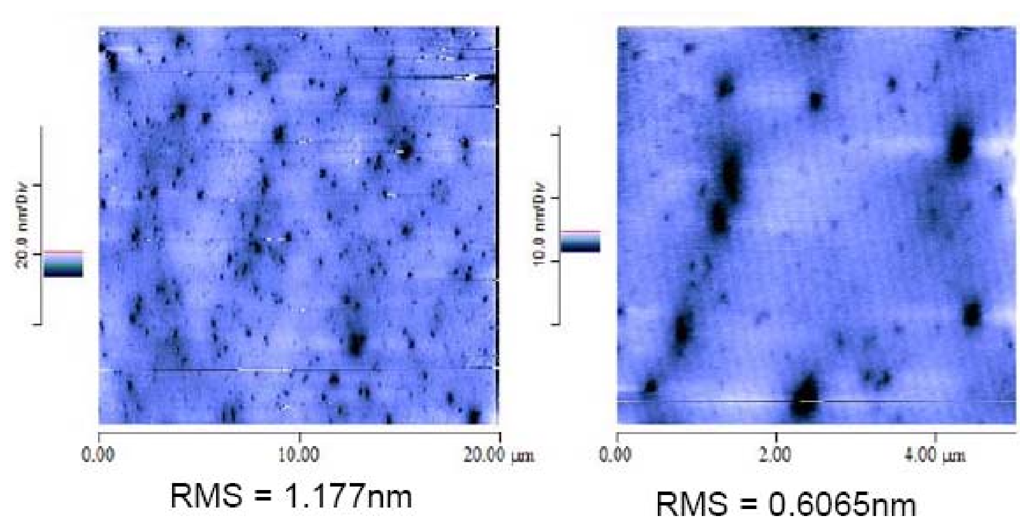


Figure 8. Representative AFM scans of the Ge surface after CMP

InGaAs/InP/Si Bottom Subcells

We fabricated InP/Si epitaxial templates through wafer bonding and helium-induced exfoliation of InP and in collaboration with Aonex, and Emcore fabricated and tested InGaAs solar cells on those templates. The devices are depicted schematically in Fig. 9. The cell consisted of a 1 um thick InP buffer layer that functions as a current spreading layer for lateral back side contact. The backside contact is InGaAs heavily doped n-type. A tunnel-junction structure was used to switch the material doping at the back contact from p-type to n-type, so that the front and back contacts could be fabricated with a single lithographic process. The remainder of the structure was typical of a single-junction InGaAs cell, as shown in Fig. 9. On top of this structure a conventional InP window layer followed by and InGaAs contact layer for making top contacts was grown.

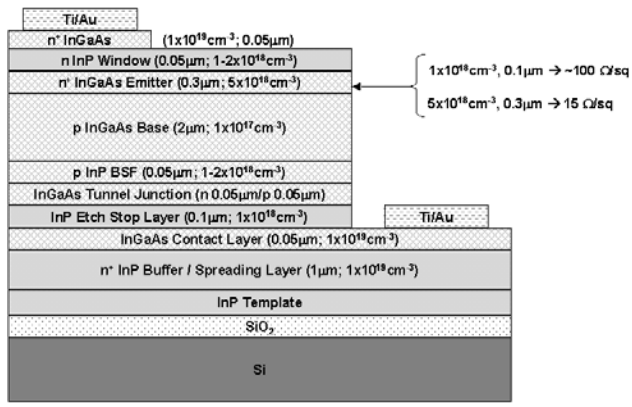


Figure 9. Schematic of InGaAs/InP/SiO_2/Si cell

The basic process for fabrication of InP/Si engineered epitaxial templates begins with the ion implantation of a (001) InP wafer. Next, the InP wafer is bonded to a (001) Si wafer with a grown silicon dioxide (SiO_2) film, which improves thermal stability relative to structures fabricated with a direct semiconductor-semiconductor bond after cleaning and surface preparation in a clean environment. The two substrates are then annealed under pressure. This anneal has two purposes. First, it enables covalent bonds to form between the InP and Si substrates. Second, it causes the implanted ions to coalesce in the InP wafer, until a thin layer of InP separates from bulk substrate and is transferred to the Si substrate. The remaining InP can be processed and used to create another template layer. Finally the InP/Si template is annealed again during subsequent epitaxial growth, further facilitating covalent bond formation at the bonded interface.

A typical image of an InP/Si epitaxial template fabricated by transferring a thin InP film to a deposited SiO_2 film on Si is shown in Fig. 10. The film was transferred from an InP substrate implanted with He^+ to a dose of $1x\ 10^{17}$ cm^{-2} at an energy of 180 keV. The transferred InP film thickness was ~900 nm.

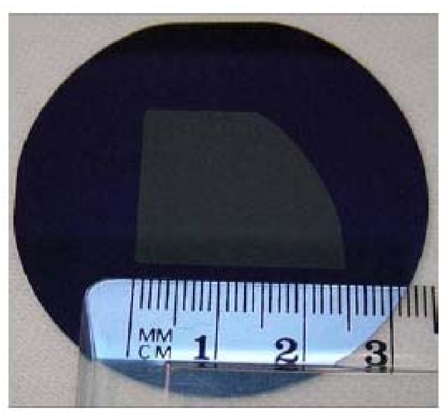


Figure 10. Photographic image of InP/Si film after transfer.

An unavoidable consequence of the use of high ion implantation doses to induce film exfoliation is that crystallographic defects are introduced in the near surface region of the transferred film with the peak of that damage roughly coinciding with the depth at which exfoliation occurs. Thus, in the final InP/Si structure there is a distribution of

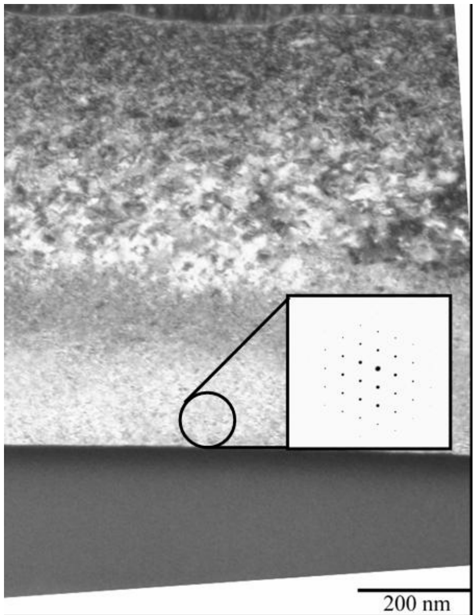


Figure 11. Cross-sectional transmission electron microscope image of an InP/Si epitaxial template fabricated using InP implanted with 115 keV He^+ to a dose of 1.0x 10^{17} cm^{-2} showing the strain contrast caused by defects caused during ion implantation and (inset) selected-area diffraction image indicating that the InP adjacent to the bonded interface (within ~200 nm) is crystalline.

lattice defects with a peak at the surface of the transferred film decreasing to a minimum defect density in the material adjacent to the bonded interface. Fig. 11 shows a representative cross-sectional transmission electron microscopy (XTEM) micrograph of a film transferred from InP implanted with 115 keV He^+ to a dose of 1.0x 10^{17} cm^{-2}. The inset selected area diffraction (SAD) pattern shows that the InP adjacent to the bonded interface is predominantly single-crystalline. Close inspection of the defect structure using high-resolution XTEM imaging shows that the strain contrast apparent in Fig. 8 is caused by a both extended defects that can be directly imaged and point defects such as vacancies and interstitials. It is essential that the damage in the as-transferred InP thin film in InP/Si engineered epitaxial templates be minimized prior to epitaxial growth of III-V materials, especially extended defects that intersect the growth surface. The damaged surface region of the as-transferred InP film was removed using a combination of inductively-coupled plasma reactive ion etching (ICP-RIE) for damage removal and wet chemical etch for surface smoothing etching process to leave a film of ~400 nm with a roughness of ~10 nm-rms, as measured by contact mode atomic force microscopy (AFM).

To test the performance of III-V compound active photovoltaic device layers grown on the InP/Si epitaxial templates in functional solar cell structures, single-junction InGaAs solar cells were grown on both the InP/Si templates and commercial bulk epi-ready (001) InP substrates by metalorganic chemical vapor deposition (MOCVD). Each of the solar cells had an n-type InGaAs emitter and a p-type InGaAs base with bandgap energy of 0.74 eV, nominally lattice-matched to (001) InP. The cells were designed to enable convenient and low-resistance contact to both base and emitter through the top surface of the cell. Photovoltaic current-voltage (I-V) characteristics of the 4 mm^2 InGaAs cells grown on the InP/Si templates and on bulk (001) InP substrates were measured under a spectral portion truncated at 850 nm by a long-pass filter, considering use as subcells under GaAs, from 1-sun AM1.5 Global solar spectrum. The photovoltaic I-V characteristics of the InGaAs solar cells grown on the InP/Si epitaxial templates and a bulk InP substrate are shown in Fig. 12. The device parameters for the InGaAs cell grown on the wafer-bonded InP/Si epitaxial template were J_{sc} = 24.9 mA cm^{-2}, V_{oc} = 0.30 V and FF = 0.66, where J_{sc}, V_{oc} and FF are short-circuit current, open-circuit voltage and fill factor, respectively. This performance was comparable to that of the InGaAs cells grown on bulk (001) InP substrates, J_{sc} = 21.5 mA cm^{-2}, V_{oc} = 0.31 V and FF = 0.70. Fig. 12 (inset) shows the spectral responses for the InGaAs solar cells grown on the InP/Si epitaxial templates and a bulk InP substrate. The larger J_{sc} and the higher quantum efficiency for the cell grown on the InP/Si template are attributed to the high reflectivity by the $InP/SiO_2/Si$ heterostructure, estimated to be ~0.45 at maximum in the IR range for normal incidence from the basic electromagnetic theory while the reflectivity at the InGaAs/InP interface is less than 0.005, due to the large refractive index differences at the InP/SiO_2 and SiO_2/Si interfaces. No significant bandgap shift was caused by the InP/Si epitaxial template structure as certified by the spectral response result. These photovoltaic I-V characteristic and spectral response results indicate that the fabricated InP/Si epitaxial templates are promising alternative substrates to InP bulk wafers for InGaAs solar cell production. The obtained J_{sc} of 24.9 mA cm^{-2} for the InGaAs cell on the InP template is large enough to current match the state-of-art InGaP/GaAs two-junction cells. This InGaAs cell is therefore a strong candidate for the bottom cell of an ultrahigh efficiency three-junction cell with its significantly higher V_{oc} than the conventional Ge bottom cell.

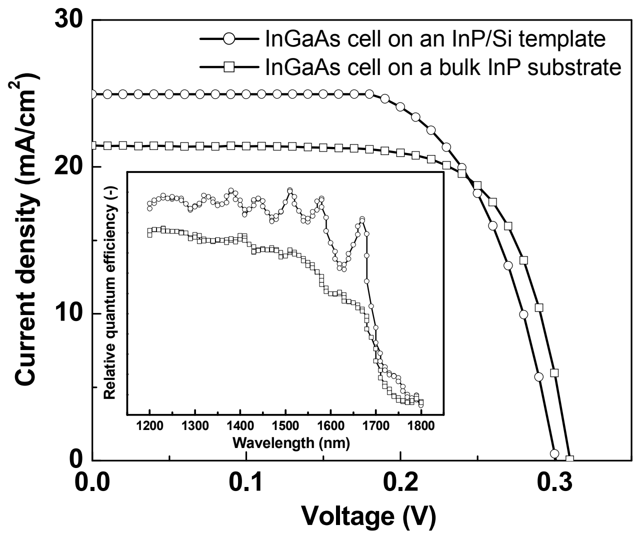


Figure 12. Photovoltaic I-V curves and (inset) spectral responses for the InGaAs solar cells grown on the InP/Si epitaxial templates and on a commercial bulk epi-ready InP substrate. The I-V measurements were under a spectral portion truncated at 850 nm from 1-sun AM1.5G spectrum.

Modeling

This year, further work was carried out on our implementation of a device physics based model for multijunction solar cells. Initially,

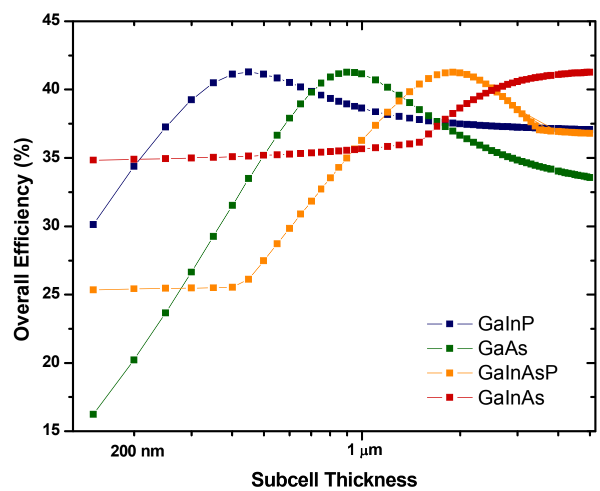


Figure 13. Overall four junction efficiency as a function of subcell thickness, varying one cell thickness at a time.

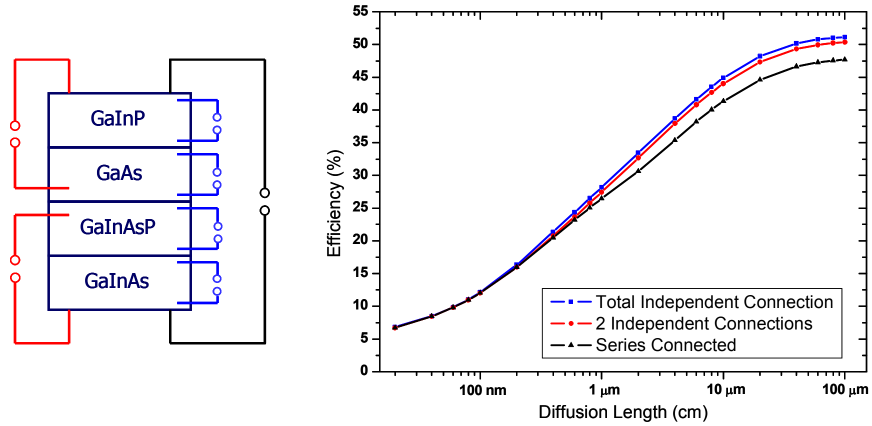


Figure 14. Overall cell efficiency as a function of the diffusion length in all four subcells for 3 different electrical connections.

we are focusing on the four junction structure proposed in this project. Primary design considerations for the model include: flux filtering from the tunnel junctions and subcells above; series resistance at bonded interfaces and in tunnel junctions; temperature and doping effects; filtering from window layers; shunt resistance; electrical connection options; flexible variation of E_g and subcell thickness; spectral shifts throughout the day and year; and optimization for the maximum power over the entire day or year.

In constructing the model, the standard electron transport equations were used including diffusion/drift, continuity, and Gauss' Law. Shockley-Read-Hall recombination was used. To simplify the equations, the following assumptions were made: abrupt p-n junction, 1-D carrier transport only, depletion approximation, depletion region recombination due to single trap level at mid-gap, following Sah, Noyce and Shockley model. In an effort to incorporate more of the realistic behaviors of III-V materials, an empirical model for mobility as a function of temperature and doping concentration was used as well as a Drude model for free carrier absorption. We are working on incorporating a better model for free carrier absorption that includes inter- and intra-valley transitions.

One of the first things that became obvious when we started to run the model is the importance of optimizing the cell thicknesses when current-matching was enforced. Figure 13 shows the overall efficiency of the four junction device as a function of subcell thickness evaluated by varying one cell thickness while keeping all the others constant.

An interesting parameter we can vary with this model (along with material parameters) is the type of electrical connection used in the device. Figure 14 shows a schematic of the 3 different types of connections we evaluated as well as the overall efficiency of the four junction cell as a function of the diffusion length in all four subcells. Each data point is representative of the optimized device at those conditions. As the material quality improves, the gain achieved through independent connections increases. At the highest quality evaluated, the difference between the series connected device and the completely independently connected device is ~3.5%. Interestingly, the 2 independent connection scheme gives us 80% of the total gain and is much more feasible.

In addition, we used reference flux data from Keith Emery for the "sunny hot day" to investigate the effects of the changing flux throughout the day. The subcell thicknesses were optimized for the peak flux of the day for each of the three electrical connections and then the power out at each hour was calculated for each of the 3 multijunction solar cells. Figure 15 shows the power out as a function of time in the day as well as the overall efficiency at each time in the day. The efficiency plots make the advantages of independent connections very clear. The most interesting result of this calculation is that ~70% of the gain achieved by total independent connection can be achieved with just 2 independent connections.

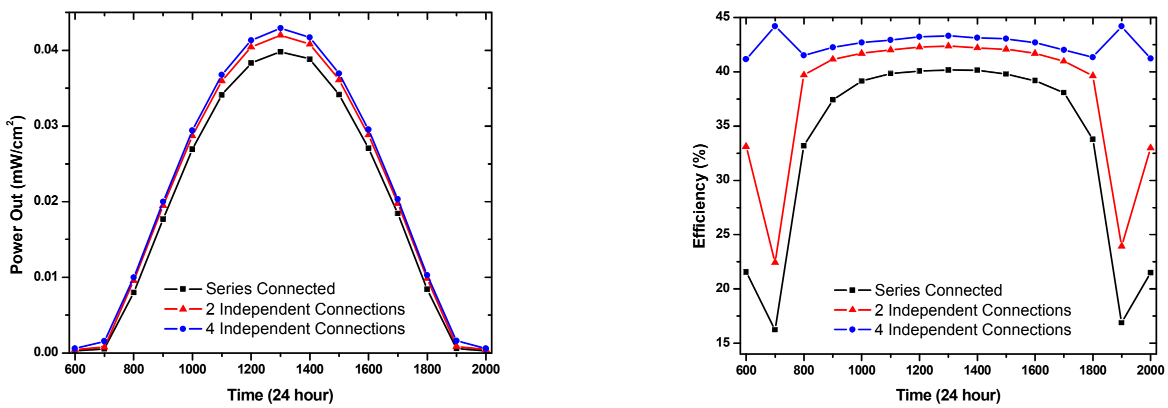


Figure 15. Overall performance of the four junction cell as a function of the time of day for the three different electrical connections.

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Presentations under Subcontract

1. "High Efficiency Photovoltaics: Meeting the TeraWatt Challenge", Harry Atwater, Future Now Conference, British-American Business Council, , Los Angeles, CA May 18th, 2007.
2. "High Efficiency Photovoltaics: Meeting the TeraWatt Challenge", Harry Atwater, Caltech Clean Energy and Transportation Conference, Pasadena, CA, May 11th, 2007.
3. "High Efficiency Photovoltaics", Harry Atwater, Shell Research, Houston TX, May 8th, 2007.
4. "High Efficiency Photovoltaics", Harry Atwater, NSF-Intelligence Community Power Workshop, Reston, VA, April 24th, 2007.
5. "Four Junction Solar Cell with 40% Target Efficiency Fabricated by Wafer Bonding and Layer Transfer", Harry Atwater, DOE Solar Energy Technologies Program Review, Denver, CO, April 16th , 2007.
6. "Design Approaches and Materials Processes for Ultrahigh Efficiency Lattice Mismatched Multijunction Solar Cells", Harry A. Atwater, paper FF8.2 (invited), Materials Research Society Spring Meeting: April 17 - 21, 2006 San Francisco, CA.
7. "p-n Junction Device Physics Modeling of Four Junction Solar Cell Efficiency", Melissa J. Griggs, Brendan M. Kayes, and Harry A. Atwater, paper FF8.3, Materials Research Society Spring Meeting: April 17 - 21, 2006 San Francisco, CA
8. "Direct-bond Interconnected Multijunction GaAs/InGaAs Solar Cell", K. Tanabe, D. J. Aiken, M. W. Wanlass, A. Fontcuberta i Morral and H. A. Atwater, MRS Spring Meeting, San Francisco, CA, paper FF 8.5 (2006).
9. "Design Approaches and Materials Processes for Ultrahigh Efficiency Lattice Mismatched Multi-Junction Solar Cells", Melissa J. Griggs, Daniel C. Law, Richard R. King, Arthur C. Ackerman, James M. Zahler, Harry A. Atwater, 4th World Conference on Photovoltaic Energy Conversion: May 7-12, 2006 Waikoloa, HI
10. "Lattice-mismatched Monolithic GaAs/InGaAs Two-junction Solar Cells by Direct Wafer Bonding", K. Tanabe, D. J. Aiken, M. W. Wanlass, A. Fontcuberta i Morral and H. A. Atwater, 4th World Conference on Photovoltaic Energy Conversion: May 7-12, 2006 Waikoloa, HI.
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During the grant period of 2005-2008, we accomplished the key milestones of the project, which were to realize (i) high-quality InGaP/GaAs two-junction "top cells" on Ge/Si templates, (ii) InGaAs/InP bottom cells, (iii) direct-bond series interconnection of tandem-junction solar cells, and (iv) modeling of bonded three- and four-junction solar cell device performance.

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