# SPi – User Manual V0.1

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## Abstract:

This document describes the Serial Powering Interface (SPi) ASIC. SPi is a general purpose ASIC prototype designed for use in serial powering of silicon detector instrumentation. This description is written as a user manual to aid application, not as a design description.

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# Contents

# 1. Introduction

SPi is a generic custom ASIC, manufactured in 0.25µm CMOS by TSMC[1], to interface between a constant current source and silicon detector read-out chips. There is no SEU (single event upset) protection, but most (not all) components are radiation tolerant design. An operating voltage of 1.2 to 2.5 volts and other design features make the IC suitable for a variety of serial powering architectures and ROICs. It should be noted that the device is likely to be a prototype for demonstration rather than a product for inclusion in a detector. The next design(s), SPin, are likely to be designed for a specific application (eg SLHC).

The component includes

- Seven bi-directional LVDS-like buffers for high data rate links to/from the read-out chips. These are AC coupled (series capacitor) off-chip for DC level conversion;
- A programmable internal programmable shunt regulator to provide a defined voltage to readout chips when linked in a serial powering chain;
- A programmable internal shunt regulator control circuit for external transistor control;
- Shunt current measurement (for internal shunt regulator);
- A programmable internal shunt regulator current alarm;
- Two programmable linear regulators.

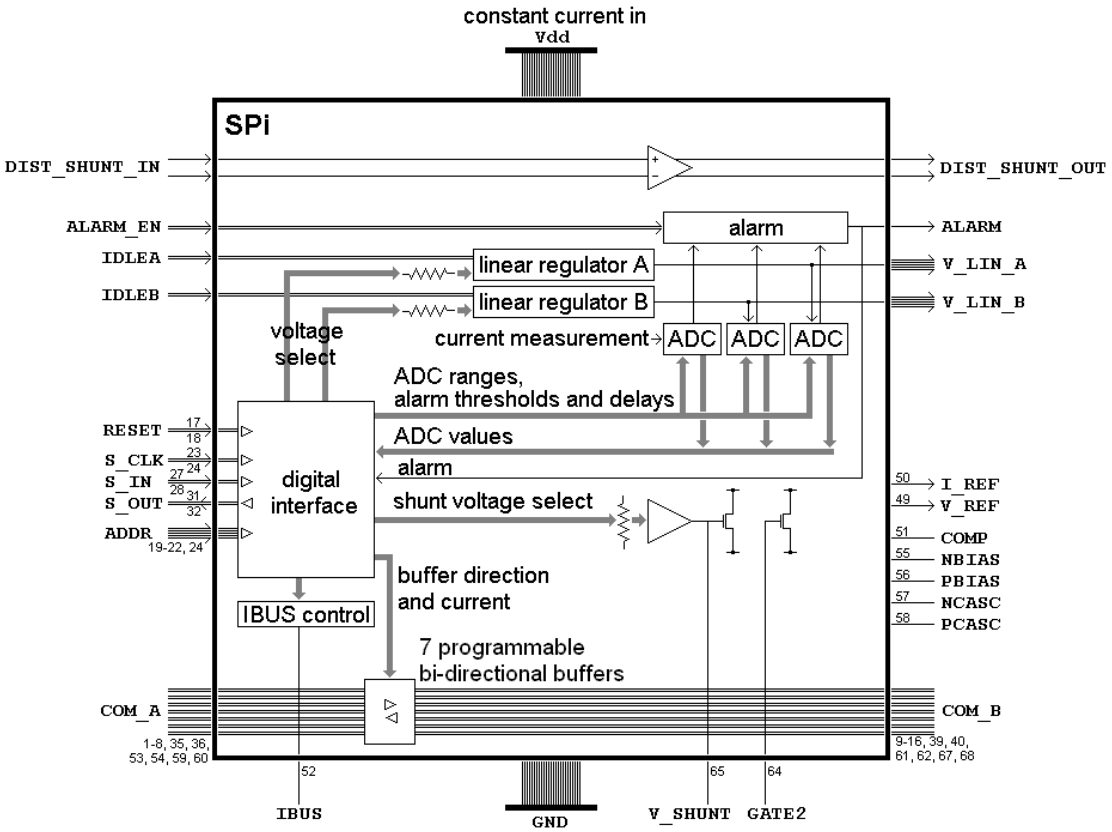



**Figure 1** – The SPi chip block diagram, showing all connections

[1] TSMC: Taiwan Semiconductor Manufacturing Company Ltd. http://www.tsmc.com/

A block diagram is shown in figure 1. Power for each block is derived from the serial power supply. Alarm and enable/idle lines are omitted.

## *1.1 Component description*

The main task of the ASIC is to supply constant voltage power to front-end electronic detector components. A programmable shunt regulator is provided to do this. A controller interfaces to a serial external bus and this can be used to set parameters including the shunt regulator voltage. Additional features are two linear voltage regulators and 7 programmable bi-directional LVDS drivers and three ADCs.

On power-up the chip resets into a defined default state: The shunt regulator is set at 1.5 volts and the SPi is ready to carry out commands from an external device such as a PC which we will define as a "SPi Master". A reset input can be used to set this condition at any time while the SPi is powered.

A number of SPis may be connected to the single "SPi Master" using a multi-drop bus consisting of 3 LVDS-like pairs as shown in figure 2. Note that LVDS (as defined by TIA/EIA-644 and the IEEE 1596.3 standards) cannot be used because the signals must be AC coupled. External capacitors AC couple (DC block) the data to/from each SPi because each SPI will operate at a different voltage with respect to the common ground within the SPi Master (this is the nature of serial powering). Thus local ground for each SPi and associated read-out chips will be different. Consequently only *changes* in serial data lines (rising and falling edges) are seen by the SPi chips. However the bus used is similar in that it uses voltage differentials over pairs of lines, can operate at similar speeds and is similarly immune to interference issues. The first of these LVDS-like pairs is a free-running (asynchronous) clock (`s_clk`) generated externally to the SPI. This is used within SPI to latch data (`s_in`), the second input. The third (`s_out`) is an output synchronised to the clock input.

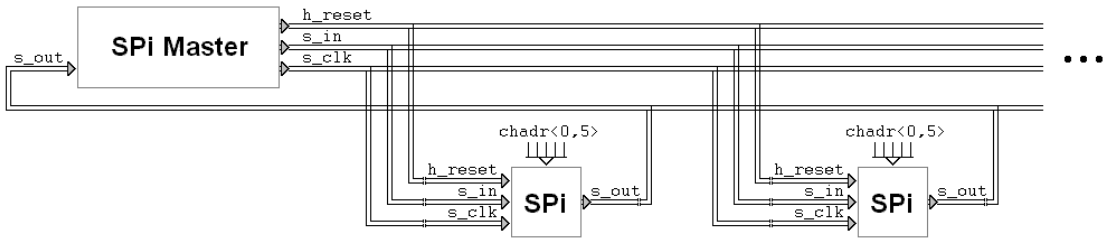



**Figure 2** – Many SPis connected to a single "SPi Master".
SPi name conventions as used by designers.

Once configured, most parameters will remain constant while the SPi is powered, but the SPi Master may command each SPi to report some parameters occasionally in a polled fashion.

# Physical description

## *1.2 Dimensions*

Spi dimensions are shown in Figure 3.

Notes

- All connection pads are the same size, octagons, 80µm passivation opening.
- The 15 unlabled pads towards the left of centre (Figure 4) of the device are not connected.
- Approximate cut die size 2675µm x 5471µm (design size 2816µm 5722µm).
- Distance from similar outer-most pads to edge (as shown top left) is 100µm approx (exact measurement depends upon die cutting)
- This is the “chip-pad-view”, not PCB footprint for bump bonding. PCB footprint is mirror image.
- 68 "active" pads (including 4 unused, excluding un-labeled) + 76 power pins = 144 pads total.

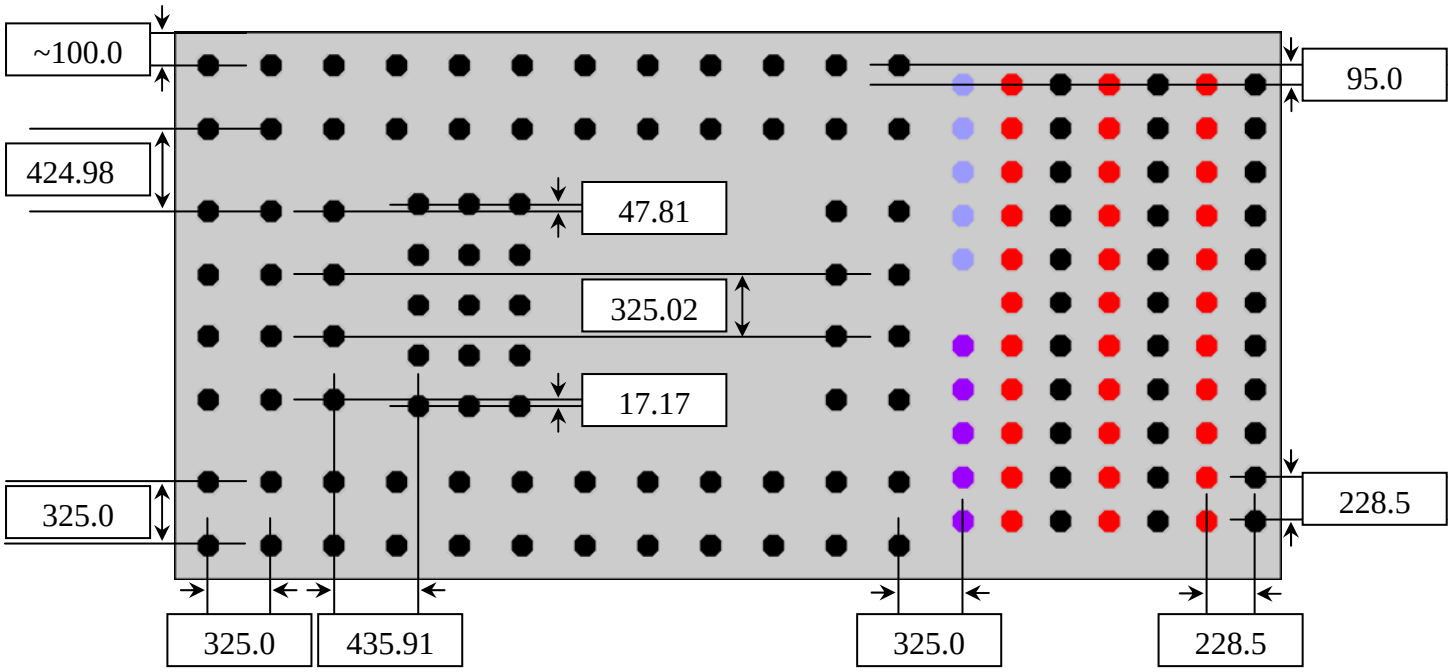



**Figure 3** –SPi dimensions.
Dimensions in µm.
(Produced from information provided by Marcel Trimpl)

## *1.3 Pad numbers*

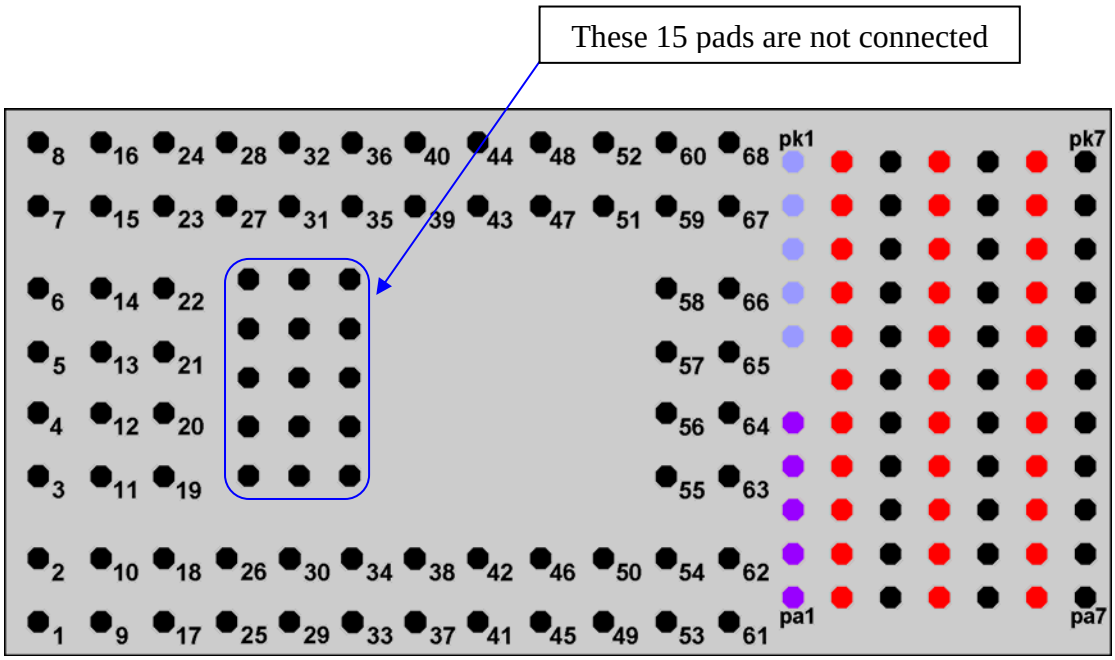



**Figure 4** –SPi pad numbering.
(Defined by Richard Holt)

Power pads:

VDD
GND
V_LIN_A
V_LIN_B

The colours of the pads shown above reflect the pad function, not the appearence of the pads on SPi.

## *Pad identification*

| Pad number | Pad name | I/O | Description |
|---|---|---|---|
| *** | **C O N T R O L** | *** | |
| 1 | COM6 A- | | Data port 6 A |
| 2 | COM6 A+ | | |
| 3 | COM5 A+ | | Data port 5 A |
| 4 | COM5 A- | | |
| 5 | COM4 A- | | Data port 4 A (default = receiver) |
| 6 | COM4 A+ | | |
| 7 | COM3 A+ | | Data port 3 A (default = receiver) |
| 8 | COM3 A- | | |
| 9 | COM6 B- | | Data port 6 B |
| 10 | COM6 B+ | | |
| 11 | COM5 B+ | | Data port 5 B |
| 12 | COM5 B- | | |
| 13 | COM4 B- | | Data port 4 B (default = driver) |
| 14 | COM4 B+ | | |
| 15 | COM3 B+ | | Data port 3 B (default = driver) |
| 16 | COM3 B- | | |
| 17 | RESET- | i | Resets the SPi to power-up configuration |
| 18 | RESET+ | i | |
| 19 | A3 | i | SPi address bit 3 |
| 20 | A2 | i | SPi address bit 2 |
| 21 | A1 | i | SPi address bit 1 |
| 22 | A0 | i | SPi address bit 0 |
| 23 | S CLK+ | i | Serial data interface clock. Data is latched on the rising edge of S_CLK+. Frequency 1 to 50 MHz. |
| 24 | S CLK- | i | |
| 25 | DIST SHUNT IN+ | i | Differential input for “distributed shunt” concept. Pin 26 = VDD/2; Pin 25=VDD. |
| 26 | DIST SHUNT IN- | i | |
| 27 | S IN+ | i | Serial data interface commands to SPi |
| 28 | S IN- | i | |
| 29 | DIST SHUNT OUT2 | o | To 2 shunt transistors within ABCn. |
| 30 | DIST SHUNT OUT1 | o | |
| 31 | S OUT+ | o | Serial data interface response from SPi |
| 32 | S OUT- | o | |
| 33 | Dummy | | No electrical connection |
| 34 | A4 | i | SPi address bit 4 |
| 35 | COM0 A+ | | Data port 0 A |
| 36 | COM0 A- | | |
| 37 | IDLEA+ | i | Disable linear regulator A |
| 38 | IDLEA- | i | |
| 39 | COM0 B+ | | Data port 0 B |
| 40 | COM0 B- | | |
| 41 | IDLEB+ | i | Disable linear regulator B |
| 42 | IDLEB- | i | |
| 43 | ALARM EN+ | i | Enables the shunt threshold ADC to initiate an alarm output (see alarm) when the shunt current exceeds a preset value. |
| 44 | ALARM EN- | i | |
| 45 | POWER DOWN- | i | These pins are not connected within SPi. May be used in the next version. |
| 46 | POWER DOWN+ | i | |
| 47 | ALARM+ | o | Indicates the shunt voltage has exceeded a preset value. Not latched within SPi. |
| 48 | ALARM- | o | |
| 49 | V REF | | Voltage reference. Connect to GND through 100pF, with facility to measure. |
| 50 | I REF | | Current reference. Connect to GND using a jumper to provide option to measure the current |

| | | | |
|---|---|---|---|
| | | | to GND using a meter. |
| 51 | COMP | | Connect to GND through 100pF, with facility to measure |
| 52 | IBUS | | Current references. Connect to GND using a jumper to provide option to measure the current to GND using a meter. |
| 53 | COM2 A- | | Data port 2 A (default = receiver) |
| 54 | COM2 A+ | | |
| 55 | NBIAS | | Connect to GND through 100pF, with facility to measure |
| 56 | PBIAS | | Connect to VDD through 100pF, with facility to measure |
| 57 | NCASC | | Connect to GND through 100pF, with facility to measure |
| 58 | PCASC | | Connect to VDD through 100pF, with facility to measure |
| 59 | COM1 A+ | | Data port 1 A |
| 60 | COM1 A- | | |
| 61 | COM2 B- | | Data port 2 B (default = driver) |
| 62 | COM2 B+ | | |
| 63 | Dummy | | No electrical connection |
| 64 | GATE2 | | Connect through jumper to pin 65 |
| 65 | V SHUNT | | See pin 64. Normally only connected to pin 64. |
| 66 | Dummy | | No electrical connection |
| 67 | COM1 B+ | | Data port 1 B |
| 68 | COM1 B- | | |
| | | *** **POWER** *** | |
| pa1 | V LIN A | o | Linear regulator output A |
| pb1 | V LIN A | o | Linear regulator output A |
| pc1 | V LIN A | o | Linear regulator output A |
| pd1 | V LIN A | o | Linear regulator output A |
| pe1 | V LIN A | o | Linear regulator output A |
| pg1 | V LIN B | o | Linear regulator output B |
| ph1 | V LIN B | o | Linear regulator output B |
| pi1 | V LIN B | o | Linear regulator output B |
| pj1 | V LIN B | o | Linear regulator output B |
| pk1 | V LIN B | o | Linear regulator output B |
| pa2 | VDD | | From constant current source + |
| pb2 | VDD | | From constant current source + |
| pc2 | VDD | | From constant current source + |
| pd2 | VDD | | From constant current source + |
| pe2 | VDD | | From constant current source + |
| pf2 | VDD | | From constant current source + |
| pg2 | VDD | | From constant current source + |
| ph2 | VDD | | From constant current source + |
| pi2 | VDD | | From constant current source + |
| pj2 | VDD | | From constant current source + |
| pk2 | VDD | | From constant current source + |
| pa3 | GND | | From constant current source - |
| pb3 | GND | | From constant current source - |
| pc3 | GND | | From constant current source - |
| pd3 | GND | | From constant current source - |
| pe3 | GND | | From constant current source - |
| pf3 | GND | | From constant current source - |
| pg3 | GND | | From constant current source - |
| ph3 | GND | | From constant current source - |
| pi3 | GND | | From constant current source - |
| pj3 | GND | | From constant current source - |
| pk3 | GND | | From constant current source - |

| | | | |
|---|---|---|---|
| pa4 | VDD | | From constant current source + |
| pb4 | VDD | | From constant current source + |
| pc4 | VDD | | From constant current source + |
| pd4 | VDD | | From constant current source + |
| pe4 | VDD | | From constant current source + |
| pf4 | VDD | | From constant current source + |
| pg4 | VDD | | From constant current source + |
| ph4 | VDD | | From constant current source + |
| pi4 | VDD | | From constant current source + |
| pj4 | VDD | | From constant current source + |
| pk4 | VDD | | From constant current source + |
| pa5 | GND | | From constant current source - |
| pb5 | GND | | From constant current source - |
| pc5 | GND | | From constant current source - |
| pd5 | GND | | From constant current source - |
| pe5 | GND | | From constant current source - |
| pf5 | GND | | From constant current source - |
| pg5 | GND | | From constant current source - |
| ph5 | GND | | From constant current source - |
| pi5 | GND | | From constant current source - |
| pj5 | GND | | From constant current source - |
| pk5 | GND | | From constant current source - |
| pa6 | VDD | | From constant current source + |
| pb6 | VDD | | From constant current source + |
| pc6 | VDD | | From constant current source + |
| pd6 | VDD | | From constant current source + |
| pe6 | VDD | | From constant current source + |
| pf6 | VDD | | From constant current source + |
| pg6 | VDD | | From constant current source + |
| ph6 | VDD | | From constant current source + |
| pi6 | VDD | | From constant current source + |
| pj6 | VDD | | From constant current source + |
| pk6 | VDD | | From constant current source + |
| pa7 | GND | | From constant current source - |
| pb7 | GND | | From constant current source - |
| pc7 | GND | | From constant current source - |
| pd7 | GND | | From constant current source - |
| pe7 | GND | | From constant current source - |
| pf7 | GND | | From constant current source - |
| pg7 | GND | | From constant current source - |
| ph7 | GND | | From constant current source - |
| pi7 | GND | | From constant current source - |
| pj7 | GND | | From constant current source - |
| pk7 | GND | | From constant current source - |

# 2 Logical description

## *2.1 Control*

A multi-drop AC-coupled serial data interface is used to configure and control SPi and allow operating parameters to be read. This means several SPi components can be connected to a single bus, consisting of S_CLK, S_IN, S_OUT and (optionally) H_RESET LVDS-like pairs. Each pair is referenced to the serial powering ground at the constant current power supply. This is shown in Figure 2 and, in more detail, in Figure 5.

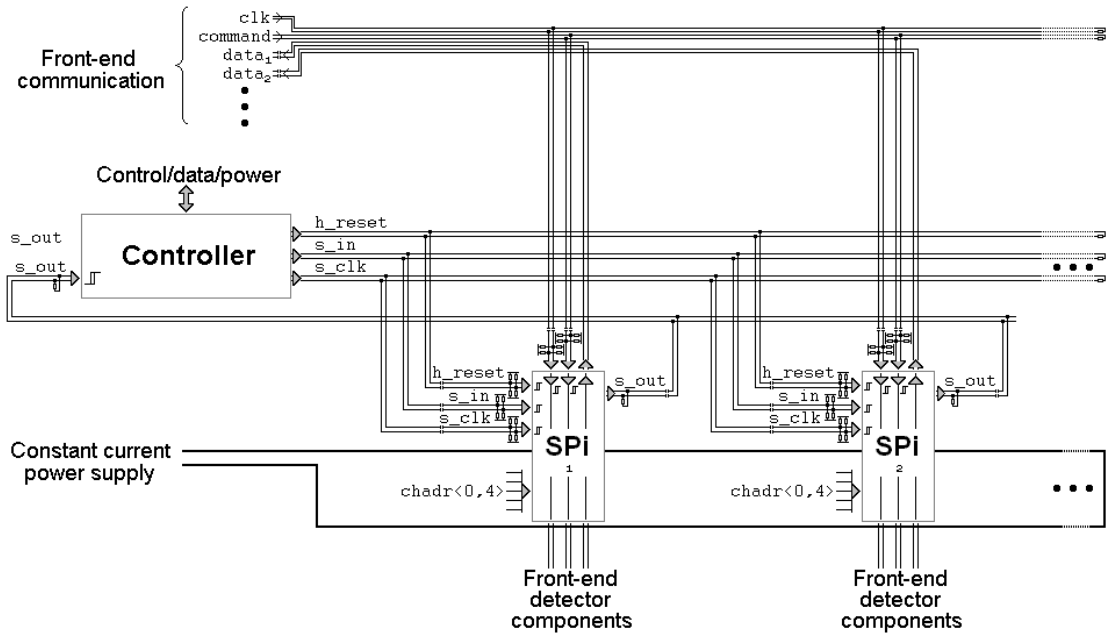



**Figure 5** – Many SPi components connected as a system.
SPi name conventions as used by designers.

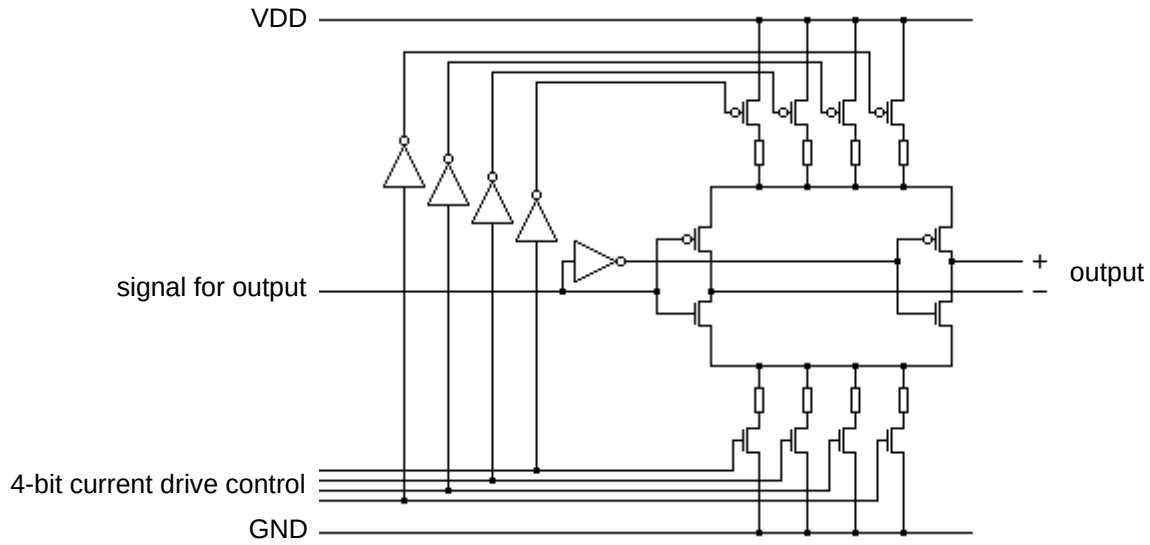



**Figure 6a** – Output drivers.

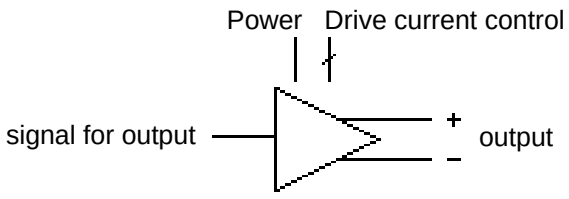



**Figure 6b** – Simplified output drivers.

A failure in a single SPi component is not likely to affect other components on the bus. Each SPi on a bus must have a unique identity specified by a chip address. Each SPi has five address bits which are hard-wired externally to define its address. There can be a maximum of $2^5$ - 2 = 30 SPi components on a single bus. (Two command addresses, 0 and 21 decimal, are assigned a special purpose (see section nnn)). Serial-in is a common input to all SPis and a single LVDS termination resistance at the far end of the multi-drop pair (not shown in diagrams 2 and 5). Serial-out may be driven by any single SPi on the bus and has a single termination resistance. When a command is issued only one addressed SPi can reply to the command so there is no chance of bus contention. (But note that every SPi will respond to address 00000). Thus normal operation will be for the controller to command each connected SPi separately. A SPi will not send information unless commanded to do so by the controller.

### 2.1.1 Command data format

Commands are always issued from the Controller and a response is only issued from the single SPi with the corresponding address (where this is included in the circuit). Commands (Figure 5) are always 32 bits long. Responses (Figure 6) are always 8 bits long.

- For each group of bits the MS bit is set first (left-most in figures below and chronologically)
- If the header (`1100111`) is not read correctly the rest of the command is ignored. The header is fixed for all SPis
- If the address (`CCCCC`) does not match the hardware inputs `chadr<0:4>` the command is ignored by SPi.
- The trailer (`0000`) is not checked by SPi, but is added only to make the command 32 bits long.

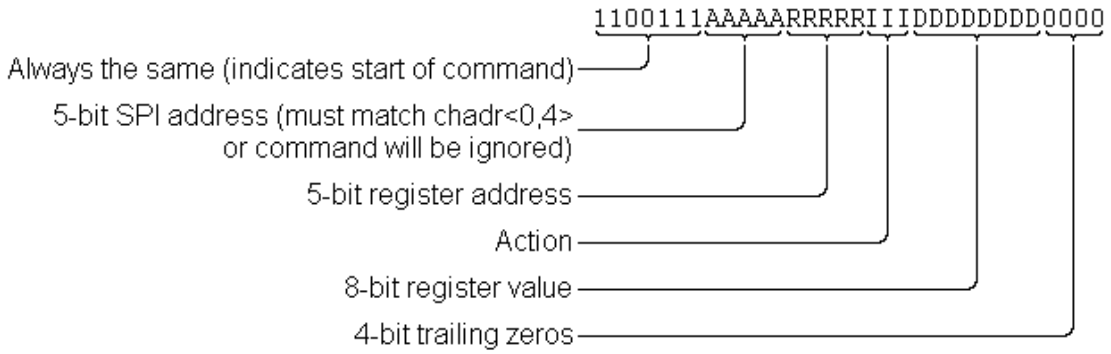



**Figure 6** – Command format.

An 8 bit response is provided by the addressed SPi simultaneosly (actually, the each data bit is changed on the rising edge of `S_CLK`) to data sent in the command word.

- For each group of bits the MS bit is set first
- Data corresponds to data set at the previous matching command (eg sending new shunt voltage command value – response is the previous shunt voltage value).

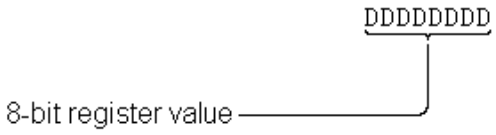



**Figure 7** – Response format.

- There are no “start of data” bits
- There are no check bits.
- There is no way to read an existing value within SPi without changing to a new value.

#### 2.1.1.1 Start of command (header)

The 7 bit bits at the start of each command (the header) are always checked by the SPi. These must be 1100111. If there is no match SPi will igniore the command.

#### 2.1.1.2 Address

The 5 bit address in the command must match the 5 bit address set by the 5 address inputs (pads on SPi). If there is no match the Spi will igniore the command.

#### 2.1.1.3 Register address

The 5 bit register address sets the parameter that will be set or read from SPi. Table 3 lists the registers.

#### 2.1.1.4 Action

3-bit parameter. An action is carried out by the SPi according to Table 2 below. Note that the only useful action in most cercumstances is '001'. There is no 'read' action.

#### 2.1.1.5 Value

An 8-bit parameter is passed to the SPi. This is required even for actions that ignore it.

#### 2.1.1.6 trailing zeros

The last four bits should be zero to ensure a 32 bit command word. These bits are ignored by the SPi.

| Action | Purpose/comment |
|---|---|
| 000 (0 dec) | Not defined |
| 001 (1 dec) | Write to register (data within 32 bit command word) |
| 010 (2 dec) | Set register to 11111111 |
| 011 (3 dec) | Not defined |
| 100 (4 dec) | Not defined |
| 101 (5 dec) | Set register to 00000000 |
| 110 (6 dec) | Set register to default condition |
| 111 (7 dec) | Not defined |

**Table 2** – SPi "actions".

| **s_in (commands)** reg addr:action | **s_out (response)** | **Default register value** | **Purpose/comment** |
|---|---|---|---|
| 00001:001 (1 dec : write) | previous state | X0000011 | 7 of the bits configure direction of the 7 LVDS-like com ports. Default is 2 drivers, 5 receivers. Bit 1 ⇒ A is input, B is output; Bit 0 ⇒ A is output, B is input. |
| 00010:001 (2 dec : write) | previous state | 01100110 | Sets LVDS driver current |
| 00011:001 (3 dec : write) | previous state | 01100110 | Sets LVDS driver current |
| 00100:001 (4 dec : write) | previous state | 01100110 | Sets LVDS driver current |
| 00101:001 (5 dec : write) | previous state | XXXX0110 | Sets LVDS driver current (the most significant 4 bits are not used) |
| 00110:001 (6 dec : write) | previous state | 01100110 | Sets output driver current for LVDS outputs s_out (MS 4 bits) and alarm (LS 4 bits) |
| 00111:001 (7 dec : write) | previous state | 00100101 | Set shunt-regulator voltage range (MS 3 bits - 001). Set shunt voltage (LS 5 bits - 00101) – default 1.5 volts. |
| 01000:001 (8 dec : write) | previous state | XX010010 | Select compensation caps for linear regulators. 3 bits each. |
| 01001:001 (9 dec : write) | previous state | XX101011 | Sets bias values for Linear regulator A LS 6 bits only |
| 01010:001 (10 dec : write) | previous state | XX101011 | Sets bias values for Linear regulator B LS 6 bits only |
| 01011:001 (11 dec : write) | previous state | 00010001 | Set voltage of Linear regulator A & B. Default = 1.2V. |
| 01100:001 (12 dec : write) | previous state | 00000000 | Routes probing current to bus – ie allows external pin output connect to a selected test point (default, 0, = all off). |
| 01101:001 (13 dec : write) | previous state | XX111111 | Sets alarm threshold for linear regulator ADC A |
| 01110:001 (14 dec : write) | previous state | XX111111 | Sets alarm threshold for linear regulator ADC B |
| 01111:001 (15 dec : write) | previous state | XX111111 | Sets alarm threshold for shunt regulator ADC |
| 10000:001 (16 dec : write) | previous state | 00001110 | Set LSB for LinA-ADC (MS 4 bits) and alarm delay for regulator A (LS 4 bits) |
| 10001:001 (17 dec : write) | previous state | 00001110 | Set LSB for LinB-ADC (MS 4 bits) and alarm delay for regulator B (LS 4 bits) |
| 10010:001 (18 dec : write) | previous state | 00001110 | Set LSB for Shunt Regulator current ADC (MS 4 bits) and alarm delay for shunt regulator (LS 4 bits) |
| 10011:001 (19 dec : write) | previous state | 00000000 | "Spare" |
| 10100:001 (20 dec : write) | previous state | 00000000 | "Spare". Data in this register is not used, but may be written to and read from for test purposes. |
| 10101:001 (21 dec : write) | previous state | ? | "Wildcard register" |
| 10110:010 (22 dec : read) | RRRRRR0A | ? | 6 bits ADC A ; 0 ; A alarm. |
| 10111:001 (23 dec : read) | RRRRRR0A | ? | 6 bits ADC B ; 0 ; B alarm. |
| 11000:001 (24 dec : read) | RRRRRR0A | ? | 6 bits ADC shunt ; 0 ; shunt alarm. |
| all other registers | Undefined | Undefined | Undefined |

**Table 3** – SPi registers.

## 2.1.2 Command electronic signals

Commands and data are sent to the SPi using LVDS-like pairs. Figure 8 shows a typical transaction. Figure 9 shows possible interactions with SPi. Note that S_OUT data changes on the rising edge of S_CLK.

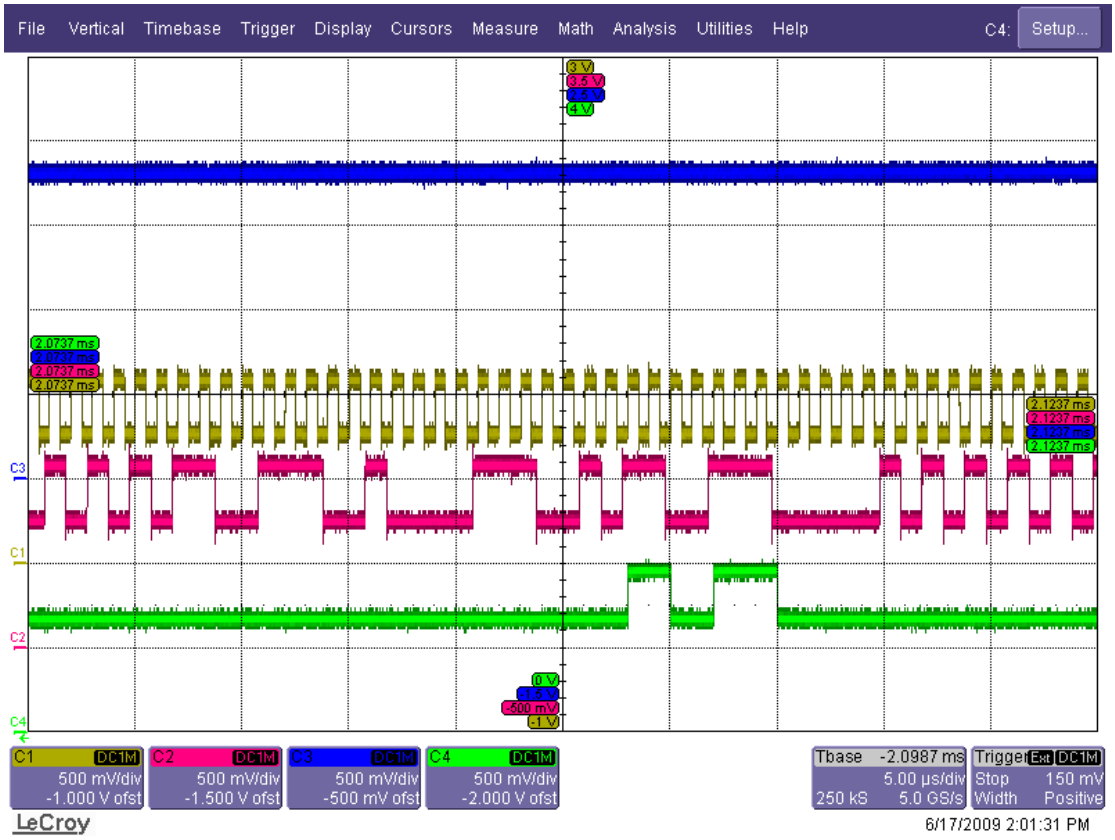



**Figure 8** – A typical command (voltages on SPi pads)
Yellow = S_CLK (1 MHz)
Red = S_IN (note changed only while S_CLK is low)
Green = S_OUT (note changes only on rising edge of S_CLK)
Blue = Vdd

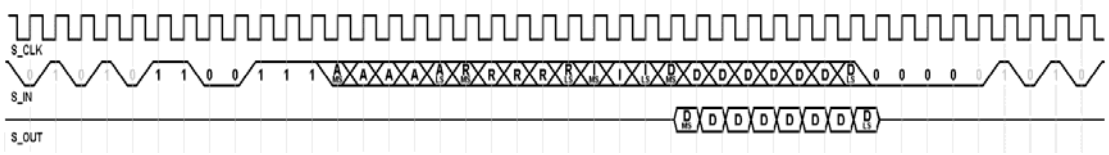



**Figure 9** – Command format
AAAAA = SPi address
RRRRR = SPi register
III = Action
DDDDDDDD = data (value) for SPi

In practice command data has been most reliably sent when the data is changed (one bit to the next) while the clock is low. Data transitions when the clock is high can

occasionally lead to failed reading of data values (although most of the command bits remain active in this case – that is, the command is operated, but values read are wrong).

### 2.1.3 Known problems

Some SPi commands are known to be unrelaible for operating voltages between 2.3 - 2.6V. Notably setting the shunt regulator voltage and setting the COM port directions are known to fail in these circumstances. This problem is under investigation.

# 3 Application

The primary purpose of SPi is to provide the elements of a shunt regulator. These elements can be controlled and used in the following configurations.

## *3.1 Communication*

Electrical connection details for serial communication are provided below.

A multi-drop AC-coupled serial data interface is used to configure and control SPi and allow operating parameters to be read. This means several SPi components can be connected to a single bus (consisting of `S_CLK`, `S_IN`, `S_OUT` and (optionally – see next section) `H_RESET` LVDS-like pairs referenced to the serial powering ground at the constant current power supply). Bus communication inputs to SPi (`S_CLK`, `S_IN` and `H_RESET`) are all identical. Figure 10 shows how these inputs may be connected. Bus communication output from SPi (`S_OUT`) is shown in Figure 11.

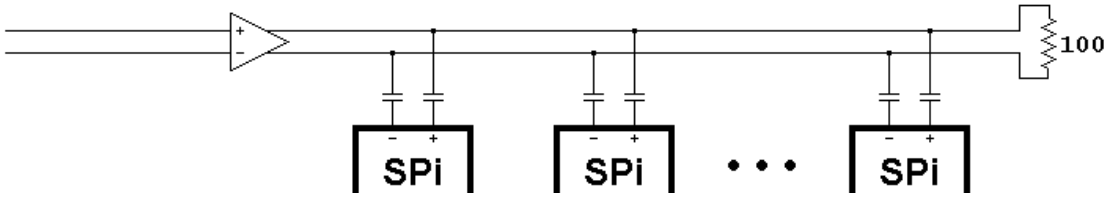



**Figure 10** – SPi command inputs (`S_CLK`, `S_IN` and (optionally) `H_RESET`)

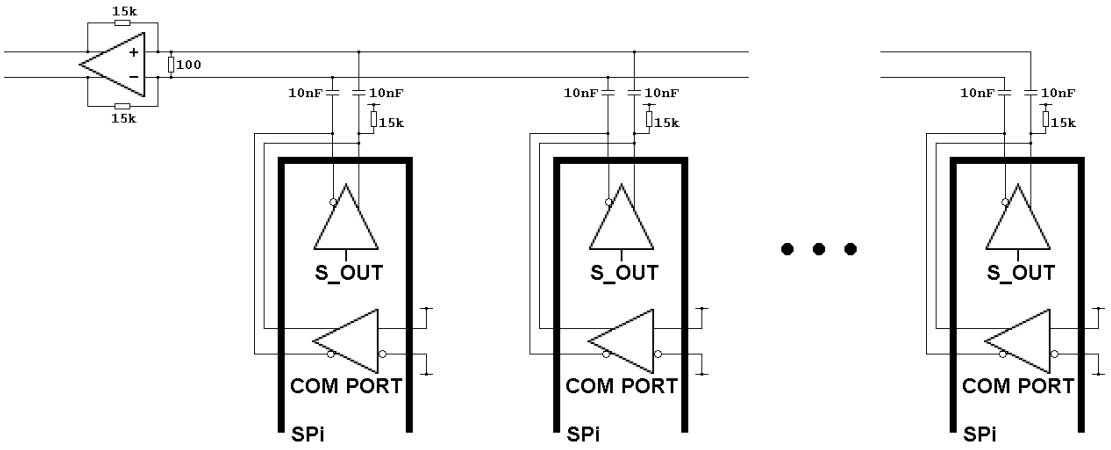



**Figure 11** – SPi command output (`S_OUT`).

## 3.2 Local Reset

SPi is reset by setting RESET+ greater voltage than RESET-. This can be done locally using the circuit in Figure 13. The reset signals are shown in Figure 14. Note that the power supply should reach 1.5 volts within the reset period. The power supply used in testing is ITT model QL355TP, which powers up within about 20ms. Any changes in the operating voltage above 1.5 volts (by changing the digitally controlled voltage regulator for example) will not cause a further reset.

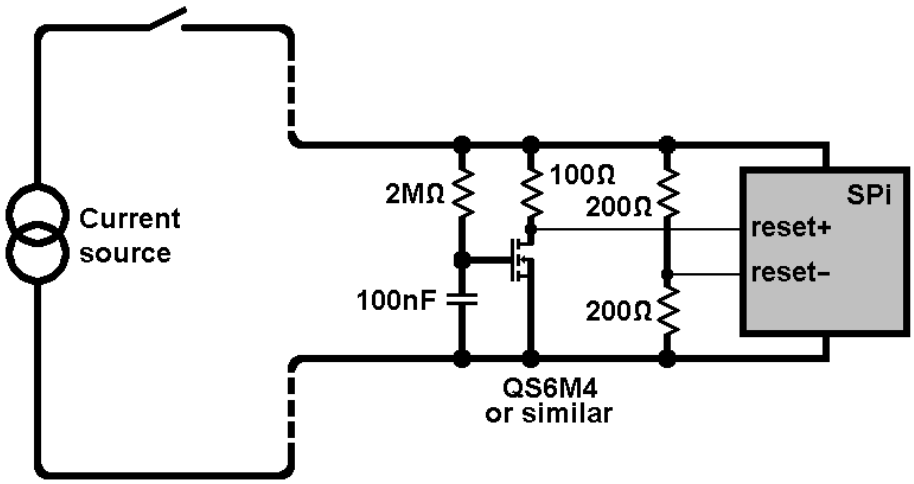



**Figure 13** – Reset circuit

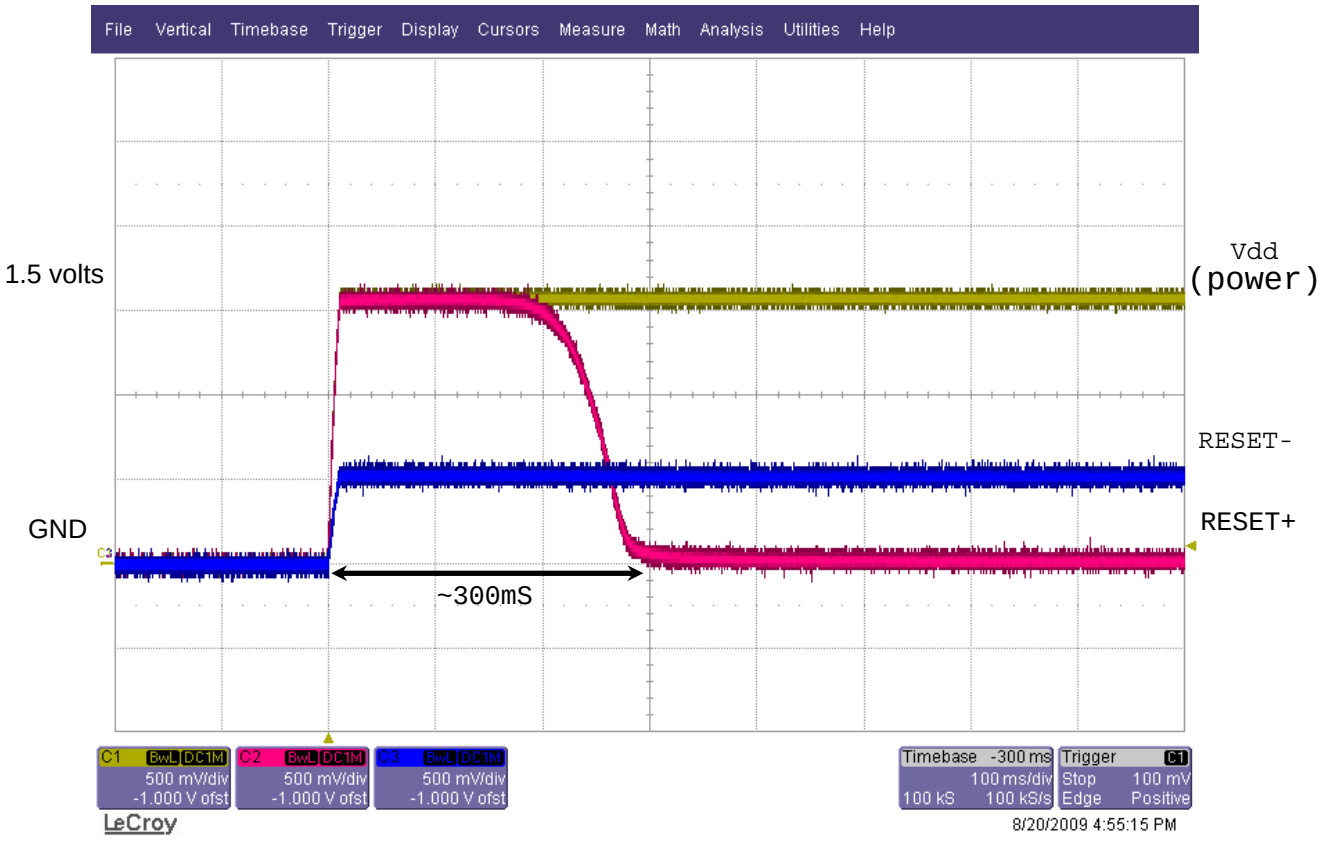



**Figure 14** – A power-up reset cycle.
Measurements taken using internal shunt regulator, current 100 mA.

Yellow = Vdd (power)
Blue = RESET-
Red = RESET+

## 3.3 Internal digital-controlled shunt regulator

SPi can be configured to provide the function of a shunt regulator using an internal transistor and controlled by serial digital command. In this case, shunt regulation heat is dissipated within SPi. By default (no commands given to SPi) SPi will be a 1.5 volt shunt regulator with appropriate wiring.

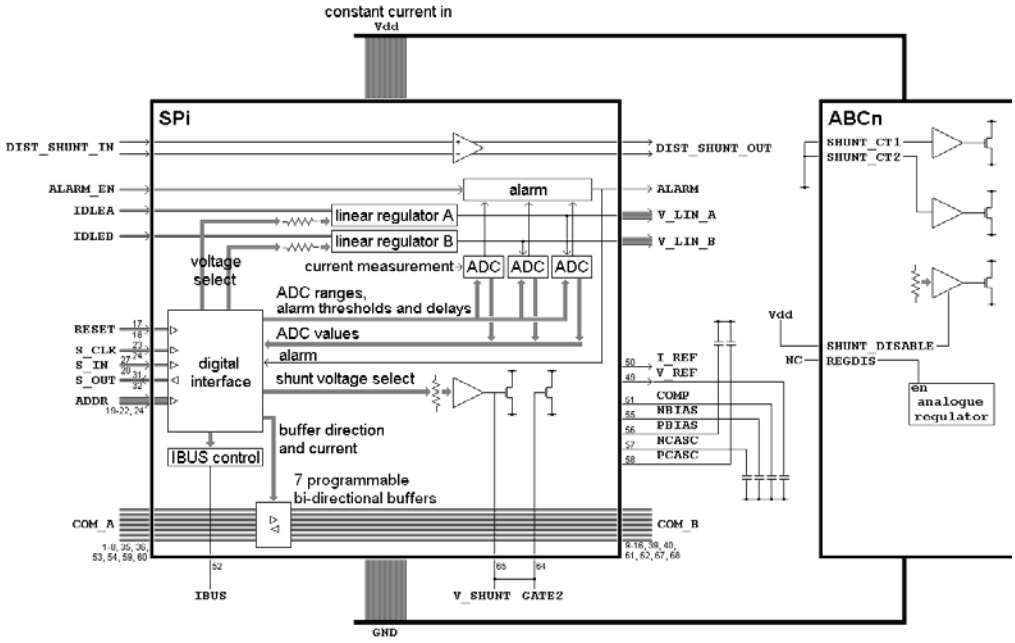



**Figure 13** – Digital internal shunt regulator

## 3.4 Linear shunt regulation with external shunt transistor(s)

SPi can be configured to provide the function of a shunt regulator using an external transistor with the voltage set by fixed external resistors. In this case, shunt regulation heat is not dissipated within SPi. The front-end ASIC ABCn includes transistors for this purpose.

Figure 14 shows a working circuit. Dotted extra components may be needed depending on circuit lay-out. The load (ABCn) can be more than one component in parallel. The internal SPi voltage reference (V_REF) may be used instead of the 1.225 V reference with suitable buffering or it may be possible to use one of the internal linear regulators.

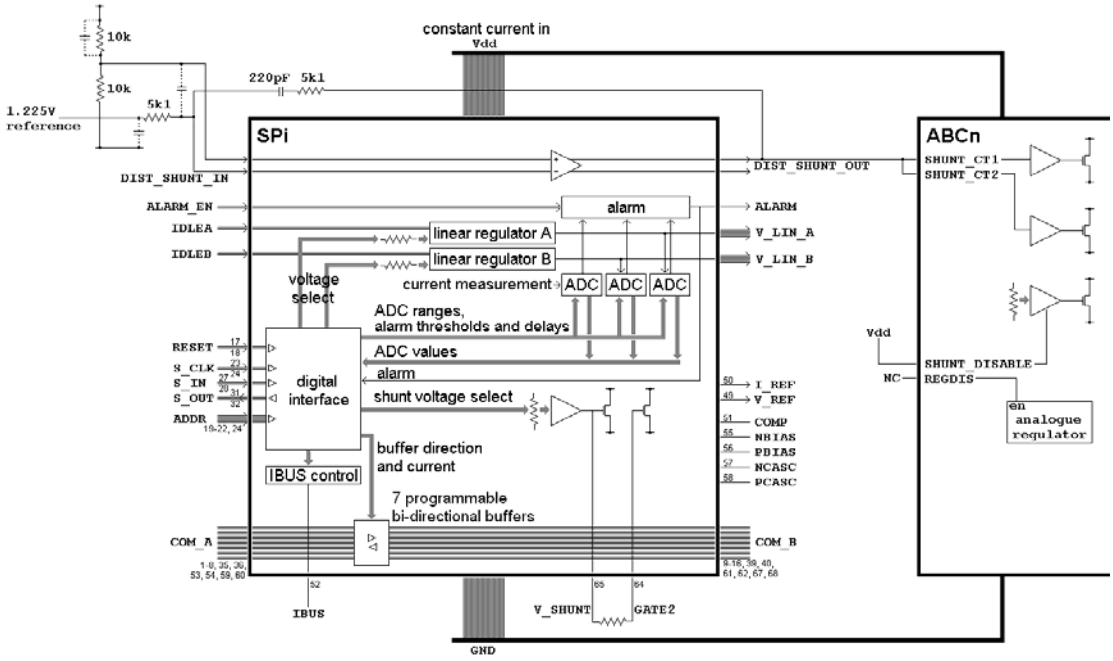



**Figure 14** – External analogue shunt regulator

## *3.5 Linear shunt regulation with internal shunt transistor(s)*

SPi can be configured as above to provide the function of a shunt regulator but using an internal transistor. In this case, shunt regulation heat is dissipated within SPi.

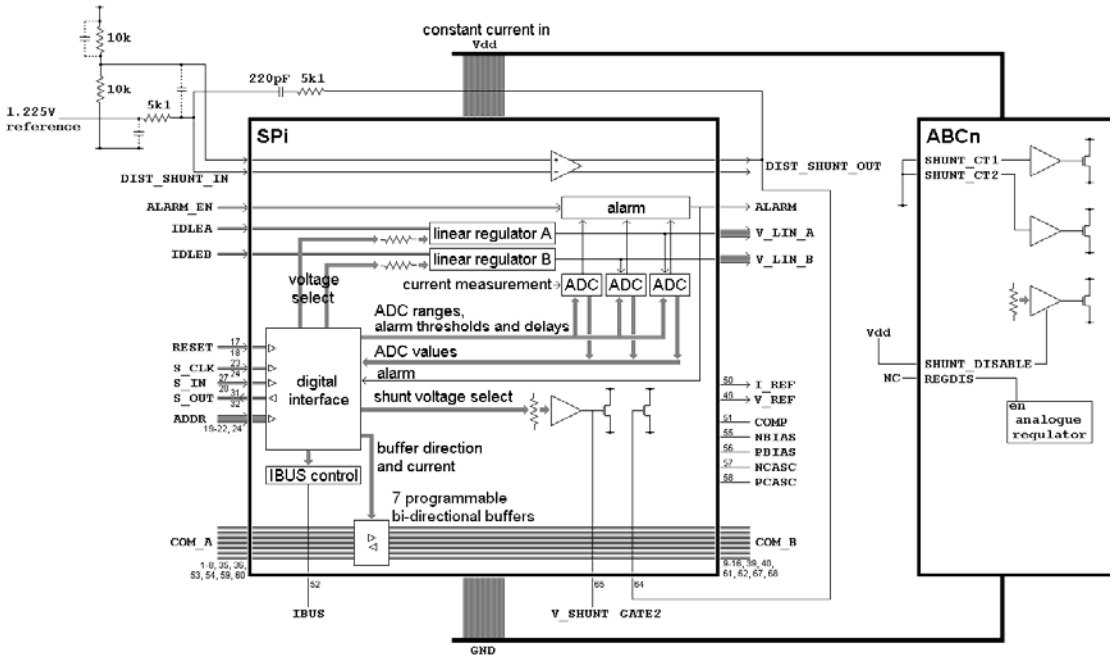



**Figure 15** – Analogue controlled internal shunt regulator

# 4 Functional Components

## 4.1 Digital control and monitoring

SPi includes registers listed in Table 3. For each addressed registester, using action 001 (Table 2), a new 8-bit value is recorded temoporarily and the old value is clocked out, bit by bit, MS bit first. On completion of the last bit (LS bit) the new value is copied into register and this new value chnages SPi operation.

## 4.2 Digital controlled shunt regulator and FETs

The internal digital controlled shunt regulator voltage is set by command 7 (see table 3). The 8 bit value of this command includes 3 bits defining the range and 5 bits setting the voltage within the range.The MS 3 bits of the command value set the voltage range and the LS 5 bits to set the voltage within that range. Note that is possible to set a voltage above the operating voltage of SPi (3 volts) that can damage the device if there is no voltage limitation. It is also possible to set the voltage below the nominal operation voltage range. In this case SPi subsequent behaviour is not defined and SPi should be reset.

| **Command 7 MS 3 bits** | **Volatge range** |
|---|---|
| 010 | Middle voltage range (default) |
| 001 | Low voltage range |
| 100 | High voltage range |

**Table nnn** – Digital controlled shunt regulator voltage range selection.

## 4.3 Amplifier for analogue shunt regulator

This is a simple op-amp with two identiacal output drive circuits. The amplier is powered from the common SPi supply (Vdd and GND). Two independent outputs are provided to allow redundant control of the 2 shunt power dissipation transistors within one ABC-n.

## 4.4 Linear power supplies

The digitally controlled linear power supply outputs can give defined voltage to other front-end components such as the analogue sections within ABC-n which require a lower voltage than the digital sections.

## 4.5 Communication ports

Seven COM ports are provided within SPi. Each has idependantly programmable direction and current. The direction is specified by command (Table 3). Figure 16 shows the default directions.

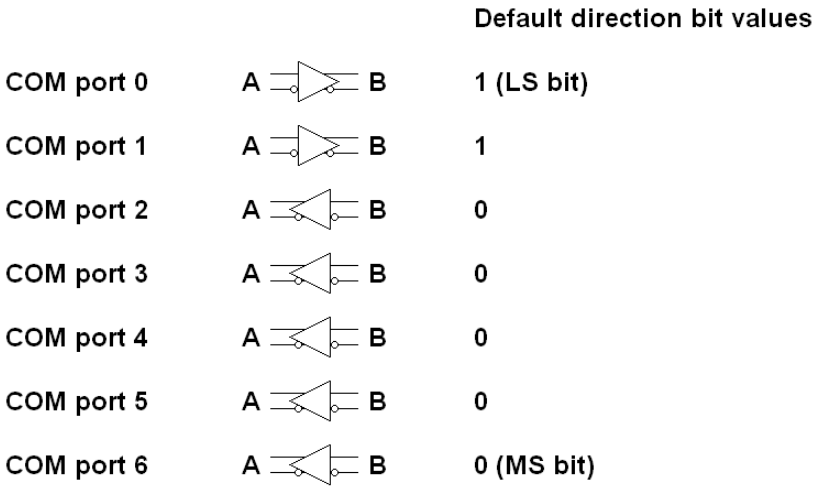



**Figure 16** – COM port directions

### *4.6 ADCs and alarms*

An alarm output is provided. The alarm is set when any one of three currents (shunt current, or either linear regulator output) exceeds a predefined value for a predefined time. The alarm output must be enabled by an external SPi input. The alarm and ADC values can be read through the digital interface. See Table 3.

# 5 Testing

## *5.1 Digital controlled shunt regulator*

Figure 16 shows measured shunt regulator voltage at specified current through the regulator for each command value. One graph is shown for each of the three ranges (see table nnn above). Of the possible 32 voltages within each range, some are repeated values and others excede the working voltage of SPi so should NOT be selected. Figure 16 shows only those voltages that can be reached safely. Note also that there is a problem within SPi that affects setting some parameters when the supply voltage excedes 1.5 volts so command values should be set while at 1.5 volts and the final command value should set the shunt voltage higher if needed.

Figure 17 shows how the read current ADC (command 24) varies with shunt regulator current.

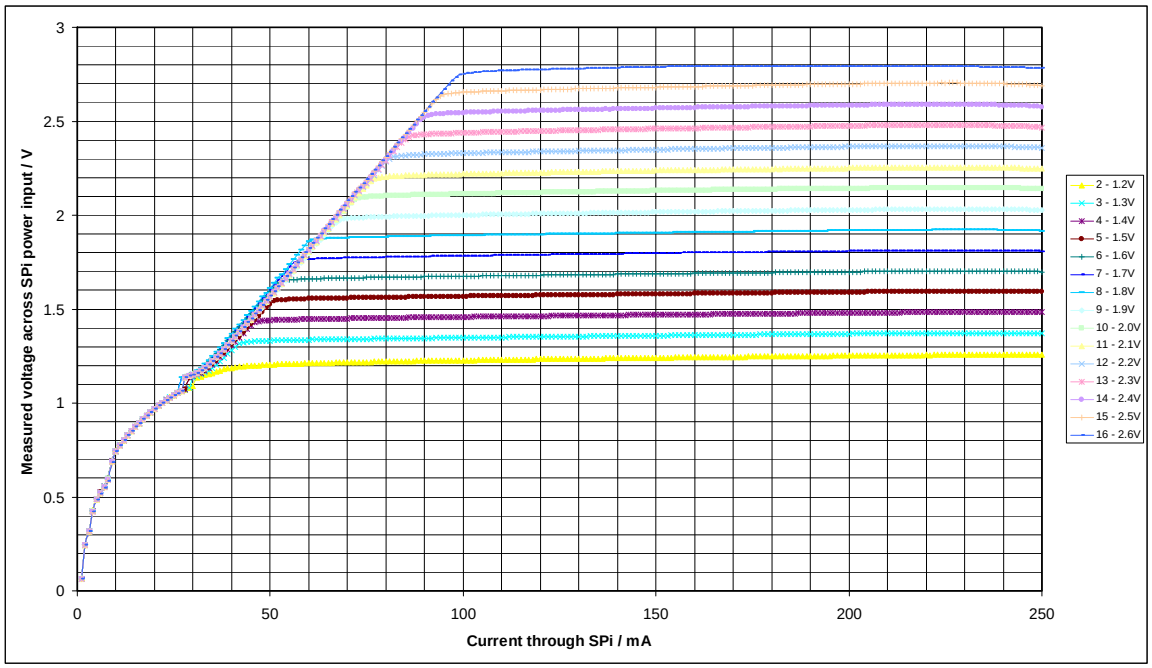



Figure 16a –Middle voltage range
Command 7 MS 3 bits = "010"

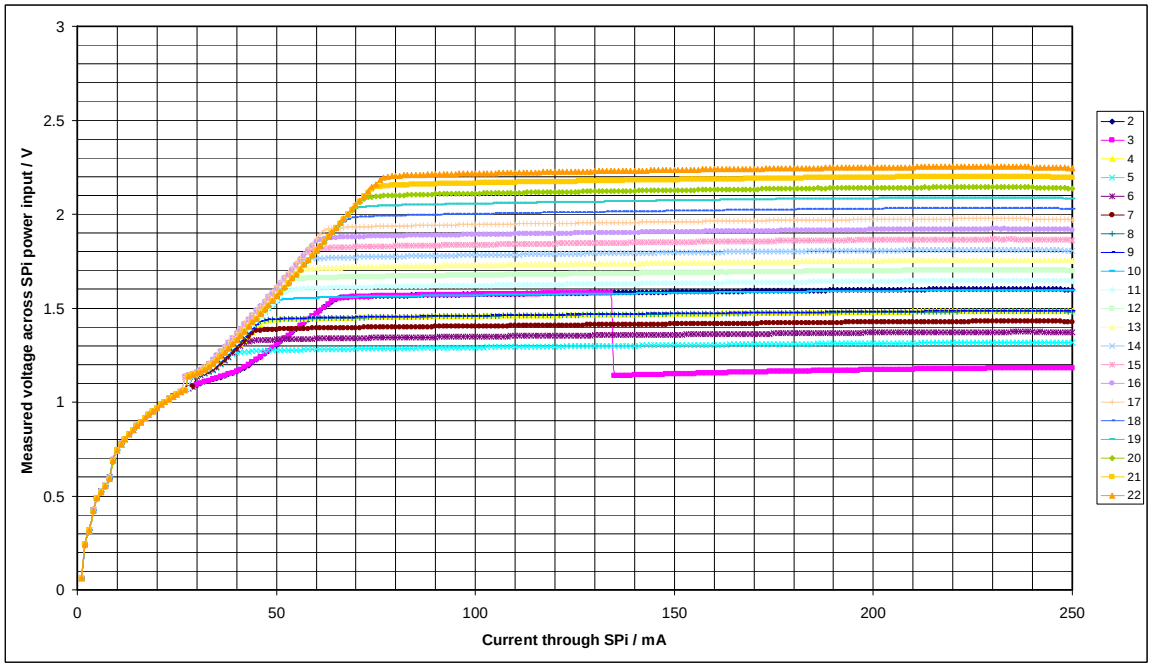



Figure 16b –Low voltage range
Command 7 MS 3 bits = "001"

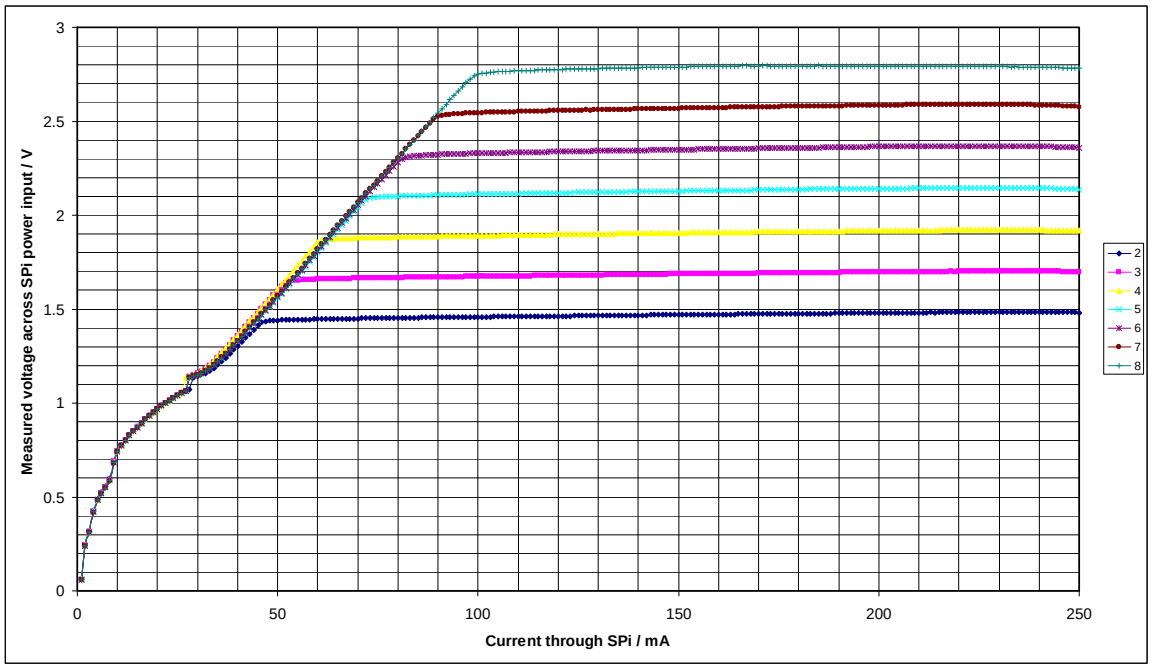



Figure 16c –High voltage range
Command 7 MS 3 bits = "100"

**Figure 16** –Shunt regulator voltage (variation with current)

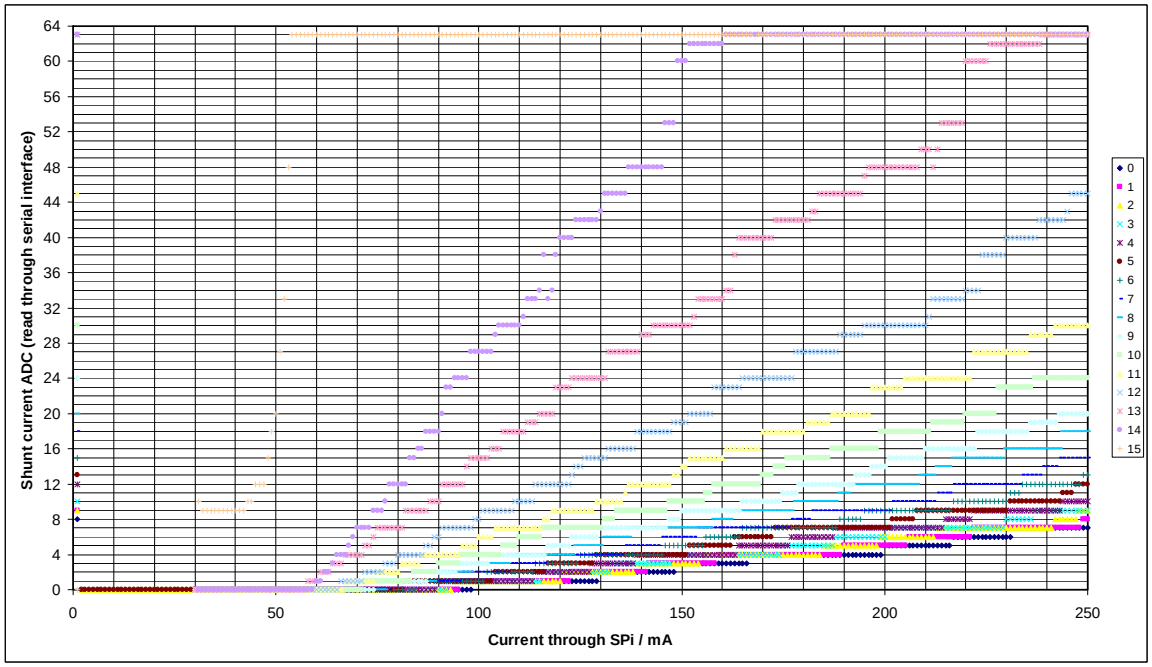



**Figure 17** –Shunt regulator current ADC

## *5.2 V_REF* power supply dependency

V_REF output of SPi is nominally 1.2 volts. Figures 18 shows measured operating parameter for different supply voltages.

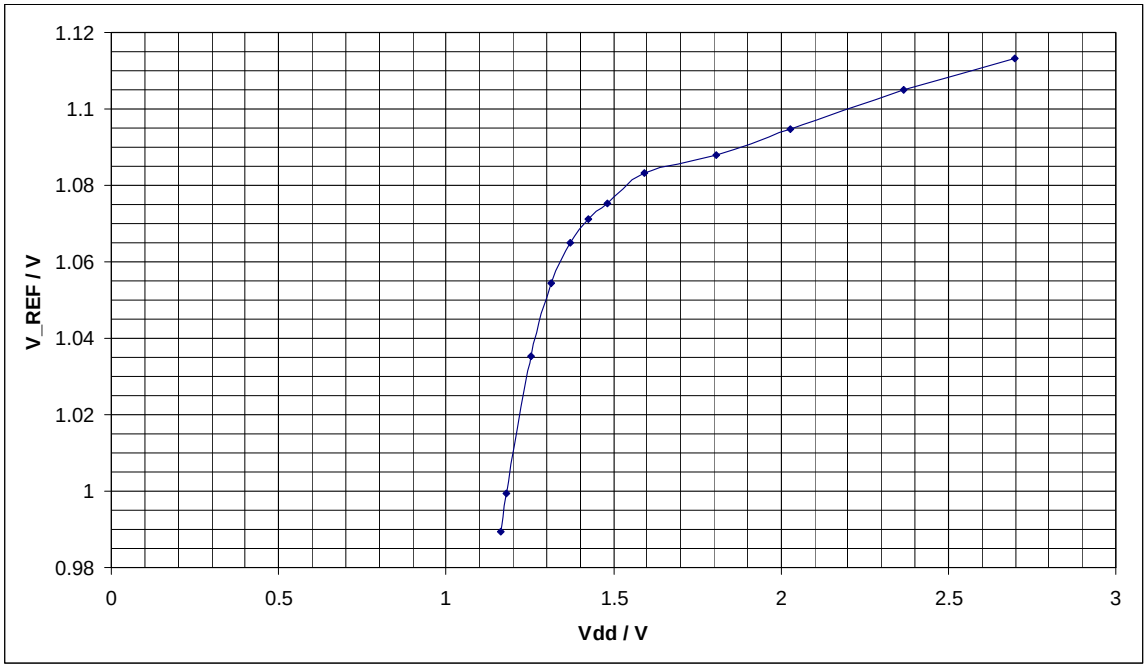



**Figure 18** – V_REF open circuit – variation with VDD.
The digitally controlled shunt regulator is used to select voltages for this test.

## *5.3 Linear regulators*

The internal linear regulator voltages are set (4 bits) by command 9, 10 and 11 (see table 3). Figure 21 show measured operating parameters.

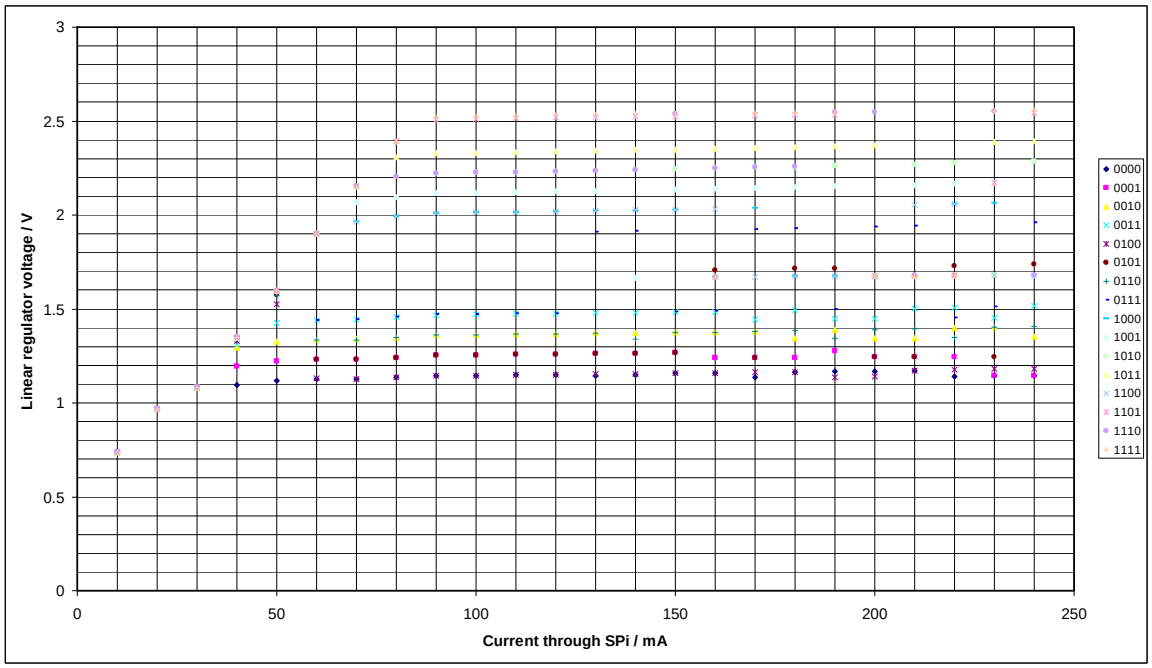



**Figure 21** – Linear regulator output variation with voltage value command.
Default bias

## 5.4 COM ports

The seven COM ports deign is identical. Each is programmed to input from two pads and out put from two pads in a programmed direction (Table 3 command 1), with a programmed drive current (Table 3 commands 2 to 6, 4 bits per port). Each COM port is fully independant and the control ports (`S_CLK`, `S_IN`, `S_OUT` and `RESET`) use the same design, but are fixed direction. Drive current is measured as the current between the output pads with zero ohm load (ie through current meter). This may be used to calculate the equivalent output impedance.

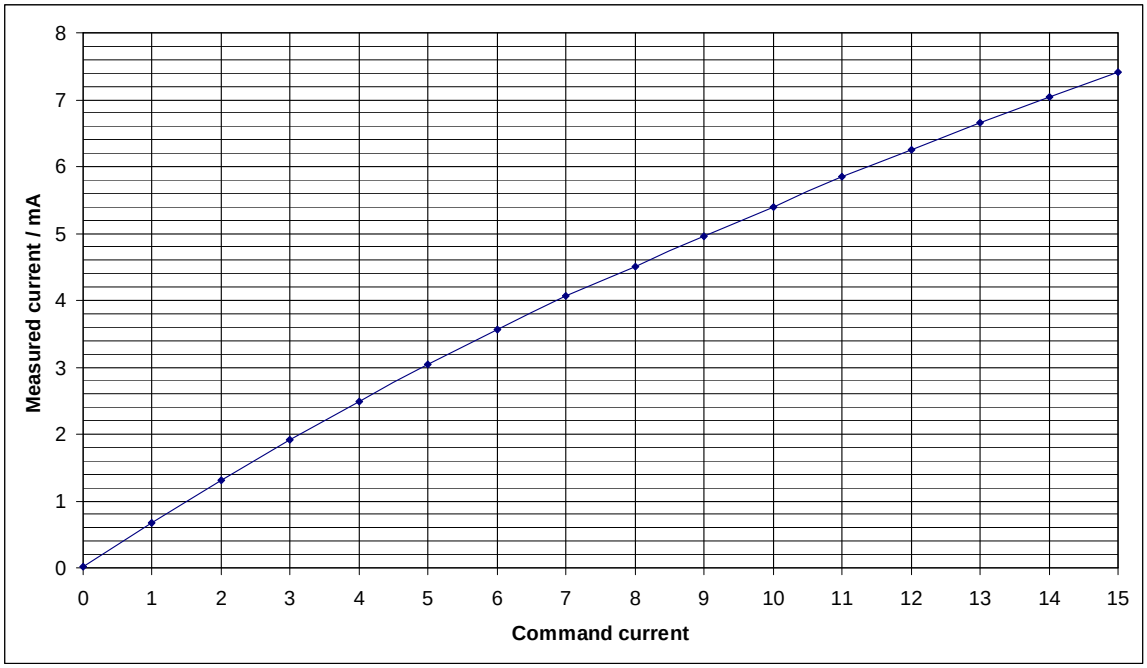



**Figure 22** – COM port drive current.

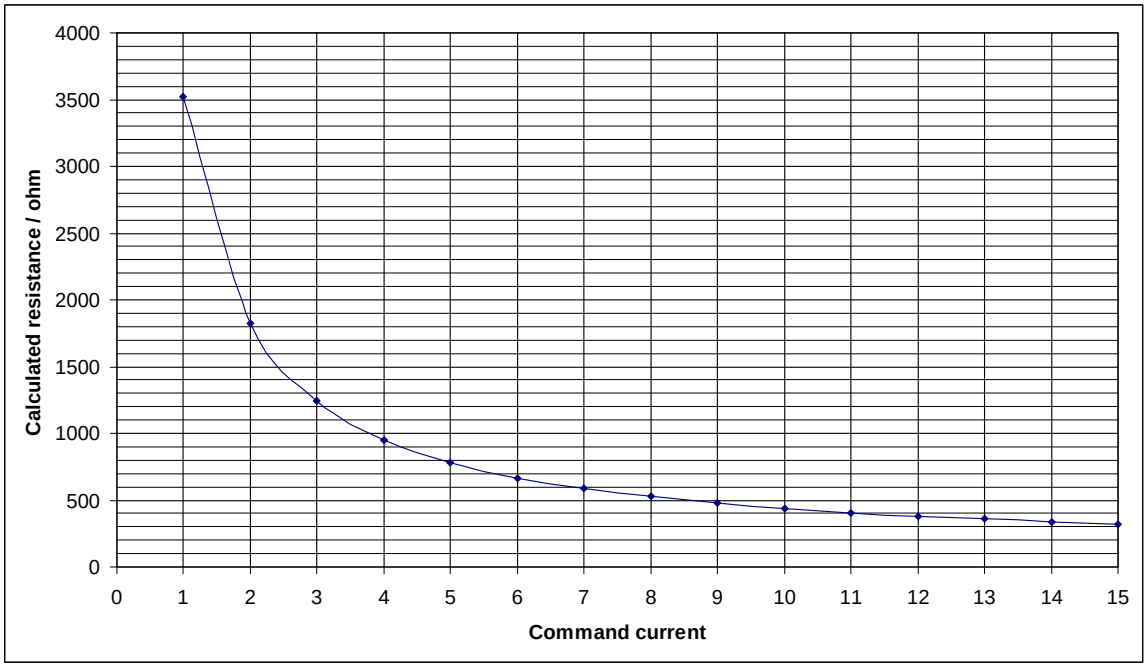



**Figure 23** – COM port impedance.

# 6 Operating parameters

## 6.1 Power

Operating voltage.

Min 1.5V

Max 3.0V

Operating current

Min 30mA (required for internal digital & analogue components)

Max 4A peak (depends upon cooling (power dissipation) and voltage)

In practice, 250mA, air cooled, is no problem.

Note that the shunt regulator can be configured to more than 3 volts, but this voltage must not be applied.

# 7 Block description

## 7.1 Control

Serial SPi interface data is used to configure SPi components and allow operating parameters to be read. A multi-drop serial data configuration has been chosen as the interface, this means several SPi components can be connected to a single bus (consisting of clock, serial-in, h_reset and serial-out LVDS pairs referenced to the serial powering ground at the constant current power supply). This is shown in Figure 2 and, in more detail, in Figure 3. A failure in a single SPi component is unlikely to affect other components on the bus compared to the alternative of a daisy chained control configuration. The penalty is that each SPi on a bus must have a unique identity specified by a chip address. Each SPi has five address bits which are hard-wired externally to define its address. Thus there can be a maximum of $2^5 = 32$ SPis on a single bus (plus one SPi Master). In practise there can be only 30 SPis on a single bus because two addresses (0 and 21 decimal) are assigned a special purpose (see section 6). Serial-in is driven only by the SPi Master and there is a single LVDS termination resistance at the far end of the multi-drop pair (not shown in diagrams 2 and 3). Serial-out may be driven by any SPi on the bus and has a single termination resistance at the SPi Master. When a command is issued by the SPi Master only the one addressed SPi can reply to the command so there is no chance of bus contention. (But note that every SPi will respond to address 00000). Thus normal operation will be for the controller to poll the connected SPis periodically to check the status. A SPi will not send information unless commanded to do so by the controller.

All parameters sent through the serial links are in binary notation. Most significant bit first, least significant bit last.

Electrically, positive data outputs are normally low, with high going level indicating “1” and low indicating “0”. The clock is generated by the SPi Master and may be run continuously or only when data is to be clocked and is a simple square wave. Serial data may be set on the falling edge of the clock and is read on the rising edge by SPi.

## 7.2 Linear regulators

There are two identical linear regulators within the chip, referred to as A and B. See figure 6. Each linear regulator

- has an output available externally - this is not used within the chip.
- has an associated ADC measuring the regulator current that can be read by the controller which in turn can be read by the SPi Master.
- is separately programmable to provide one of 16 pre-set output voltages, each with a 16 level (4 bit) fine adjustment.
- has an idle input (available externally on the chip) – when set to idle, the output is undefined and the regulator is disabled.
- has a programmable alarm level. The status of this alarm can be read by the controller and reported to the SPi Master.

The alarm line output from the ADC goes only to the controller. This can be read by the SPi Master, but no action is taken within the SPi chip and the line is not available externally. The alarm does not latch, but there is a programmable delay between over-current and raising the alarm.

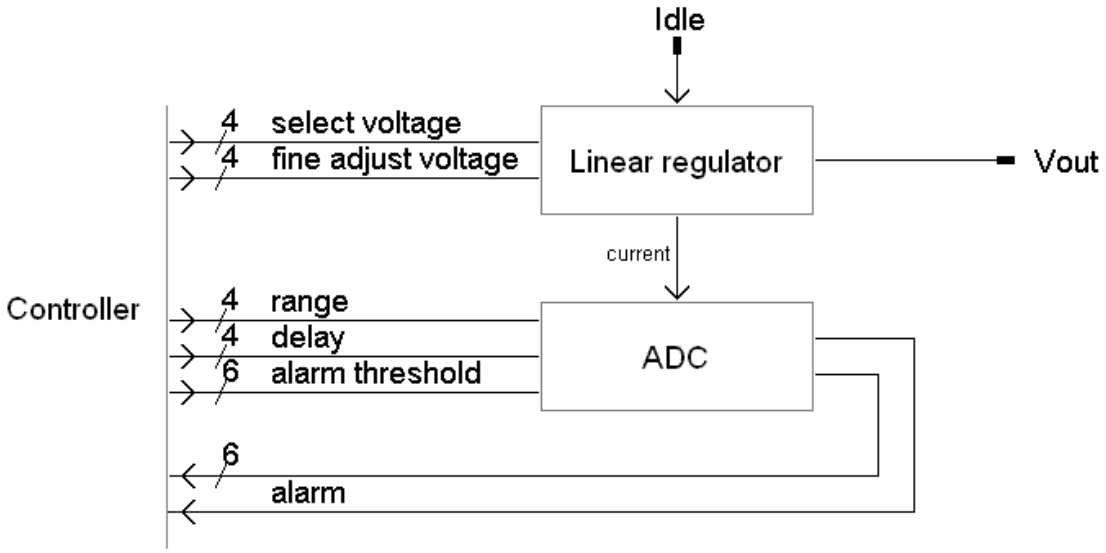



**Figure 6** – Linear regulator.
Simplified names. Voltage references and select lines omitted for clarity.

## 7.3 Shunt regulators

The main shunt regulator can be programmed to set a voltage for front-end components.

Front-end components can be protected from damage by a trip voltage sense. Note that if the current exceeds the trip value, voltage to the read-out chips will be collapsed (and also to the SPi). In this event the constant current through the SPi will remain and will continue to provide power to other SPis in the serial powering chain, but there will be less power consumed by the tripped SPi.

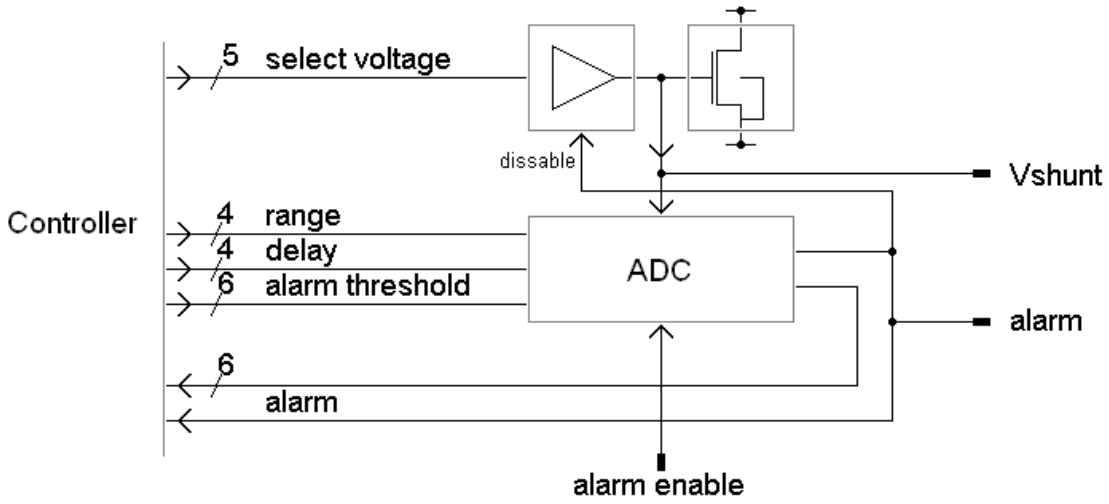



**Figure 7** – Shunt regulator.
Simplified names. Voltage references and select lines omitted for clarity.

Note that the internal shunt transistor cannot be disabled. In order to use external shunt regulation, the internal shunt regulator should be set to its highest voltage or the line Vshunt should be tied low. When using an external shunt regulator, the internal alarm will not be used because the internal shunt regulator is not active.

# 8 Appendix

## *8.1 SPi pad positions*

SPi pad positions are listed below. In each case, the position of the centre is shown, with respect to pad 1.

| pad number | x | y |
|---|---|---|
| 1 | 0 | 0 |
| 2 | 0 | 325 |
| 3 | 0 | 750 |
| 4 | 0 | 1075 |
| 5 | 0 | 1400.02 |
| 6 | 0 | 1725.02 |
| 7 | 0 | 2150 |
| 8 | 0 | 2475 |
| 9 | 325 | 0 |
| 10 | 325 | 325 |
| 11 | 325 | 750 |
| 12 | 325 | 1075 |
| 13 | 325 | 1400.02 |
| 14 | 325 | 1725.02 |
| 15 | 325 | 2150 |
| 16 | 325 | 2475 |
| 17 | 650 | 0 |
| 18 | 650 | 325 |
| 19 | 650 | 750 |
| 20 | 650 | 1075 |
| 21 | 650 | 1400.02 |
| 22 | 650 | 1725.02 |
| 23 | 650 | 2150 |
| 24 | 650 | 2475 |
| 25 | 975 | 0 |
| 26 | 975 | 325 |
| 27 | 975 | 2150 |
| 28 | 975 | 2475 |
| 29 | 1300 | 0 |
| 30 | 1300 | 325 |
| 31 | 1300 | 2150 |
| 32 | 1300 | 2475 |
| 33 | 1625 | 0 |
| 34 | 1625 | 325 |
| 35 | 1625 | 2150 |
| 36 | 1625 | 2475 |
| 37 | 1950 | 0 |
| 38 | 1950 | 325 |
| 39 | 1950 | 2150 |
| 40 | 1950 | 2475 |
| 41 | 2275 | 0 |
| 42 | 2275 | 325 |
| 43 | 2275 | 2150 |
| 44 | 2275 | 2475 |
| 45 | 2600 | 0 |
| 46 | 2600 | 325 |
| 47 | 2600 | 2150 |
| 48 | 2600 | 2475 |
| 49 | 2925 | 0 |
| 50 | 2925 | 325 |
| 51 | 2925 | 2150 |
| 52 | 2925 | 2475 |
| 53 | 3250 | 0 |
| 54 | 3250 | 325 |
| 55 | 3250 | 750 |
| 56 | 3250 | 1075 |
| 57 | 3250 | 1400.02 |
| 58 | 3250 | 1725.02 |
| 59 | 3250 | 2150 |
| 60 | 3250 | 2475 |
| 61 | 3575 | 0 |
| 62 | 3575 | 325 |
| 63 | 3575 | 750 |
| 64 | 3575 | 1075 |
| 65 | 3575 | 1400.02 |
| 66 | 3575 | 1725.02 |
| 67 | 3575 | 2150 |
| 68 | 3575 | 2475 |
| 1a | 3900 | 95 |
| 1b | 3900 | 323.5 |
| 1c | 3900 | 552 |
| 1d | 3900 | 780.5 |
| 1e | 3900 | 1009 |
| 1f | | |
| 1g | 3900 | 1466 |
| 1h | 3900 | 1694.5 |
| 1i | 3900 | 1923 |
| 1j | 3900 | 2151.5 |
| 1k | 3900 | 2380 |
| 2a | 4150 | 95 |
| 2b | 4150 | 323.5 |
| 2c | 4150 | 552 |
| 2d | 4150 | 780.5 |
| 2e | 4150 | 1009 |
| 2f | 4150 | 1237.5 |
| 2g | 4150 | 1466 |
| 2h | 4150 | 1694.5 |
| 2i | 4150 | 1923 |
| 2j | 4150 | 2151.5 |
| 2k | 4150 | 2380 |
| 3a | 4400 | 95 |
| 3b | 4400 | 323.5 |

| | | |
|---|---|---|
| 3c | 4400 | 552 |
| 3d | 4400 | 780.5 |
| 3e | 4400 | 1009 |
| 3f | 4400 | 1237.5 |
| 3g | 4400 | 1466 |
| 3h | 4400 | 1694.5 |
| 3i | 4400 | 1923 |
| 3j | 4400 | 2151.5 |
| 3k | 4400 | 2380 |
| 4a | 4650 | 95 |
| 4b | 4650 | 323.5 |
| 4c | 4650 | 552 |
| 4d | 4650 | 780.5 |
| 4e | 4650 | 1009 |
| 4f | 4650 | 1237.5 |
| 4g | 4650 | 1466 |
| 4h | 4650 | 1694.5 |
| 4i | 4650 | 1923 |
| 4j | 4650 | 2151.5 |
| 4k | 4650 | 2380 |
| 5a | 4900 | 95 |
| 5b | 4900 | 323.5 |
| 5c | 4900 | 552 |
| 5d | 4900 | 780.5 |
| 5e | 4900 | 1009 |
| 5f | 4900 | 1237.5 |

| | | |
|---|---|---|
| 5g | 4900 | 1466 |
| 5h | 4900 | 1694.5 |
| 5i | 4900 | 1923 |
| 5j | 4900 | 2151.5 |
| 5k | 4900 | 2380 |
| 6a | 5150 | 95 |
| 6b | 5150 | 323.5 |
| 6c | 5150 | 552 |
| 6d | 5150 | 780.5 |
| 6e | 5150 | 1009 |
| 6f | 5150 | 1237.5 |
| 6g | 5150 | 1466 |
| 6h | 5150 | 1694.5 |
| 6i | 5150 | 1923 |
| 6j | 5150 | 2151.5 |
| 6k | 5150 | 2380 |
| 7a | 5400 | 95 |
| 7b | 5400 | 323.5 |
| 7c | 5400 | 552 |
| 7d | 5400 | 780.5 |
| 7e | 5400 | 1009 |
| 7f | 5400 | 1237.5 |
| 7g | 5400 | 1466 |
| 7h | 5400 | 1694.5 |
| 7i | 5400 | 1923 |
| 7j | 5400 | 2151.5 |

| | | |
|---|---|---|
| 7k | 5400 | 2380 |
| Dummy pads | 1085.91 | 732.83 |
| | 1085.91 | 992.83 |
| | 1085.91 | 1252.83 |
| | 1085.91 | 1512.83 |
| | 1085.91 | 1772.83 |
| | 1410.91 | 732.83 |
| | 1410.91 | 992.83 |
| | 1410.91 | 1252.83 |
| | 1410.91 | 1512.83 |
| | 1410.91 | 1772.83 |
| | 1735.91 | 732.83 |
| | 1735.91 | 992.83 |
| | 1735.91 | 1252.83 |
| | 1735.91 | 1512.83 |
| | 1735.91 | 1772.83 |
| | | |
| | | |
| | 1220.09 | 1384.06 |
| Alignment marks | 1220.09 | 1124.06 |
| | 5465.09 | -95.94 |

**Table 1** – Pad positions

## *8.2 Test environment*

### 8.2.1 SPi Daughter (SPiD) PCB

Red is the “top” view – this is the side that SPi will be bonded to and will be visible when fitted to the bigger test PCB. Drawings in this section are mirror image of manufactured PCBs and are presented this way to be consistent with supplied information and diagrams previously shown in this document. Hence top copper layer has mirror image text. Bottom copper is as viewed through the PCB and so does not appear mirrored here.

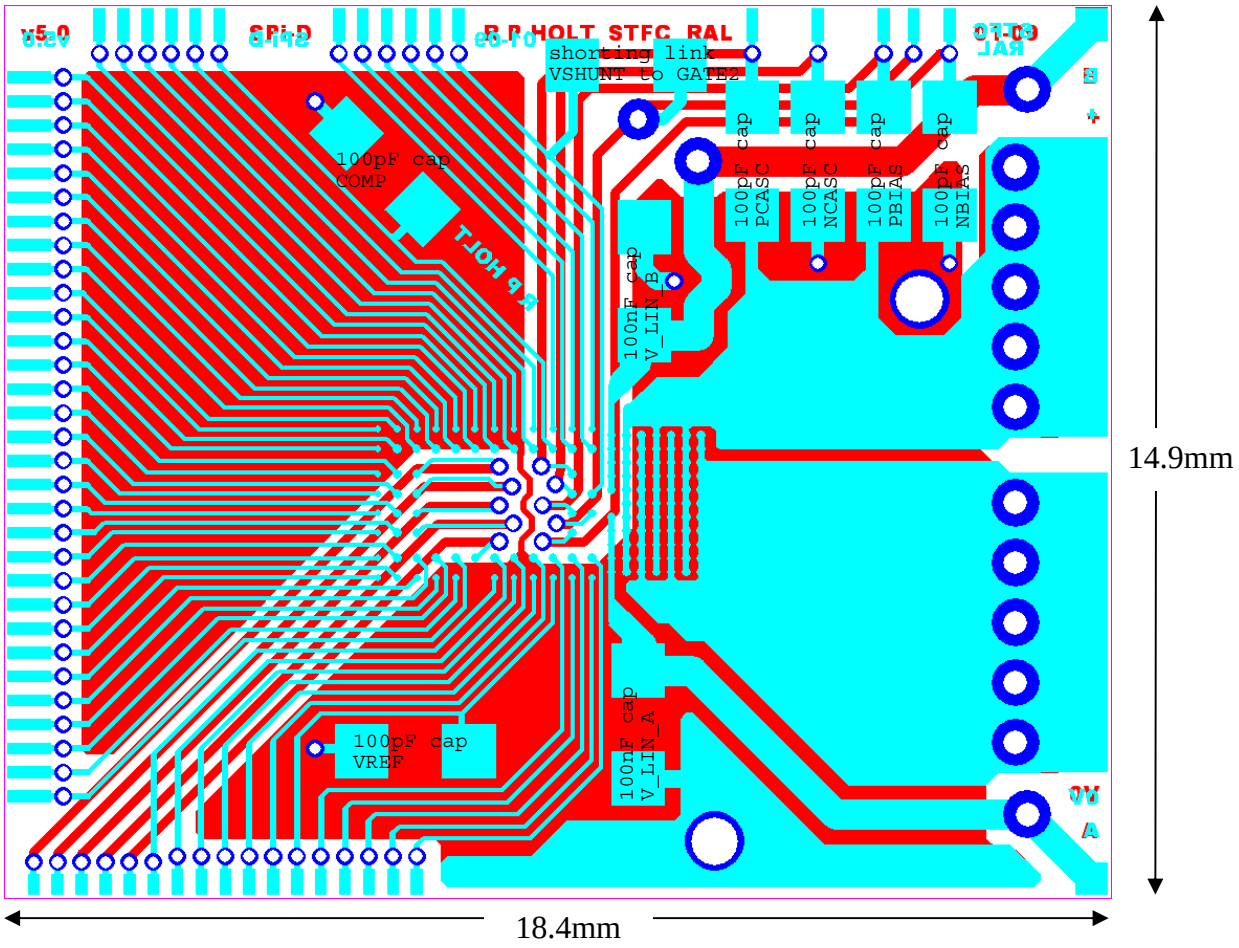
Daughter PCB is designed to enable wire-bonding OR soldering to Mother Board.

Thin PCBs will be used to maximise heat transfer to a cooling plate for higher current tests.

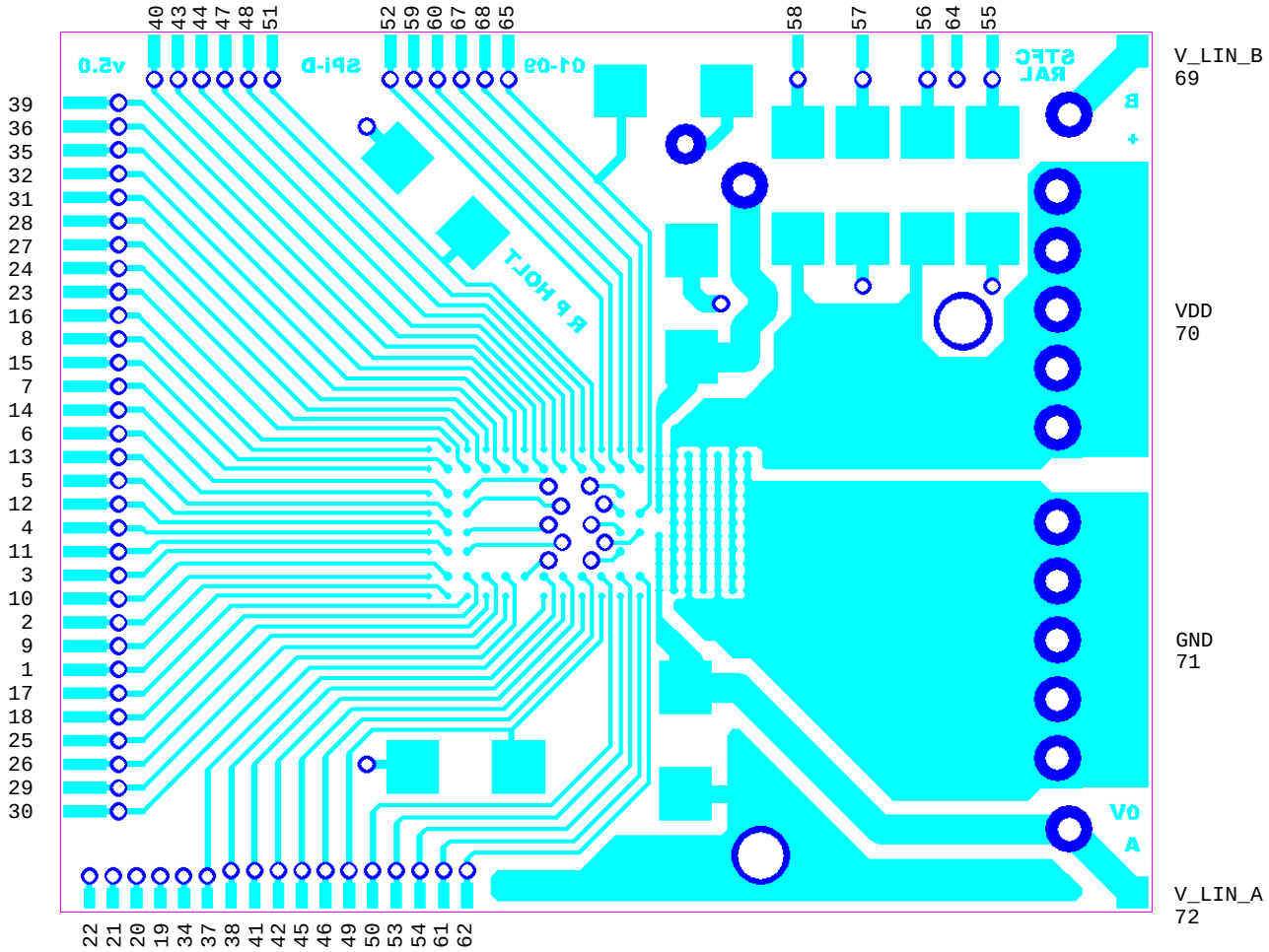
Decoupling cap pads are 900μm square, 200μm separation, suitable for 0805 size components. Small wire-bond pads are 200μm wide, 200μm separation.

Solder mask (top PCB side) is not shown.

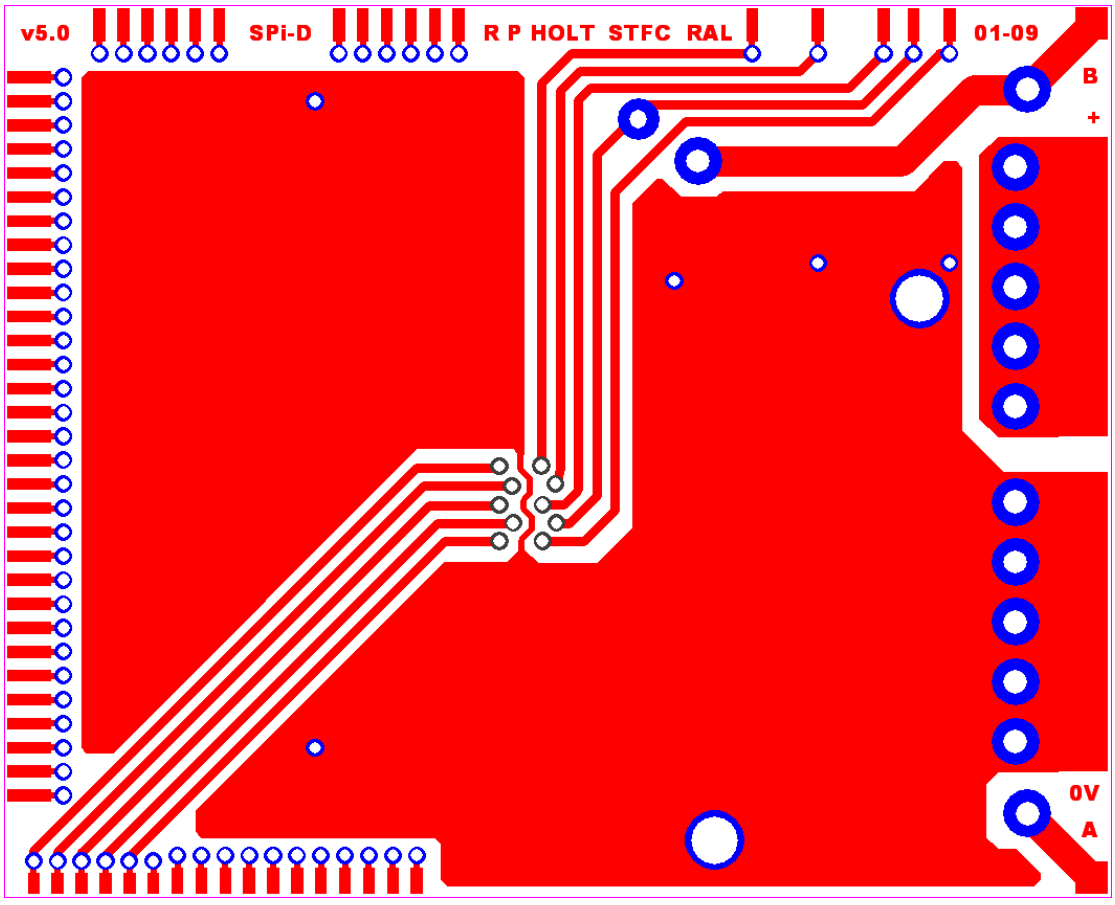
All copper layers *(Note: this is mirror image to manufactured PCB)*



Top copper

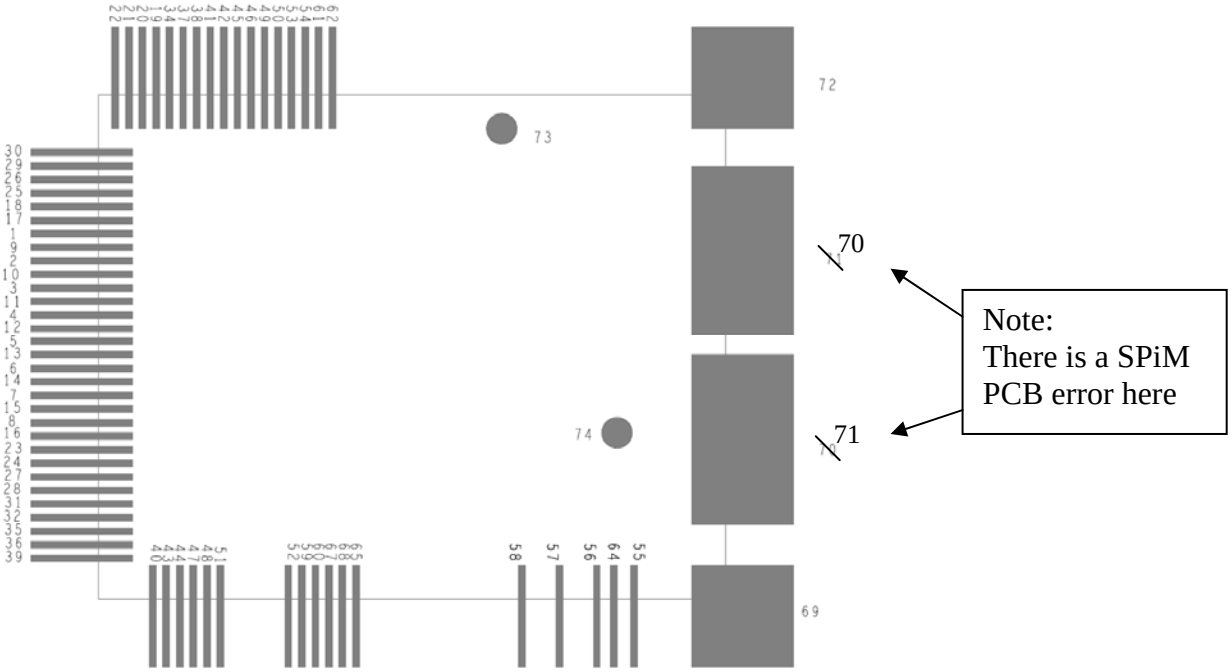


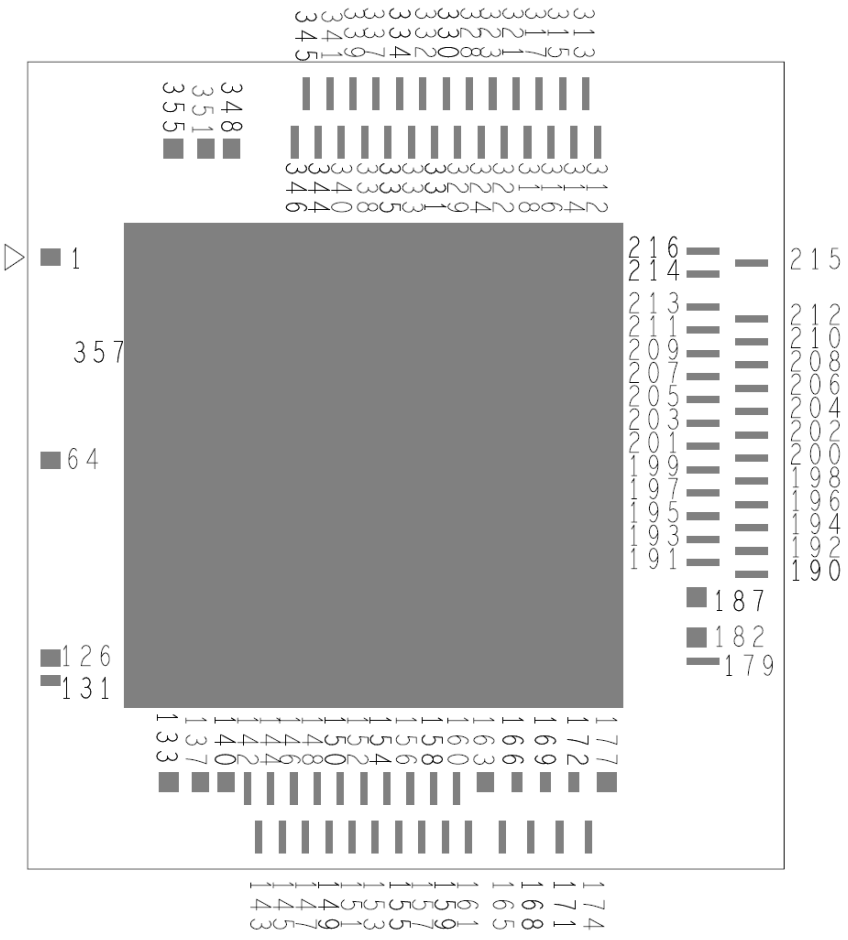

Bottom copper



## 8.2.2 SPi Mother (SPiM) PCB

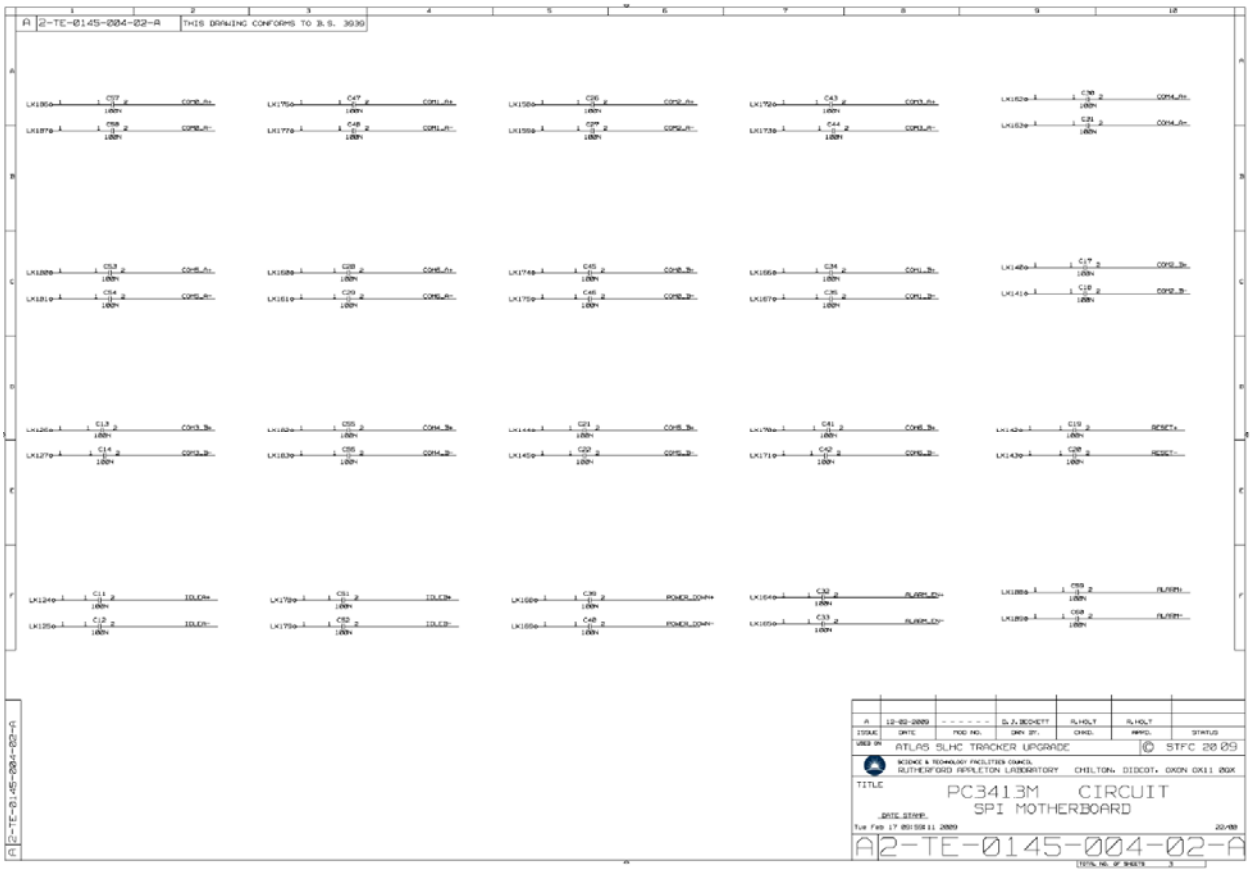
Information supplied through PCB designer (note: this is *NOT* mirror image)



ABCn footprint for SPiM

# Schematic


A2-TE-0145-004-02-A
THIS DRAWING CONFORMS TO B.S. 3939
ATLAS SLHC TRACKER UPGRADE
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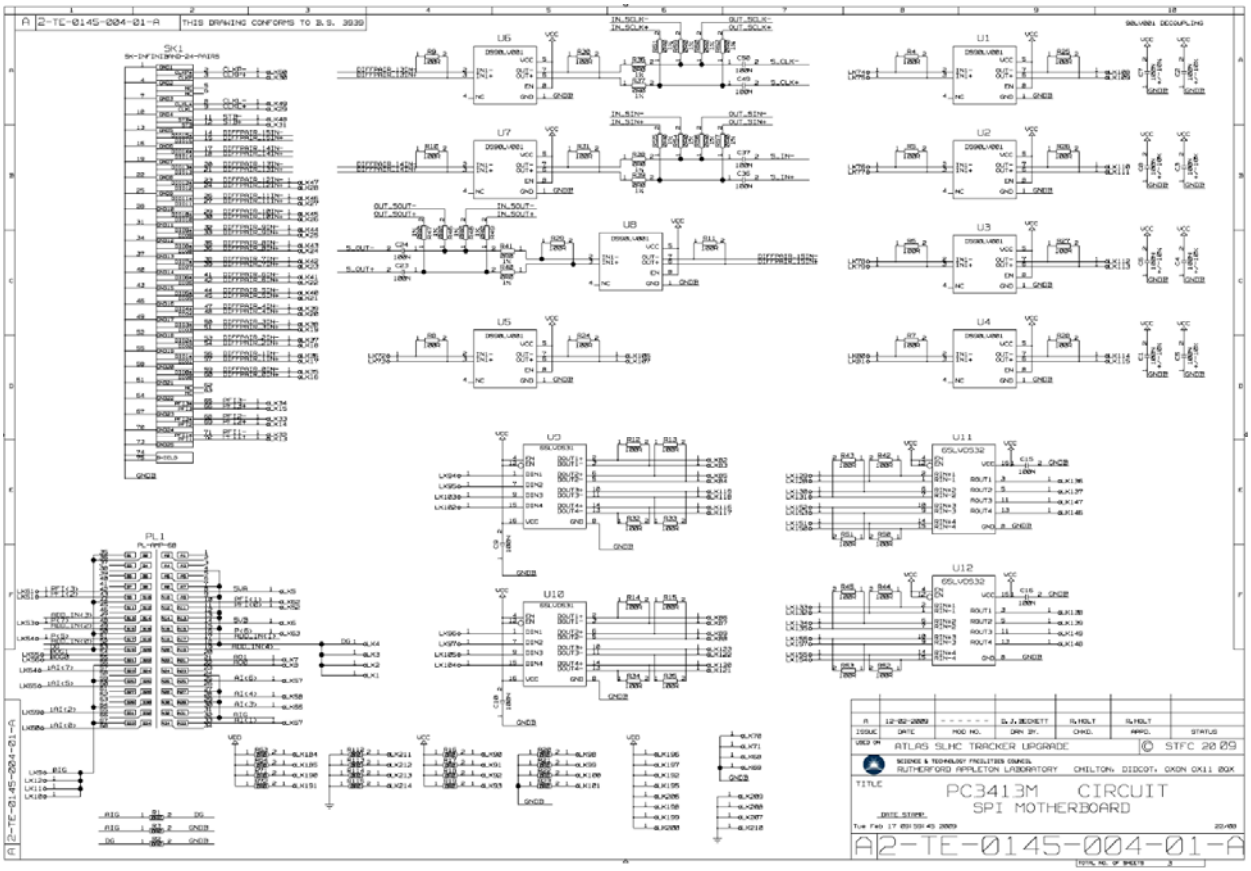
SCIENCE & TECHNOLOGY FACILITIES COUNCIL
RUTHERFORD APPLETON LABORATORY CHILTON, DIDCOT, OXON OX11 0QX
TITLE
PC3413M CIRCUIT
SPI MOTHERBOARD
A2-TE-0145-004-02-A


A2-TE-0145-004-01-A
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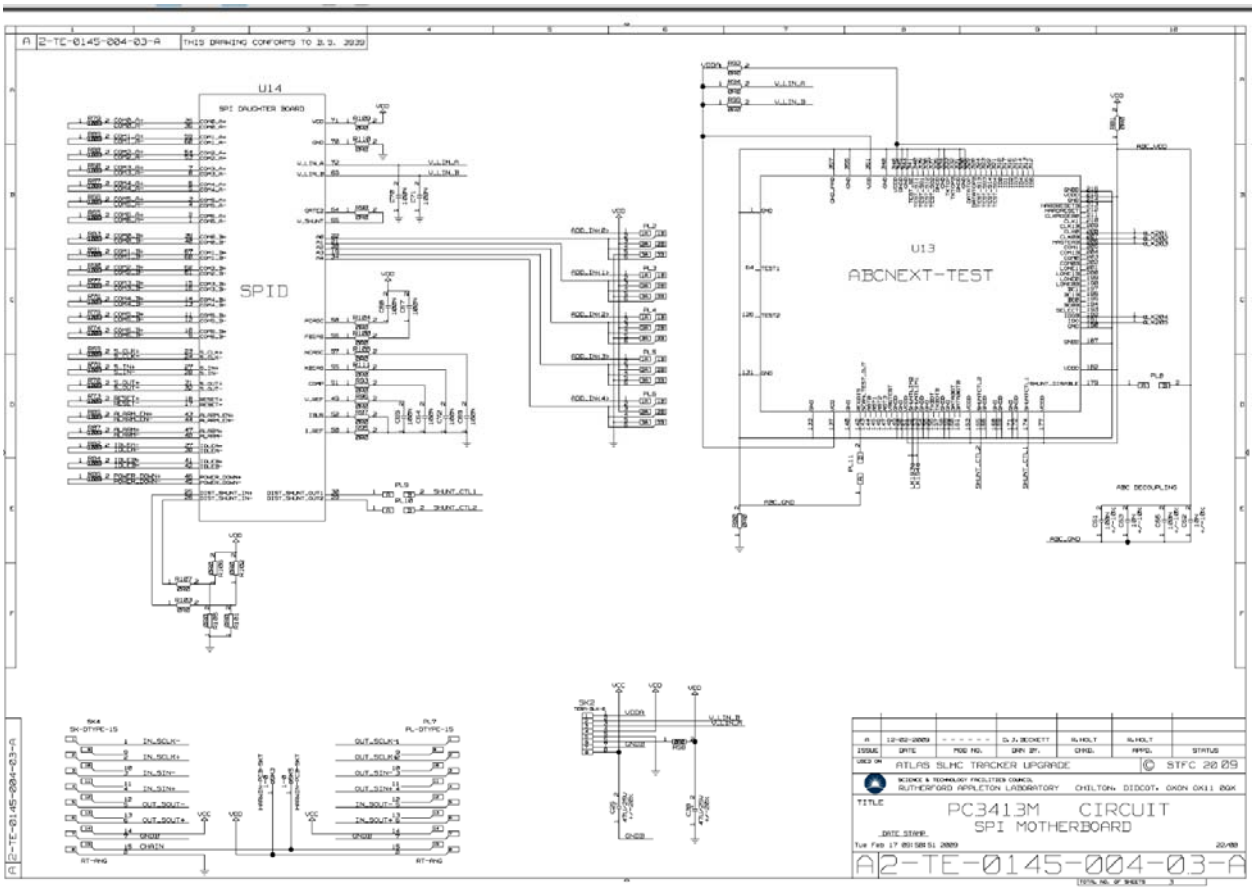
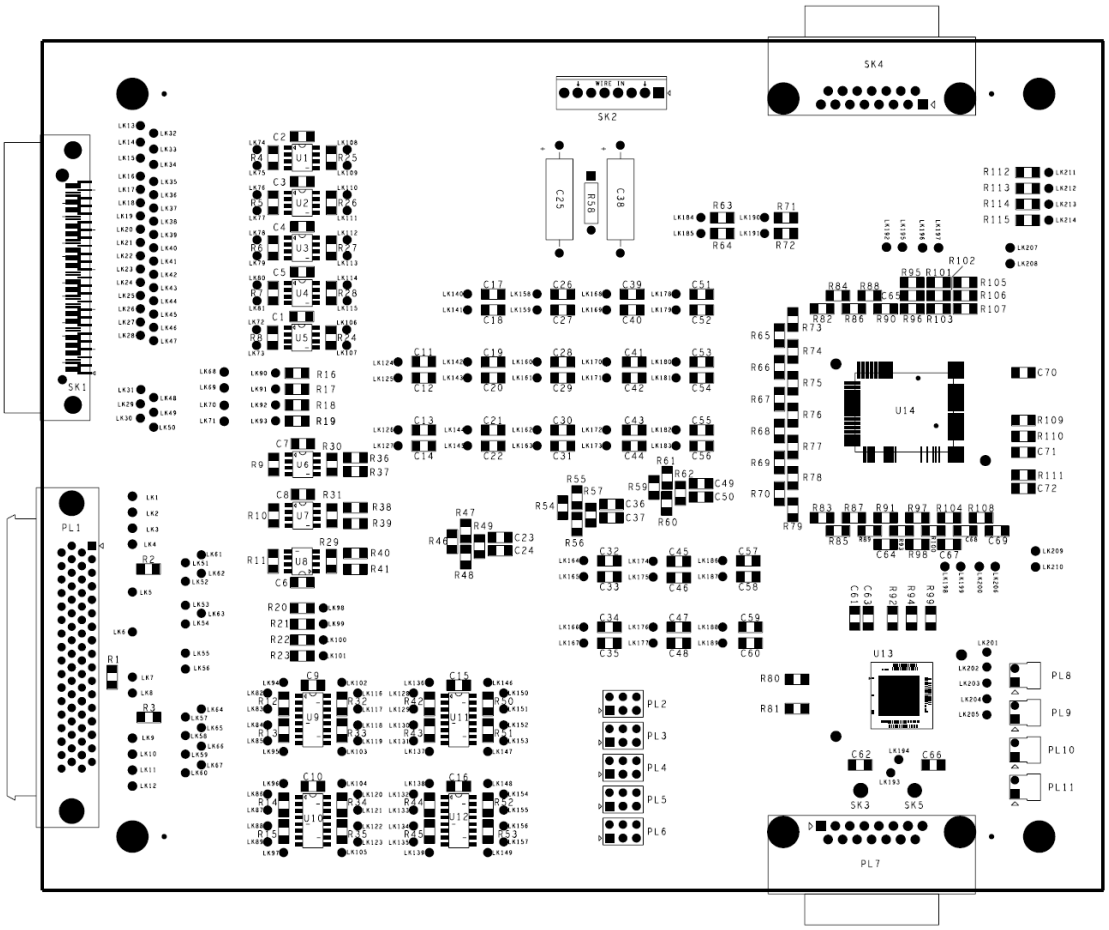
TITLE
PC3413M CIRCUIT
SPI MOTHERBOARD
A2-TE-0145-004-01-A

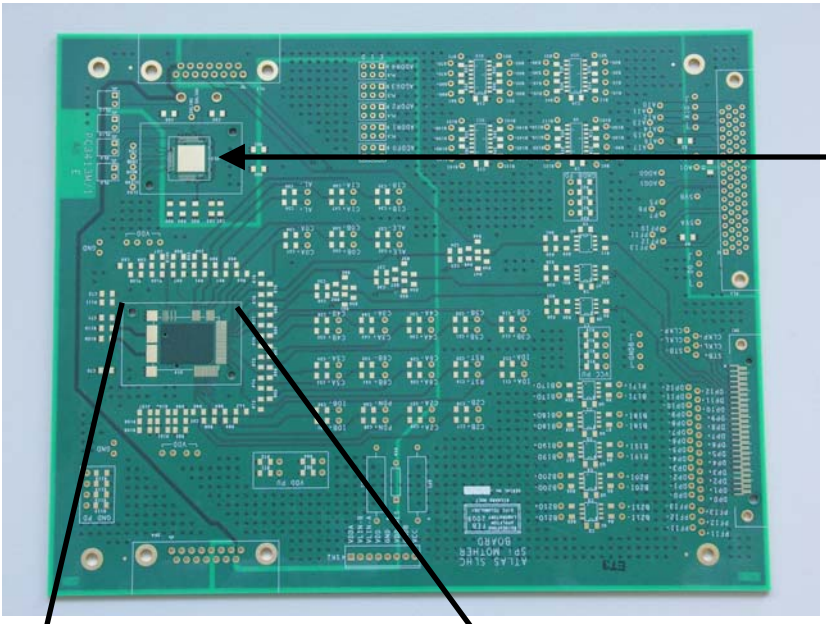

U14
SPI DAUGHTER BOARD
SPID
U13
ABCNEXT-TEST
ATLAS SLHC TRACKER UPGRADE
PC3413M CIRCUIT
SPI MOTHERBOARD
A2-TE-0145-004-03-A

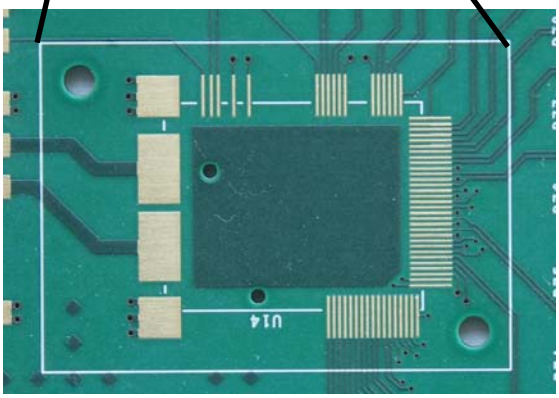
Layout

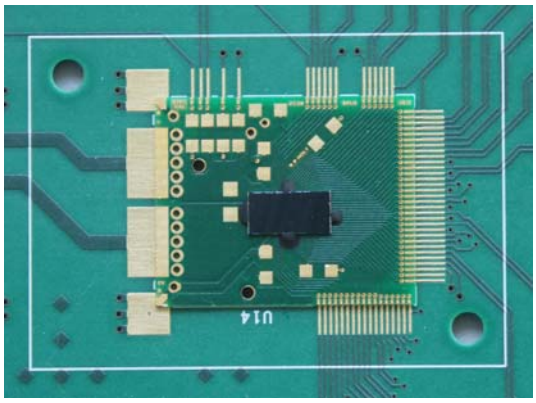

SK4
SK2
SK1
PL1
PL2
PL3
PL4
PL5
PL6
PL7
PL8
PL9
PL10
PL11
U13
U14
SK3
SK5

# Photos

SPiM

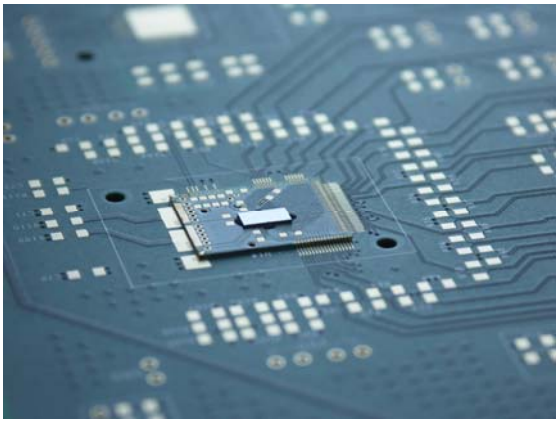


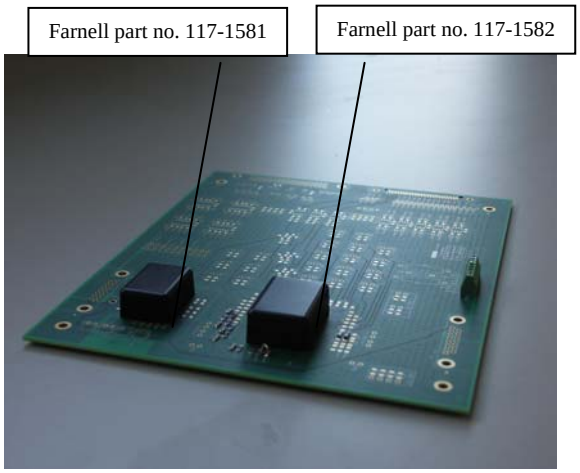


SPi mounting position on SPiM

SPiD mounted & wire-bonded to SPiM PCB

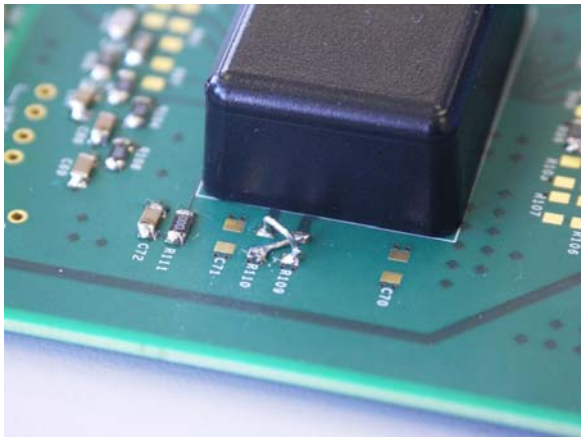


SPi side view




SPi and ABCn covers

Correction needed on (current) SPiM to correct error noted on section “SPi Mother (SPiM) PCB”:



# 9 Specifications (unfinished)

## *9.1 Default values (after power-up)*

| Parameter | default value (nominal) | unit |
|---|---|---|
| Shunt regulator voltage | 1.5 | V |
| Linear regulator A voltage | 1.2 | V |
| Linear regulator B voltage | 1.2 | V |
| Shunt regulator current trip | 4.0 | A |

### 9.1.1 "LVDS-like" Serial data

| Parameter | min | typ | max | unit |
|---|---|---|---|---|
| Clock frequency | | | 50 | MHz |
| + input to SPi: "0" (with respect to source ground, at time of clock rising edge) | 0.95 | 1.025 | 1.1 | V |
| + input to SPi: "1" (with respect to source ground, at time of clock rising edge) | 1.3 | 1.375 | 1.45 | V |
| Termination resistance | 95 | 100 | 105 | Ω |
| Rise time | 0.01 | 0.1 | 0.2 | ns |
| Fall time | 0.01 | 0.1 | 0.2 | ns |
| Time between command and response | 5.0 | 10.0 | 15.0 | ns |
| Time between response and next command | 20.0 | 25.0 | ∞ | ns |
| Setup time (data ready to rising edge of clock) | | | | ns |

### 9.1.2 Shunt regulator general

| Parameter | min | typ | max | unit |
|---|---|---|---|---|
| Shunt regulator full range voltage (5 bits, see below) | 1.5 | | 2.5 | V |
| Shunt regulator smallest step voltage | | 100 | | mV |
| Current (ie current though SPi) | 1 | | 4 (target) | A |
| ADC range (4 bits, see below) | | | | |
| ADC alarm delay (4 bits, see below) | | | | |
| ADC alarm threshold (register 16, 6 LSbits) | Defined by ADC range | | | |
| ADC measurement (register 18, 6 MSbits) | Defined by ADC range | | | |

### 9.1.3 Shunt regulator: Register 7 - output

(register 7, 5 LS bits) to output voltage at ADC range = ???

| (decimal) | (binary) | min | typ | max | unit |
|---|---|---|---|---|---|
| 0 | 00000 | | | | V |
| 1 | 00001 | | | | V |
| 2 | 00010 | | | | V |
| 3 | 00011 | | | | V |
| 4 | 00100 | | | | V |
| 5 default | 00101 default | | 1.5 | | V |
| 6 | 00110 | | | | V |
| 7 | 00111 | | | | V |
| 8 | 01000 | | | | V |
| 9 | 01001 | | | | V |
| 10 | 01010 | | | | V |
| 11 | 01011 | | | | V |
| 12 | 01100 | | | | V |
| 13 | 01101 | | | | V |
| 14 | 01110 | | | | V |
| 15 | 01111 | | | | V |
| 16 | 10000 | | | | V |
| 17 | 10001 | | | | V |
| 18 | 10010 | | | | V |
| 19 | 10011 | | | | V |
| 20 | 10100 | | | | V |
| 21 | 10101 | | | | V |
| 22 | 10110 | | | | V |
| 23 | 10111 | | | | V |
| 24 | 11000 | | | | V |
| 25 | 11001 | | | | V |
| 26 | 11010 | | | | V |
| 27 | 11011 | | | | V |
| 28 | 11100 | | | | V |
| 29 | 11101 | | | | V |
| 30 | 11110 | | | | V |
| 31 | 11111 | | | | V |

### 9.1.4 Shunt regulator: Register 18 - LSB

(register 18, 4 MS bits) to ADC range

| (decimal) | (binary) | min | | max | unit |
|---|---|---|---|---|---|
| 0 default | 0000 default | | | | V |
| 1 | 0001 | | | | V |
| 2 | 0010 | | | | V |
| 3 | 0011 | | | | V |
| 4 | 0100 | | | | V |
| 5 | 0101 | | | | V |
| 6 | 0110 | | | | V |
| 7 | 0111 | | | | V |
| 8 | 1000 | | | | V |
| 9 | 1001 | | | | V |
| 10 | 1010 | | | | V |
| 11 | 1011 | | | | V |
| 12 | 1100 | | | | V |
| 13 | 1101 | | | | V |
| 14 | 1110 | | | | V |
| 15 | 1111 | | | | V |

### 9.1.5 Shunt regulator: Register 18 - alarm delay

(register 18, 4 LS bits) to ADC delay

| (decimal) | (binary) | min | typ | max | unit |
|---|---|---|---|---|---|
| 0 | 0000 | | | | ms |
| 1 | 0001 | | | | ms |
| 2 | 0010 | | | | ms |
| 3 | 0011 | | | | ms |
| 4 | 0100 | | | | ms |
| 5 | 0101 | | | | ms |
| 6 | 0110 | | | | ms |
| 7 | 0111 | | | | ms |
| 8 | 1000 | | | | ms |
| 9 | 1001 | | | | ms |
| 10 | 1010 | | | | ms |
| 11 | 1011 | | | | ms |
| 12 | 1100 | | | | ms |
| 13 | 1101 | | | | ms |
| 14 default | 1110 default | | 3 | | ms |
| 15 | 1111 | | | | ms |

### 9.1.6 Shunt regulator: Register 24 – ADC (read & alarm threshold)

ADC measurement (register 24, 6 MS bits) & alarm threshold (register 15, 6 LS bits)

| (decimal) | (binary) | min | typ | max | unit |
|---|---|---|---|---|---|
| 0 | 00000 | | | | V |
| 1 | 00001 | | | | V |
| 2 | 00010 | | | | V |
| 3 | 00011 | | | | V |
| 4 | 00100 | | | | V |
| 5 | 00101 | | | | V |
| 6 | 00110 | | | | V |
| 7 | 00111 | | | | V |
| 8 | 01000 | | | | V |
| 9 | 01001 | | | | V |
| 10 | 01010 | | | | V |
| 11 | 01011 | | | | V |
| 12 | 01100 | | | | V |
| 13 | 01101 | | | | V |
| 14 | 01110 | | | | V |
| 15 | 01111 | | | | V |
| 16 | 10000 | | | | V |
| 17 | 10001 | | | | V |
| 18 | 10010 | | | | V |
| 19 | 10011 | | | | V |
| 20 | 10100 | | | | V |
| 21 | 10101 | | | | V |
| 22 | 10110 | | | | V |
| 23 | 10111 | | | | V |
| 24 | 11000 | | | | V |
| 25 | 11001 | | | | V |
| 26 | 11010 | | | | V |
| 27 | 11011 | | | | V |
| 28 | 11100 | | | | V |
| 29 | 11101 | | | | V |
| 30 | 11110 | | | | V |
| 31 | 11111 | | | | V |

### 9.1.7 Control data interface parameters

| Parameter | min | typ | max | unit |
|---|---|---|---|---|
| Data pulse width | 0.8 | 1.0 | 1.2 | ms |
| Data pulse height (wrt constant current PSU gnd) | 4.0 | 5.0 | 6.0 | V |
| Time between start of each data packet data pulse | 4.8 | 5.0 | 5.2 | ms |
| Pulse rise time | 0.01 | 0.1 | 0.2 | ms |
| Pulse fall time | 0.01 | 0.1 | 0.2 | ms |
| Time between command and response | 5.0 | 10.0 | 15.0 | ms |
| Time between response and next command | 20.0 | 25.0 | ∞ | ms |