



Final Report for PV Incubator Subcontract No. NEU-0-99010-09

March 29, 2010 — March 28, 2011

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MicroLink Devices
Niles, Illinois

NREL Technical Monitor: Kaitlyn VanSant

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Executive Summary

MicroLink has developed a process technology that will enable the manufacture of high-efficiency, low-cost, multijunction solar cells for use in concentrating photovoltaic (CPV) applications. The multijunction cells were fabricated using a novel low-temperature wafer bonding process. A triple-junction InGaP/GaAs/Ge tandem solar cell with efficiency of 30% at 1 sun AM1.5 illumination was fabricated by wafer bonding a dual-junction InGaP/GaAs cell to a single-junction Ge cell. Temperature cycling over the range -25°C to $+40^{\circ}\text{C}$ resulted in no degradation of cell performance. Triple junction InGaP/GaAs/Ge cells were mounted onto ceramic carriers and tested at concentrations up to 300 suns.

Task 1 - Hardware Baseline

The Subcontractor shall deliver triple junction InGaP/GaAs/InGaAs IMM (Inverted Metamorphic) ELO (Epitaxial Liftoff) cells that represent current ELO cell manufacturing technology.

Baseline Deliverable: Three 0.5 x 0.5 cm² working triple-junction InGaP/GaAs/InGaAs IMM ELO solar cells tested under AM1.5D at 1 sun illumination. The triple junction ELO cells shall be delivered on full 4-inch wafers.

One full 4-inch ELO wafer with IMM triple-junction solar cells of 0.25 cm² area was delivered to NREL. Figure 1 shows the efficiency map of the wafer, which was measured at MicroLink using a Newport Solar Simulator. The performance of the cells was also measured by NREL; data for device H1 is shown in Figure 2. The data from MicroLink and NREL are in reasonable agreement. The efficiency results for the triple junction solar cell indicate MicroLink's baseline technology.

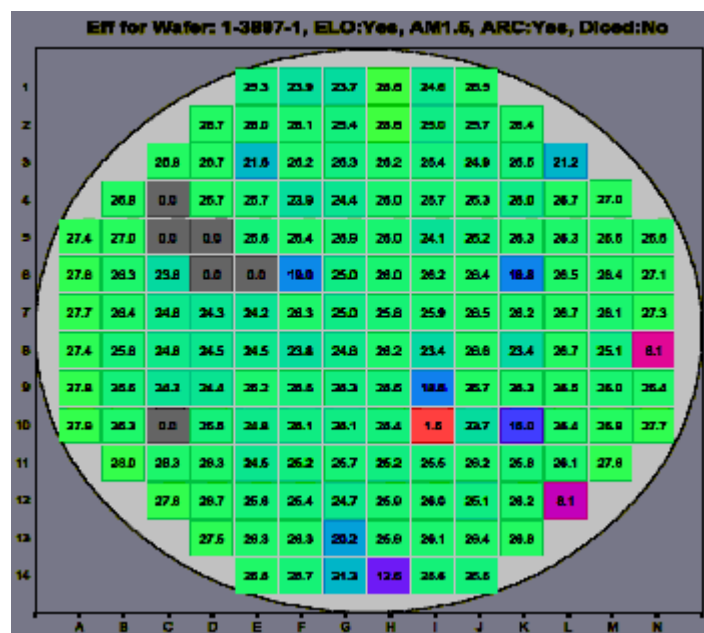


Figure 1: Efficiency map for wafer 1-3897-1, which was delivered to NREL as Deliverable #1.

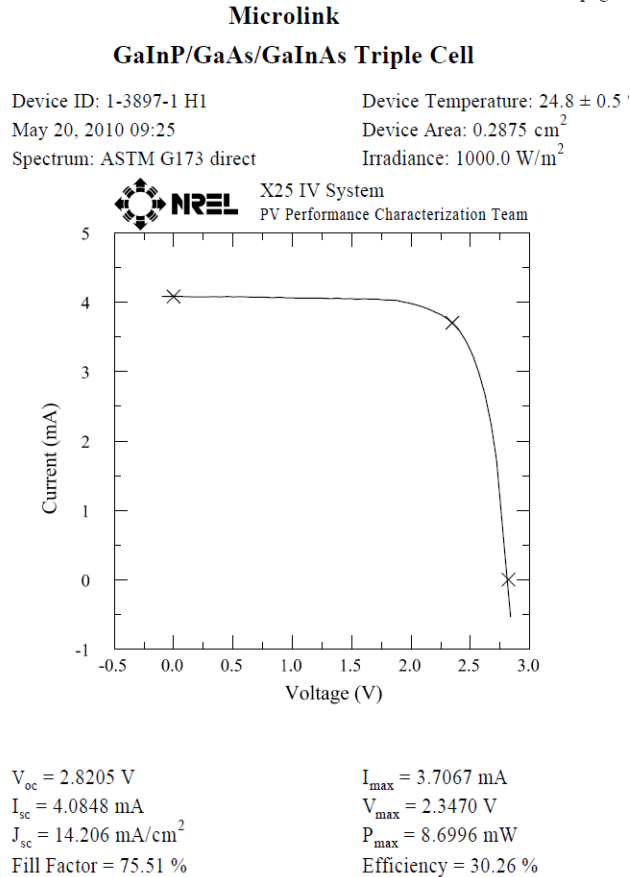


Figure 2: I-V measurements done at NREL on 1-3897-1, cell H1.

Task 2 – Cell Design Development

The Subcontractor shall develop a design for a triple-junction, wafer-bonded cell that maximizes the efficiency of the cell for AM1.5D illumination at 300x concentration.

Milestone 1: Design for a triple junction, wafer-bonded ELO cell with efficiency at least 28% under AM1.5D illumination at 300x concentration. This information shall be provided in Quarterly Report #1.

Wafer Bonded Cell Design and Modeling:

A model of the wafer-bonded solar cell was constructed. The cell performance was simulated under AM1.5 spectrum illumination. We assumed that the cell absorbs all the photons above the bandgap. Photons with wavelength $< 300 \text{ nm}$ were excluded from the model. The modeled efficiency values were based on total illumination of 1 kW/m^2 .

Two baseline triple junction structures were modeled. Structure A (Figure 3) contained a dual-junction assembly, in which the top two cells were grown on a GaAs substrate, and a single-junction bottom cell grown on an InP substrate. Structure B (Figure 5) was a single-junction top cell grown on a GaAs substrate and a dual-junction bottom cell assembly grown on InP substrate.

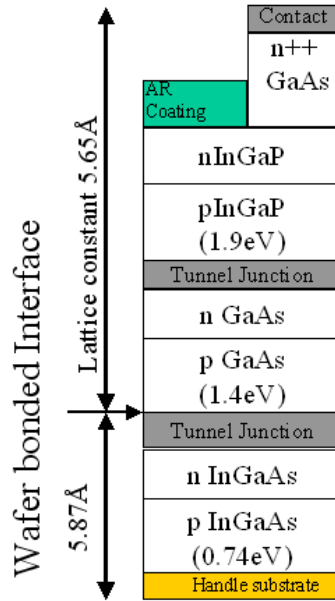


Figure 3: Structure A: wafer bonded triple junction solar cell where the top two cells are lattice matched to a GaAs substrate.

The cell efficiency was optimized by varying the top cell band gap and keeping the bandgaps of the other two cells fixed. In Figure 4, calculated cell efficiencies are plotted for Structure A as a function of top cell band gap.

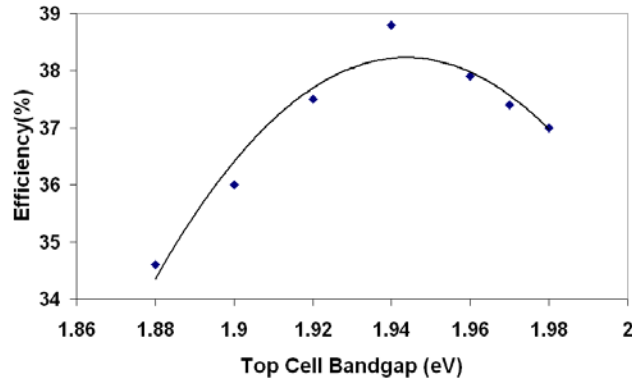


Figure 4: Effect of InGaP top cell band gap on calculated efficiency for Structure A, which is shown in Figure 3.

It is evident from Figure 4 that the calculated cell efficiency goes through a maximum as the top cell bandgap is varied. The peak efficiency of 38.8% was obtained for a top cell bandgap of 1.94 eV. To obtain this bandgap in practice, it would be necessary to include aluminum in the top InGaP cell. Higher Al content materials are difficult to grow, due to their affinity towards oxygen, which in turn will lower the life-time. This will in turn effect the long term reliability of the devices. This cell under concentration of 300 suns is expected to have efficiency in excess of 40%.

In Structure B, which is shown in Figure 5, the dual-junction cell is lattice matched to InP. The top cell, which is grown lattice matched to GaAs, is fixed as InGaP. In simulations, the bandgap of the bottom (InGaAs) cell was varied, and the efficiency of the bonded, triple-junction cell was calculated.

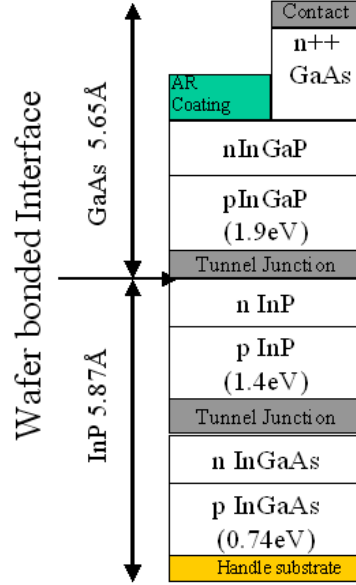


Figure 5: Structure B: wafer bonded triple junction solar cell where the bottom two cells are lattice matched to InP substrate.

In Figure 6, calculated cell efficiencies are plotted for Structure B as a function of bottom cell bandgap.

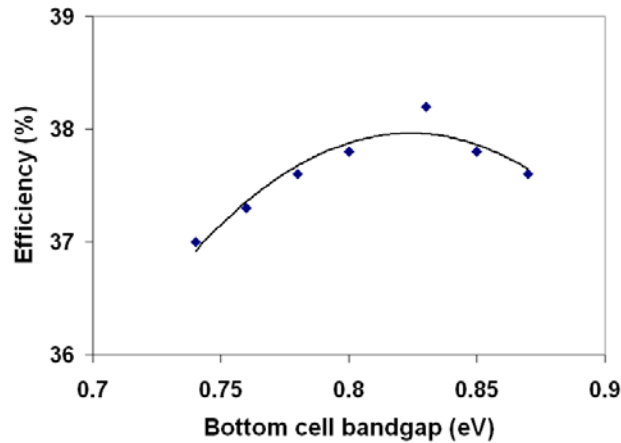


Figure 6: Effect of InGaAs bottom cell band gap on efficiency for Structure B.

Figure 6 shows that the calculated cell efficiency goes through a maximum as the bottom cell bandgap is varied. The optimum bandgap value of 0.84 eV gives an efficiency of 38.2%. This value of bandgap is consistent with the quaternary material InGaAsP lattice matched to InP. However, even if we are restricted to lattice matched InGaAs bandgap of 0.74 eV, the efficiency

is still a respectable 37%. The efficiency of Structure B at 300 suns illumination is expected to be more than 40%.

Task 3 – Chemical Mechanical Polishing

One of the important aspects of wafer bonding is the requirement of obtaining atomically flat interfaces, which are to be bonded together. The chemical mechanical polishing (CMP) of ELO and non-ELO (before lift-off) of InP surfaces and GaAs surfaces shall be investigated by the Subcontractor with various chemicals such as sodium hypochlorite and citric acid solutions. The Subcontractor shall investigate the limits of the flatness that can be achieved using this process. The Subcontractor shall investigate optimal composition of the slurry for III-V materials. A balance between reduced sub-surface mechanical damage and smooth surface morphology is the target of this task.

Milestone 2: Description of method for performing CMP across the full area of a 2-inch diameter ELO wafer resulting in surface roughness <1 nm root mean square (RMS). Verification shall consist of Atomic Force Microscopy (AFM) measurement at five points across the wafer. The results shall be provided in Quarterly Report #2.

CMP Technology

MicroLink purchased and installed a Logitech PM5A CMP tool. Procedures for mounting the wafer on the polishing jig were investigated. One procedure found to be suitable was a wax-less mounting procedure, in which the wafer is mounted directly to the polishing jig without a wax-mounted carrier puck. This step greatly reduces the time for the CMP process and reduces wafer handling breakage problems. The force applied to the wafer surface is a critical aspect of the polishing procedure. A scale is necessary to set this force (with the sample polishing jig). A photograph of the setup used is shown in Figure 7. It consists of a laboratory scale and a stand to mount the polishing jig on top. Such a force measurement is crucial for reproducible polishing.

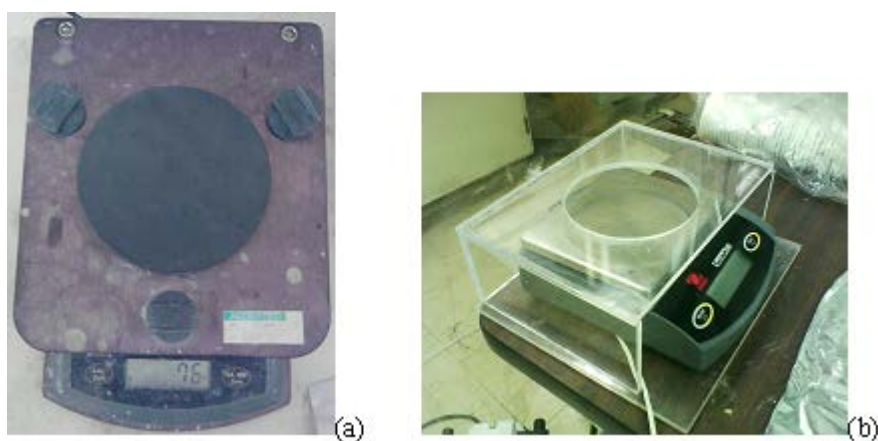


Figure 7: Scales and supports used to calibrate the stress on the wafer during CMP.

The surface roughness of the polished wafers can be assessed using X-ray reflectivity and AFM. This procedure involves measuring glancing angle x-ray reflectivity and modeling that uses a simulation program.

Figure 8 shows x-ray reflectivity spectra of an InGaAs layer grown on top of an InP substrate. Figure 8 (b) shows the diffuse scan, from which we can determine the surface roughness of the epilayer. In this case, the surface roughness is approximately 32 nm.

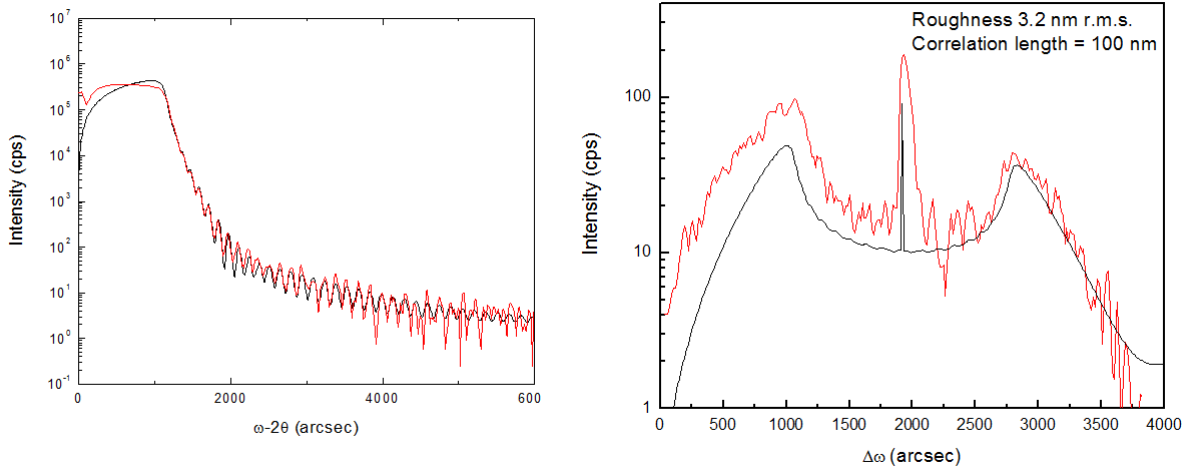


Figure 8: (a) x-ray reflectivity specular scan (b) diffuse scan (rocking curve) showing RMS roughness values of 32 nm determined from the simulated scans (black).

Abrasive-Free CMP

To better understand the CMP process, special InP substrates with a known surface roughness were prepared using chemical etching. The effect of the CMP process on these surfaces was then studied. Atomic force microscopy was used to assess roughness at different locations on the wafer surface. To determine the polishing rate, indented grooves were produced in the wafer at different locations. Some of the grooves can be observed in the optical micrograph shown in Figure 9; the red boxes in the Figure show the location of the AFM images produced after each subsequent CMP step. This allows us to produce a map of the change in roughness over the entire 100 mm diameter substrate.

With this procedure, we determined the overall material removal rate, as well as the roughness removal rate for the citric acid, sodium hypochlorite, and water solution. The scale mass applied was 3,000 g over the 100 mm diameter InP substrate surface. On average, when decreasing roughness from an initial value of 30 nm RMS to 0.5 nm RMS, we calculated an average material removal rate of 5 nm per minute and the roughness reduction rate was 0.4 nm RMS per minute. This indicates that to reduce roughness from a value of 3 nm RMS to 0.5 nm RMS, one should polish for approximately six minutes, which will reduce the overall thickness by about 30 nm. Bonding structures should therefore be designed with an appropriate layer thickness to allow for the removal of material to reduce the roughness.

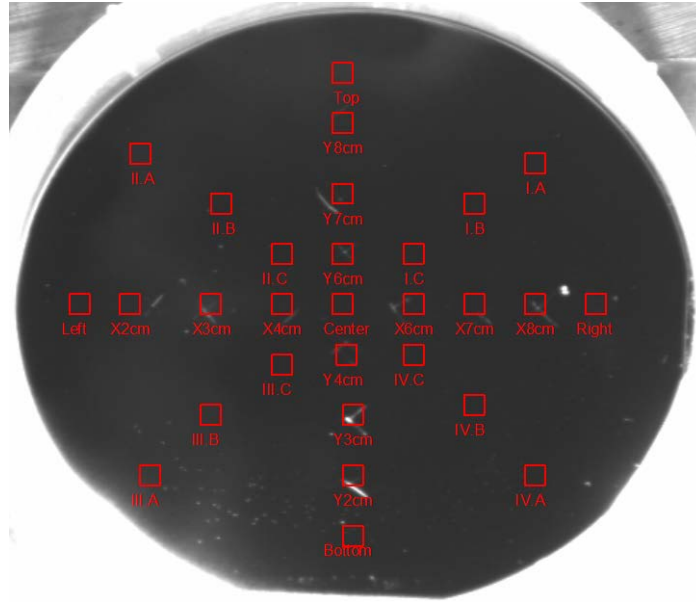
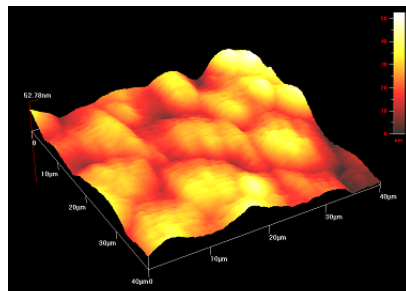


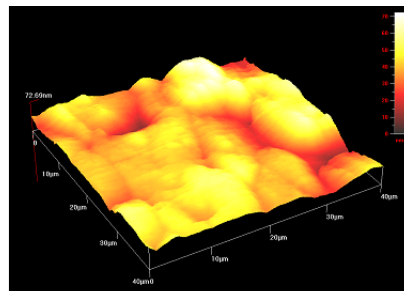
Figure 9: A map of the AFM measurement locations.

Surface Roughness of InGaAs Epilayers on InP Surface:

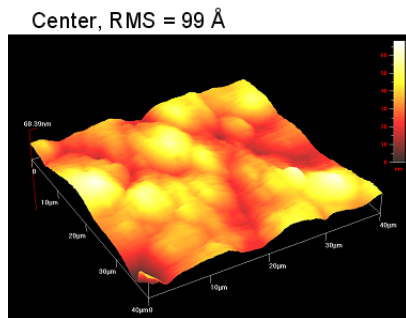
InGaAs single-junction cells grown on InP had a surface roughness $>30 \text{ \AA}$ as measured by AFM. Figure 10 shows the AFM images for as-grown InP surfaces on top of InGaAs single-junction cells on InP substrates.



Left, RMS = 82 \AA



Right, RMS = 99 \AA



Center, RMS = 99 \AA

1-4238-2 As grown

Figure 10: AFM images of InP surfaces showing roughness $>80 \text{ \AA}$.

Figure 11 shows the effect of CMP time on the average roughness of the InP surface. CMP reduced the surface roughness to 20 Å but not to <10 Å, which is needed for successful wafer bonding. The excess surface roughness was primarily due to two factors: i) large particles from the reactor ceiling were deposited on the growth surface; ii) the CMP polishing jig created rust, which was a source of large particles. A better technical understanding of the process and/or an improved epitaxial growth process is necessary to solve this problem.

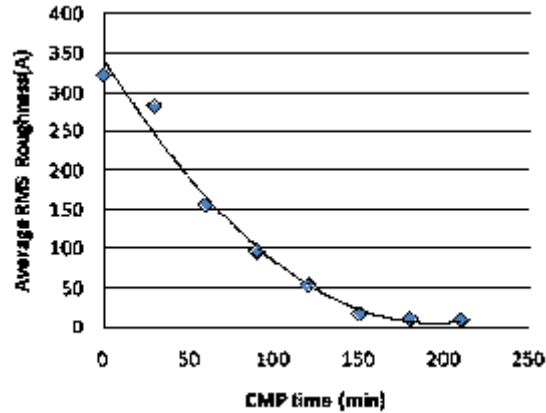


Figure 11: CMP time versus surface roughness for InP layers.

Task 4 – Wafer Bonding

The Subcontractor shall develop a low-temperature wafer-bonding process to bond 2-inch wafers of InP-based and GaAs-based solar cells. The success of the wafer bonding process critically depends upon the integrity of the bonded interface. The electrical and structural properties of the interface shall be used to measure the quality of the interface. Efficiency improvements shall be achieved through minimizing the defects at the interface. In order to accomplish this, we need flat and smooth bonding surfaces. Finally the occurrence of voids at the bonded interface needs to be minimized.

GaAs-GaAs and InP Wafer Bonding

Surface roughness of the bonding interfaces is a parameter that is critical to the success of wafer bonding. Activation of the surface is essential for low-temperature bonding. Surface activation can be achieved by exposing the surface to sulfur-based solutions. Surface roughness is not affected by sulfur termination.

An IR reflectivity image of a GaAs-GaAs wafer bonded sample is shown in Figure 12. The uniform dark areas in the IR image indicate well-bonded regions; by contrast, lighter areas indicate poorly bonded regions or voids. Except for two regions where fringes are observed, a uniformly dark area is seen, indicating good, void-free bonding. In this example, the GaAs wafers were terminated with sulfur and then were brought in contact with each other in vacuum at about 325 °C. The wafers were then annealed under pressure of 6 kN for about 1 hr. The wafer-bonding process was done in a commercial EVG510 bonder.

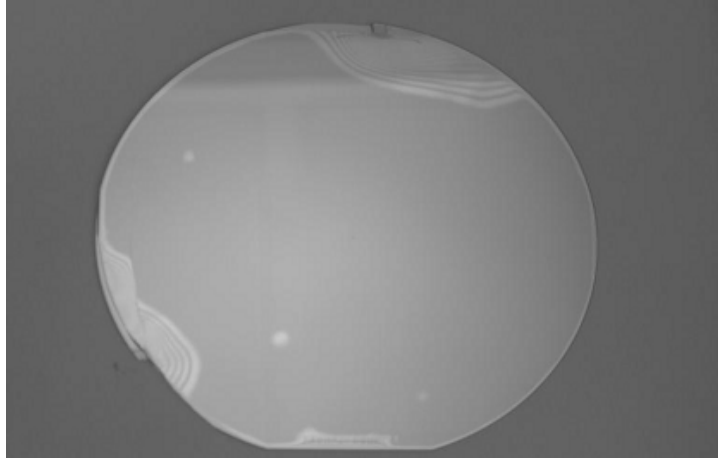


Figure 12: 4-inch GaAs wafer bonded to another GaAs substrate wafer.

Figure 13 shows IR images of two examples of a GaAs wafer bonded to an InP substrate. The striations seen in the figure are reflections of ceiling tiles; they are not defects. In Sample 1, there are no visible voids; in Sample 2, voids are indicated by the arrow. These wafers were bonded together after activating the surfaces in sulfur solution for 10 min. The surface roughness of these substrates is <1 nm.

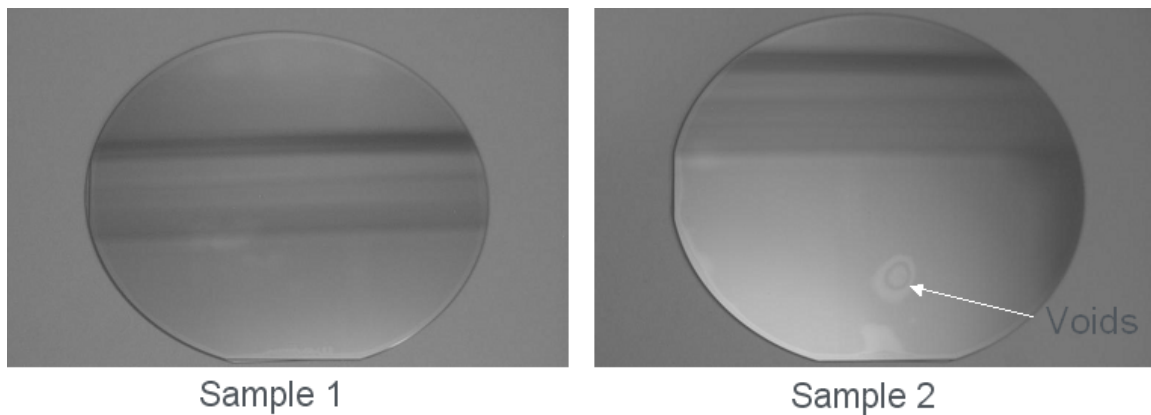


Figure 13: IR reflection images of a GaAs wafer bonded to an InP wafer.

Wafer bonding experiments using epitaxial layers grown on InP and GaAs substrates were not successful. Epitaxial surfaces grown on top of InP substrates exhibit roughness in excess of 3 nm. During the development of InP-GaAs wafer bonding, we have encountered the following problems:

1. **Surface Roughness of InGaAs Epilayers on InP Surface:** As described in the progress report for Task 3, the InGaAs single-junction cells grown on InP had a surface roughness that was too large to permit successful wafer bonding. A better technical understanding of the CMP process and/or an improved epitaxial surface roughness is necessary to solve this problem.
2. **Coefficient of Thermal Expansion (CTE):** Another problem is that the InP wafers tend to crack after a wafer bonding cycle. The underlying reason for this is that the CTE of GaAs and InP are different and the GaAs substrate cools faster than InP substrate,

thereby creating strain in the InP substrate. For successful bonding, the temperatures for GaAs and InP based material systems are in the range of 550-650⁰C. The CTE mismatch of GaAs and InP substrate usually leads to either cracking in the InP layers or de-bonding at the bonding interface, during cool down process. One possible solution is to reduce the thickness of the InP substrate because thin substrates are more compliant; however, thin InP substrates are more brittle and tend to crack and break more readily.

3. **Exposure of Wafer-Bonded GaAs/InP Structures to HF Results in De-Bonding:** We have attempted to perform the ELO process on samples that we have successfully bonded in order to reclaim the InP and GaAs substrates. To do this, the wafer-bonded structure has to remain in an HF etching solution for more than six hours to dissolve the release layer. We have found that soaking the bonded interfaces in HF results in complete de-bonding of the samples. We believe this is caused by percolation of HF solution into any available small pores (un-bonded areas at the edges of the wafers) and subsequent etching of the oxide layer present at the bonded interface.
4. **ELO Backing Metal Diffusion:** Wafer bonding of an ELO single-junction InGaAs cell and a dual-junction GaAs/InGaP cell on a GaAs substrate resulted in diffusion of the ELO backing metal into the epitaxial structures and complete destruction of the solar cell layers. This can be avoided by designing a new ELO metal stack, which has metal diffusion barriers before the epilayers.
5. **Development of InGaAsP/InGaAs Dual-Junction Cells:** In the next stage of MicroLink's development plan, which involves increasing the number of junctions from three to four, we will need to develop InGaAsP/InGaAs dual-junction solar cells on InP. This development will require work on InGaAsP single junction cells and also on the tunnel diode. We believe this technology development needs additional time.

Alternative Path to Wafer-Bonded, Triple-Junction Cells using Ge Substrates:

In light of the problems described above, an alternate method of fabricating wafer-bonded triple-junction solar cells was proposed and adopted. The alternate path is based on wafer bonding InGaP/GaAs dual junction solar cell on a GaAs substrate to a Ge single-junction cell on a Ge substrate. This solution has following advantages:

1. **Surface Roughness:** Surface roughness is not an issue as there is no epitaxial growth on a Ge substrate, only diffusion of p-n junctions. AFM studies show 10 Å average surface roughnesses on Ge substrates, which should lead to good-quality wafer bonding.
2. **Coefficient of Thermal Expansion(CTE):** The CTE of GaAs and Ge are very similar, so high-temperature bonding (400-500⁰C) may be used with little risk of cracking or breaking of the wafers during cool-down after wafer bonding. The risk is further diminished by the fact that Ge substrates with thickness <200 µm are available today. This is due to the higher mechanical strength of Ge substrates in comparison with InP substrates. The surface hardness of Ge is nearly twice that of InP based on knoop's pyramid test.
3. **Wafer-Bonded Quadruple-Junction Cells:** The proposed alternate structure can be extended from three to four junctions by wafer bonding a triple-junction IMM cell to a Ge substrate, thereby achieving an InGaP/GaAs/InGaAs/Ge quadruple-junction solar cell.

This is expected to be more robust and achievable than the original solution of a InGaAsP/InGaAs dual-junction cell on an InP substrate.

The process flow for fabrication of triple-junction InGaP/GaAs/Ge cells is shown in detail in Figure 14.

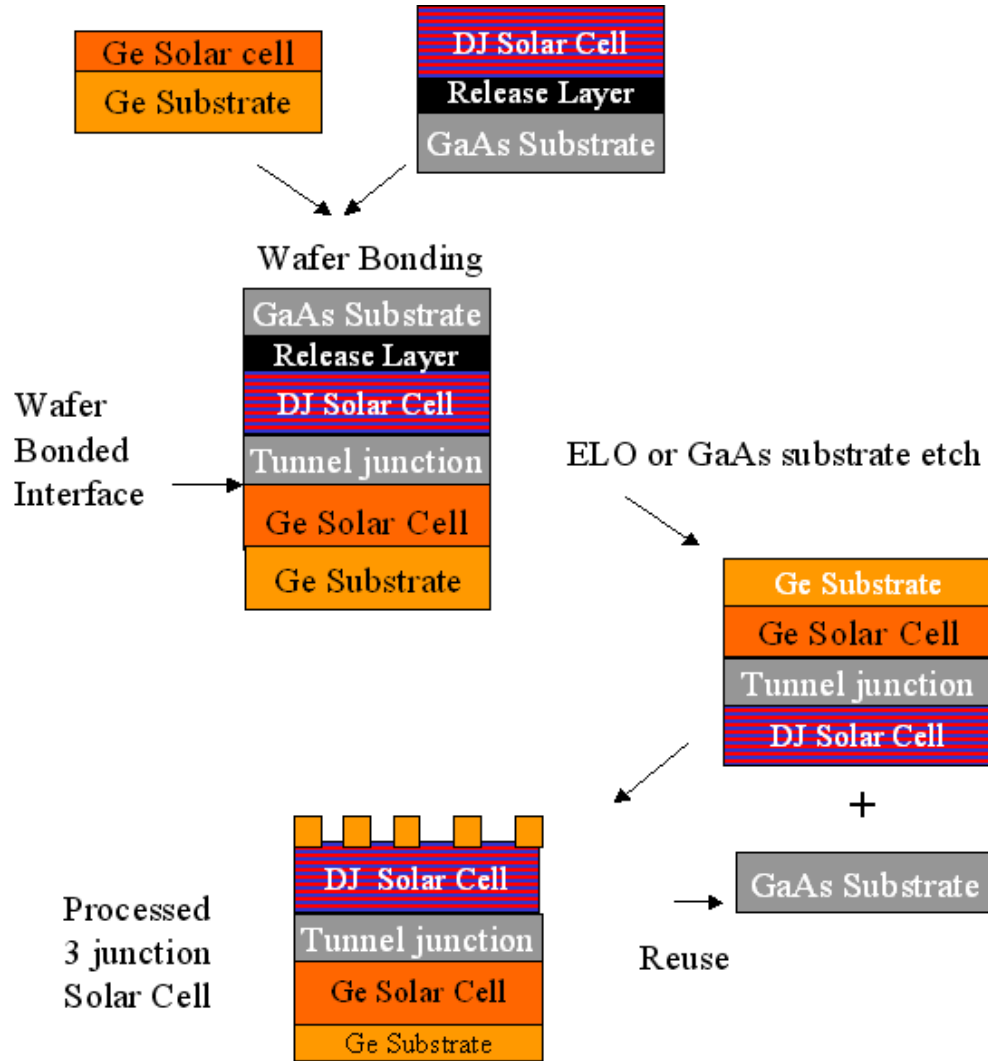


Figure 14: Process flow for fabrication of triple-junction InGaP/GaAs/Ge solar cells using wafer bonding and ELO of the GaAs substrate.

The process consists of the following four steps:

Step 1: Grow Inverted Dual-Junction Solar Cell

An inverted dual-junction InGaP/GaAs solar cell is grown on a GaAs substrate. The InGaP/GaAs cell is terminated with a GaAs-n⁺⁺/GaAs-p⁺⁺ tunnel junction followed by an InGaP cap layer. A typical layer structure for a dual-junction cell terminated with a tunnel junction is shown in Figure 15.


nInGaP	Window	
nGaAs	TJ	
pGaAs	TJ	
pInGaP	BSF	
pGaAs	Base	
nGaAs	Emitter	
nInGaP	Window	
nGaAs	TJ	
pGaAs	TJ	
pInGaP	BSF	
pInGaP	Base	
nInGaP	Emitter	
nInAlP	Window	
nGaAs	Contant	
InGaP	Etch Stop	
GaAs	Substrate	

Figure 15: Schematic of inverted dual-junction solar cell terminated with tunnel junction.

One of the critical criteria for wafer bonding to occur successfully is to have a very smooth bonding surface; in practice a surface with a RMS roughness less than 1-2 nm. We have used an AFM to study and measure the morphology of the surfaces of our inverted InGaP/GaAs dual-junction solar cells. Figure 16 shows an AFM scan for the bonding surface of a typical InGaP/GaAs dual-junction solar cell. The average RMS surface roughness in this case is about 1.2 nm, which is acceptable for bonding.

1-4527-3 DJ GaAs wafer
Sq = 1.22nm

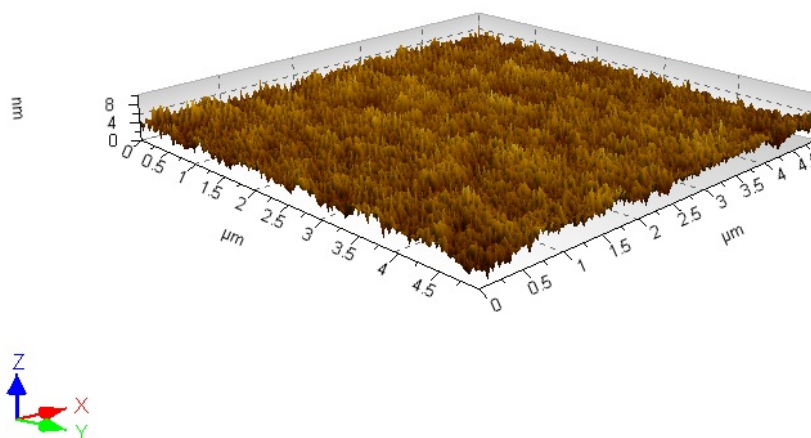


Figure 16: AFM scan showing the surface morphology of the bonding surface of an inverted InGaP/GaAs dual-junction solar cell.

Step 2: Develop Single Junction Ge Solar Cell

Prior to this program, MicroLink had no knowledge of the fabrication of Ge single-junction solar cells; this expertise had to be developed. Ge p-n junctions can be fabricated by n-diffusion of Group V species (As or P) into a p- Ge substrate. We decided to use phosphine (PH_3) as the phosphorus dopant source. Phosphorus has been reported to have low diffusivity in Ge and, as such, can result in shallow p-n junctions, which allows better control of the doping profile and depth. A typical Ge single-junction solar cell structure is shown in Figure 17.

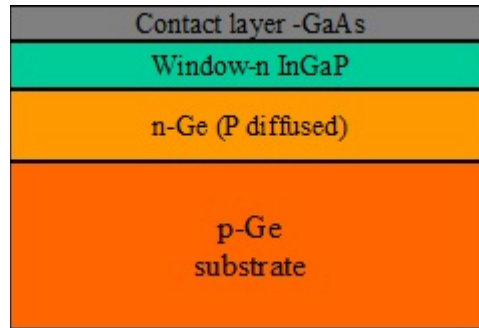


Figure 17: Schematic of single-junction Ge n on p solar cell.

Ge single junction cells were grown and their surface morphology was measured. The surface morphology of a typical Ge substrate with a diffused p-n junction is shown in Figure 18. The morphology measurement shows an RMS surface roughness value of 1.3 nm, which is very similar to the value obtained for the inverted dual-junction solar cells.

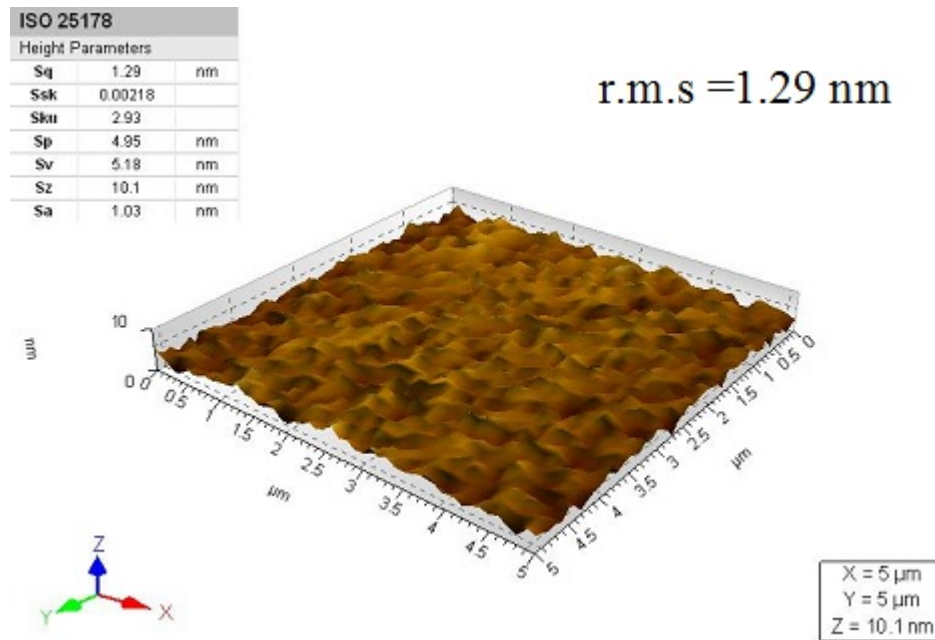


Figure 18: AFM scan showing the surface morphology of the bonding surface of a Ge solar cell with diffused p-n junction.

Step 3: Wafer Bonding and Cell Fabrication

The wafers described above were bonded together in MicroLink's EVG wafer bonder. Successful wafer bonding was obtained by applying a pressure of 7 kN/cm^2 at 450°C for 3 hr under vacuum. The GaAs substrate was removed by an etch process after the bonding was complete. The wafer-bonded InGaP/GaAs/Ge structure was processed using standard solar cell processing steps, including grid metallization and isolation etch. A fully processed quarter of a 4-inch wafer bonded solar cell is shown in Figure 19.

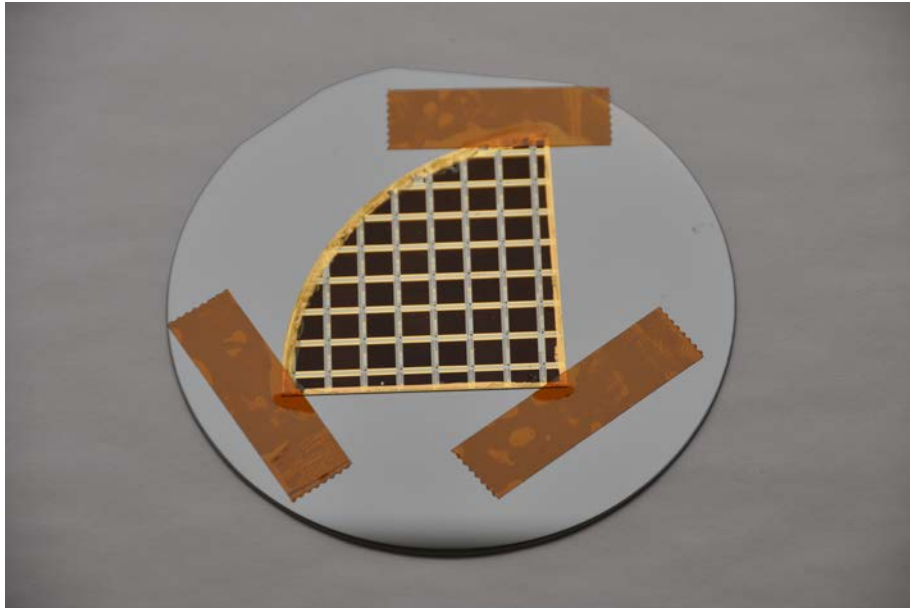


Figure 19: Processed wafer-bonded triple-junction solar cells.

Step 4: I-V Analysis of Wafer-Bonded, Triple-Junction Cells

We performed I-V and QE analysis of the wafer-bonded cells. In general, it was found that most wafer-bonded cells exhibited high series resistance. This causes a reduction of the fill factor, which reduces the efficiency of the cells. I-V curve for a wafer-bonded cell is shown in Figure 20. The triple-junction solar cell had efficiency 24.4%, fill factor 77%, $J_{sc} = 12.92 \text{ mA/cm}^2$, and $V_{oc} = 2.48 \text{ V}$.

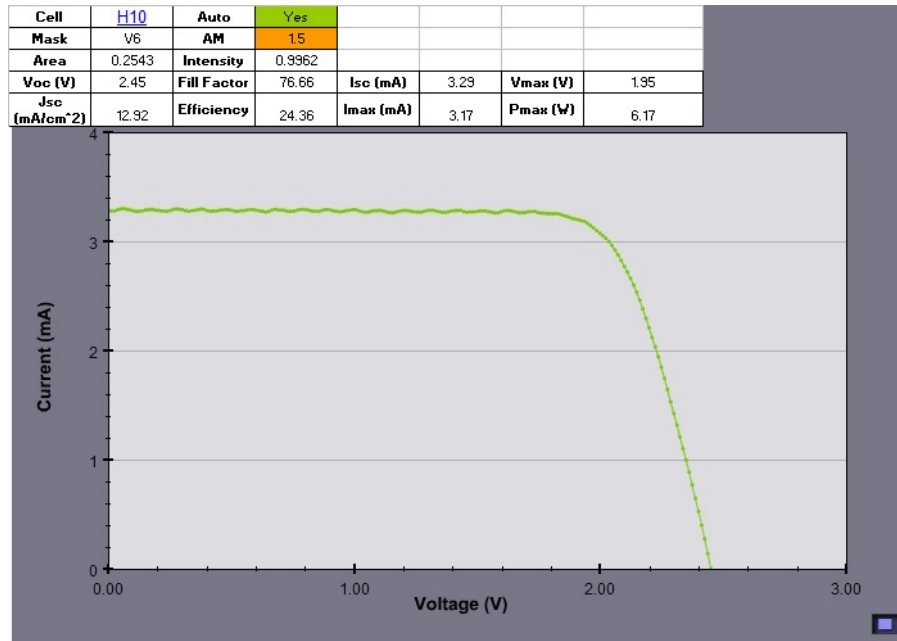


Figure 20: I-V curve for wafer bonded triple-junction InGaP/GaAs/Ge solar cell using 1 sun AM1.5 illumination.

Figure 21 shows a map of efficiency for an array of wafer-bonded triple-junction solar cells measured using a Newport solar simulator producing 1 sun, AM1.5 illumination. The efficiency map indicates a maximum efficiency of 24.4%. All cells are functional, although there is some efficiency variation. The cells meet the intermediate deliverable efficiency target value of 25% within the experimental uncertainty. A value of $\pm 6\%$ measurement uncertainty has been applied to these devices by the NREL Measurement and Characterization group. The accepted error in measurements for multi-junction concentrated cells is of the order of 5%, if the device is top cell limited. On the other hand, for wafer bonded cells, which are bottom InGaAs cell limited, the measurement errors are higher. In the current context, the wafer bonded cells we observed have low fill factor values arising due to high series resistance associated with the wafer-bonded interface.

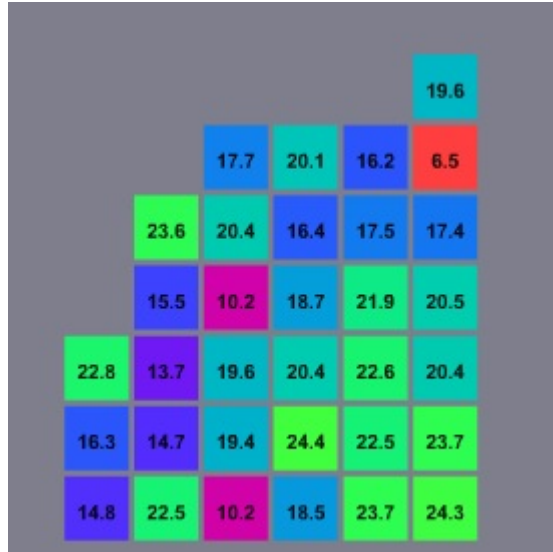


Figure 21: Efficiency map for WB-0.042-4.

Subtask 4.2: Intermediate Deliverable

Three wafer-bonded quarters of a 4-inch wafer of InGaP/GaAs/ Ge cells were submitted to NREL as the intermediate deliverable. The NREL measured I-V and QE data on wafer-bonded cells is shown in Figure 22 and Figure 23.

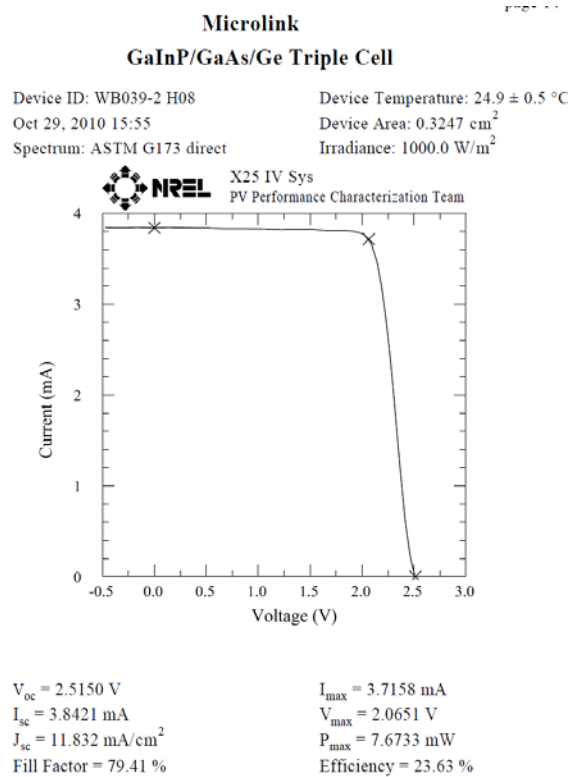


Figure 22: LIV curves for wafer-bonded triple junctions of InGaP/GaAs/Ge.

IV data shows the cells exhibited efficiency of 23.64% with $J_{sc} = 11.83 \text{ mA/cm}^2$ and $V_{oc} = 2.51 \text{ V}$. The fill factor of the cells was about 79% indicating the presence of high resistive layer or shunts in the cells. The QE plot shown in figure 23, has interference oscillations due to the refractive index difference of the top GaAs and the InGaAs cell.

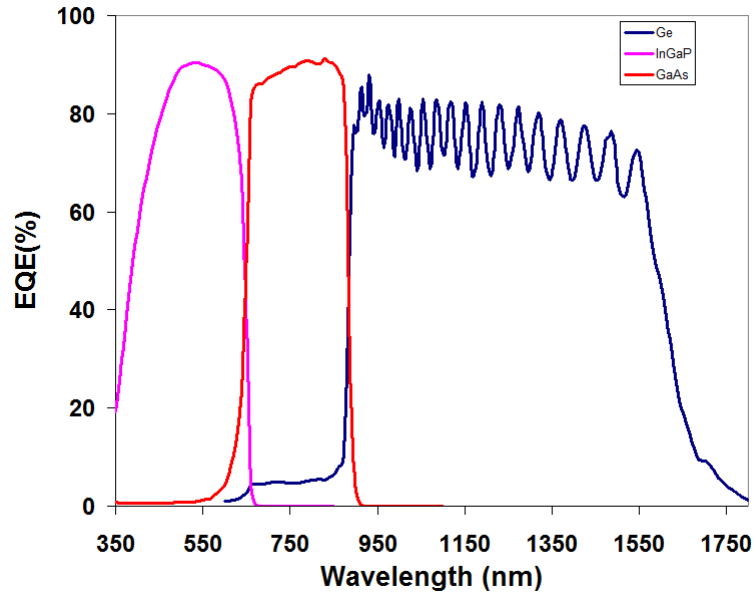


Figure 23: EQE of wafer bonded InGaP/GaAs/Ge triple junction cell.

Subtask 4.3

The Subcontractor shall develop full 2-inch diameter InGaP/GaAs-on-GaAs/InGaAs-on-InP wafer-bonded ELO solar cells with efficiency > 30% at AM1.5D one sun illumination.

Milestone 4: A summary of the fabrication and characterization of 2-inch diameter InGaP/GaAs-on-GaAs/InGaAs-on-InP wafer-bonded ELO solar cells with efficiency > 30% at AM1.5D one sun illumination shall be provided in the Final Report.

Based on our Intermediate deliverable results, it was clear that the main parameter that needs improving is the fill factor of wafer-bonded cells. All the process steps of the wafer-bonded cells were analyzed and critical steps were identified. Improvements in the process steps have resulted in increased efficiency of wafer bonded triple junction cells as shown in Figure 24.

The process improvements were made in two key areas.

1. **Optimizing the wafer bonding parameters:** Wafer bonding parameters such as bonding surface preparation, bonding temperature and pressure were optimized to improve the bonding interface. Bonding temperatures higher than 400°C have resulted in improved device performance.
2. **Isolation Etch:** Area two which resulted in improved device performance was isolation etch. This step was necessary to provide a dicing path and also to isolate each of the cells, when wafer testing is done. Isolation etch using non-selective etchants resulted in cells

with low fill factor values. This may be because of undercutting of the mesa isolation areas. When isolation etching was performed using selective etchants, and employing different etchants for GaAs and Ge, the fill factor values improved considerably.

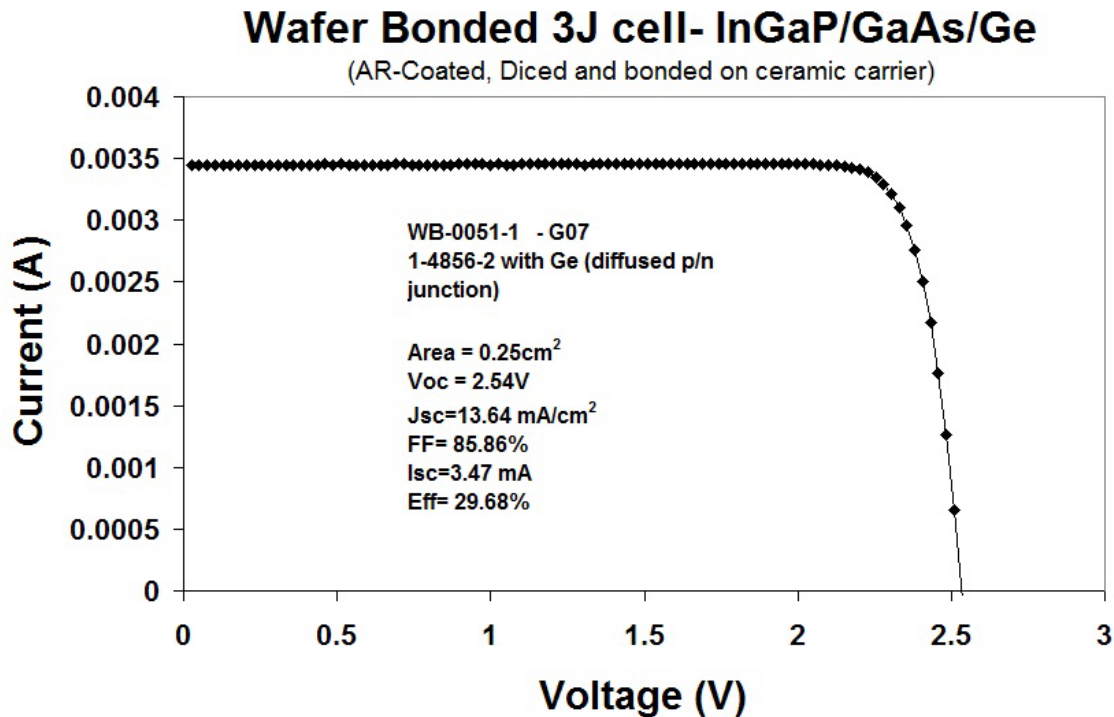


Figure 24: Wafer bonded triple junction solar cells with improved fill factor.

Task 5 - Analysis of Wafer-Bonded Cells

The Subcontractor shall perform optical and electrical analysis of the bonded cells to gain detailed information about the nature of species at the bonded interface. The analysis shall be performed on several wafer-bonded cells. The analysis shall comprise at least X-ray, photoluminescence (PL), infrared (IR), X-ray topography (XRT), and capacitance-voltage (C-V) measurements.

Milestone 5: The results of the optical and electrical analysis performed on several wafer-bonded cells shall be provided in the Final Report.

X-ray and X-ray topography (XRT) measurements were substituted with ultrasonic imaging as it provided better insight into the wafer bonded interface quality. Capacitance-Voltage (C-V) analysis was also not performed on the samples as the measurements on the large area solar cell samples yielded very high capacitance values, which was out of the range of MicroLink's equipment.

Wafer-bonded triple-junction solar cells were studied using IR reflection measurements, which clearly indicate if there are any voids or de-bonding. Figure 25 shows an IR reflectivity image of a 4-inch wafer-bonded cell.

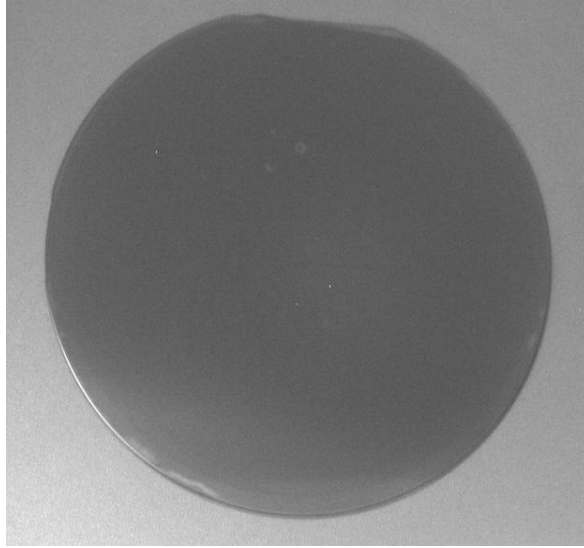


Figure 25: IR reflection image of InGaP/GaAs dual junction wafer bonded to Ge.

The IR image shown in Figure 25 is almost completely dark with only a few light spots, which indicates a uniformly well-bonded sample with very few voids. The lighter areas in the Figure indicate a void or an un-bonded area, which are likely due to the presence of particles or trapped air.

We have used IR imaging to monitor the bonding interface throughout the whole device processing sequence. Figure 26 contains an IR image of the wafer shown in Figure 25 after it was diced and the substrate removed. Again, the relative absence of voids is evident.

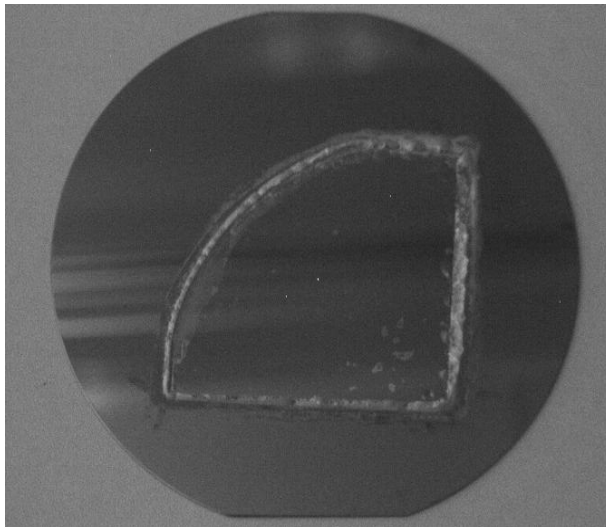


Figure 26: IR image of bonded triple-junction cell after GaAs substrate has been removed.

Ultrasonic Imaging of Wafer-Bonded Cells

Ultrasonic imaging was used to study the wafer-bonded cells. Ultrasonic imaging is very effective in identifying voids and de-lamination at the bonded interface. Results of ultrasonic

imaging of a wafer-bonded triple junction cell are shown in Figure 27. One of the cells is scanned with higher resolution and the presence of white dots and/or de-bonded areas. Figure 28 shows a comparison of the ultrasonic image and an optical image of the wafer bonded cells.

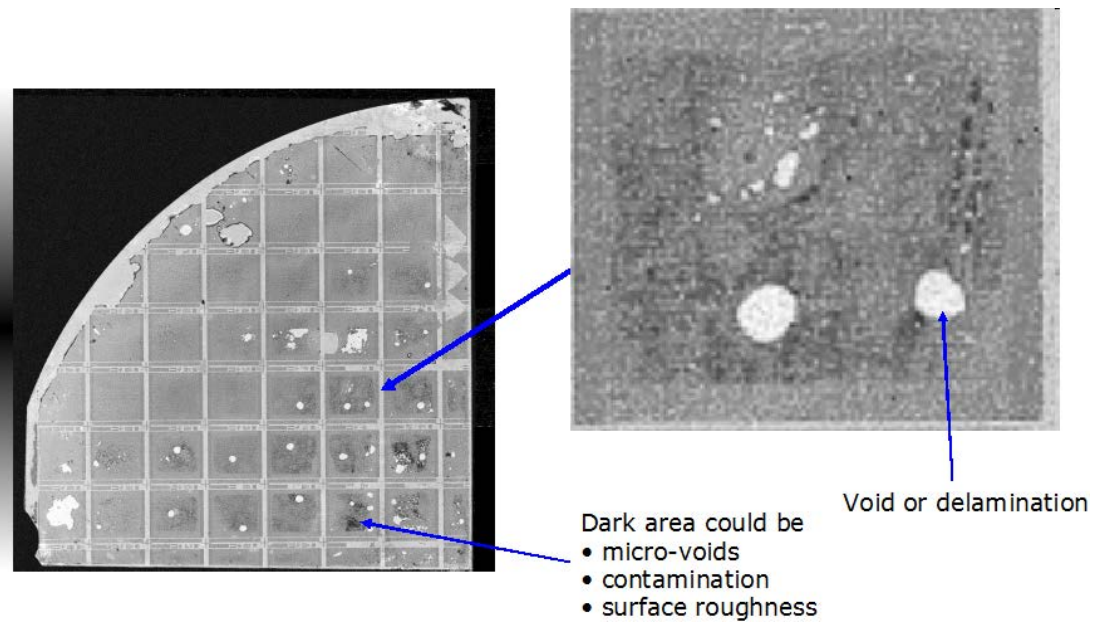


Figure 27: Ultrasonic image of wafer-bonded triple junction cell.

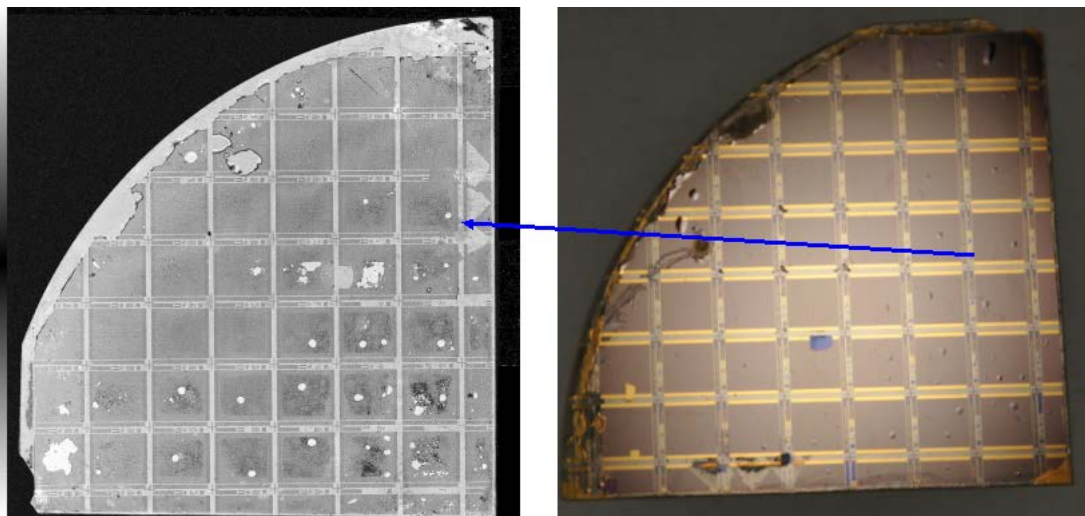


Figure 28: Comparison of ultrasonic image and optical image.

From Figure 28, it can be seen that there is correlation between the optical and ultrasonic image. The presence of dots as evidenced by the bubbles on optical image corresponds to white spots on the ultrasonic image. There is no correlation between an efficiency map and the ultrasonic image.

Transmission Electron Microscopy (TEM) of Wafer-Bonded Cells:

Kim Jones performed TEM analysis of wafer-bonded cells at NREL. This analysis can give information about the interface integrity and the presence of defects or impurities.

WB-051-1

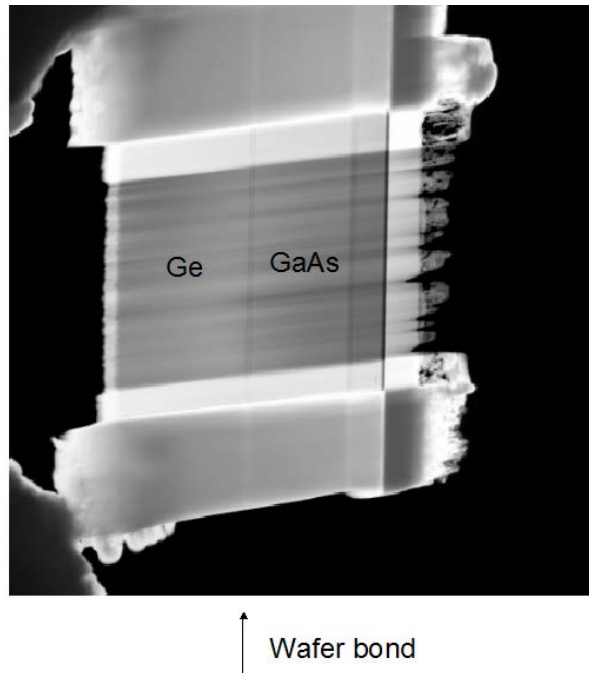


Figure 29: SEM image of FIB cross-section for wafer bonded InGaP/GaAs/Ge solar cell. The wafer bond interface is indicated by the arrow.

Figure 29 shows an SEM image of the focused ion beam (FIB) FIB cross-section of an InGaP/GaAs/Ge wafer bonded cell. Figure 29 clearly shows all three sub-cells; the dark lines indicate the tunnel junctions at interface of the top and middle cells and the middle and bottom cells. A more detailed image of the wafer-bonded interface is shown in Figure 30.

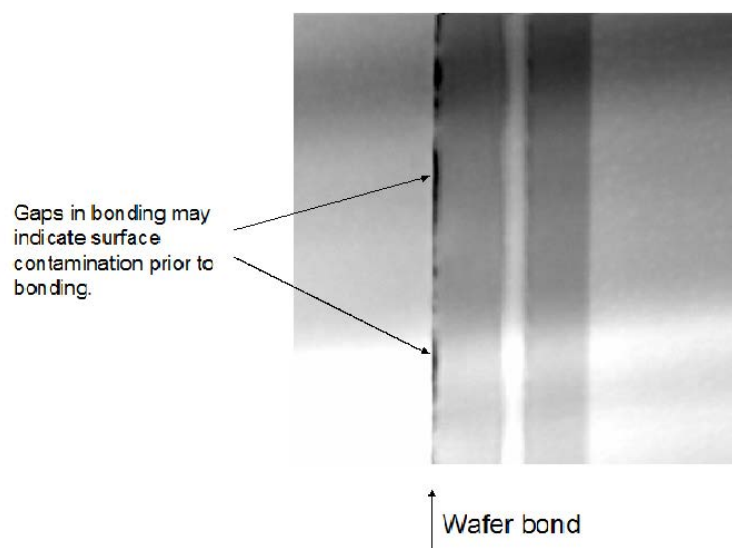


Figure 30: TEM micrograph of wafer bond interface for GaAs and Ge.

In Figure 30, dark and light areas are observed at the bonding interface. The dark areas have been probed using Energy Dispersive Spectroscopy (EDAX), which revealed the presence of Carbon, Ge, Ga, and As. The presence of impurities at the interface underlines the importance of the cleaning before the wafer bonding process. Impurities such as Carbon and other organics can influence the interface resistance, thereby affecting the fill factor of the processed cells.

Chemical Mechanical Polished Surfaces:

In order to access the surface quality of the CMP surfaces, we performed re-growth on CMP surface. FIB cross-sections and TEM were employed to study the re-growth interface. In Figure 31, a TEM cross-section of the re-growth interface of an InAlGaAs graded buffer layer is shown.

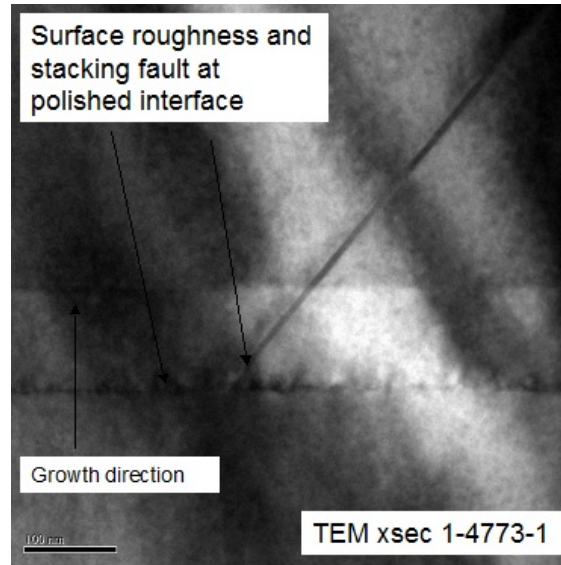


Figure 31: TEM X-section of re-growth interface.

TEM studies revealed that the CMP polished surface interface appears rough and may contain small particles or contamination. The presence of stacking faults that nucleate at the polished surface as shown in Figure 31 implies that there is some type of contamination prior to the re-growth step. It can be concluded that the re-growth layer has a high density of dislocations and stacking faults. Such a surface, if employed in wafer bonding, will create further voids and a very poor interface.

Photoluminescence Mapping:

Photoluminescence (PL) mapping is a very effective tool to analyze the cell performance at the wafer level, before the cells are diced and mounted onto carriers. PL mapping has been routinely performed on all our wafer bonded cells to evaluate the performance of the devices. A good PL intensity of the top cell clearly indicates that the cell is behaving well. A quantitative relationship between efficiency measured and the PL intensity needs more detailed study and statistical analysis.

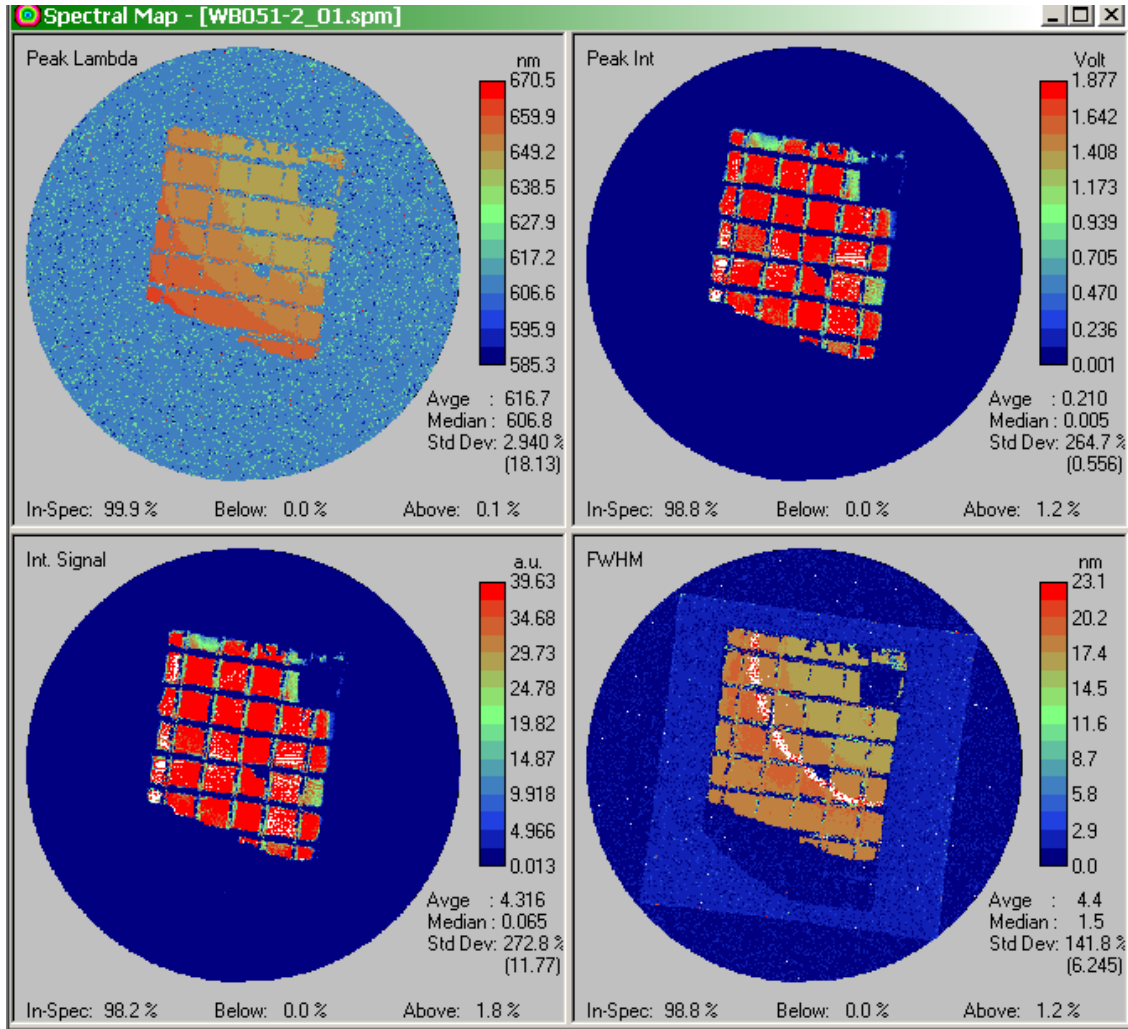


Figure 32: InGaP PL peak mapping analysis of InGaP/GaAs/Ge wafer bonded cells.

In Figure 32, InGaP PL peak analysis is presented. Four important peak parameters such as peak lambda (wavelength), peak Intensity (relative units), total integrated intensity under the peak, and full width at half maximum of the peak are plotted in figure 32. The analysis of these four parameters can provide good basis for quality assessment of the top cell. Cells with low efficiency performance, generally exhibit low PL intensities and relate to either poor carrier separation in the top cell p-n junction or shunts in the top cell. A similar kind of PL peak analysis can also be made for GaAs peak.

Task 6 – Reliability of Wafer Bonded Cells

The Subcontractor shall perform preliminary reliability measurements of the wafer-bonded interfaces by employing thermal cycling tests and high temperature operation tests of the fabricated solar cells. The tests shall consist of 200 cycles between -25 °C and +40 °C, and 500 hours exposure to 80 °C. The effect of thermal cycling on the integrity of the bonded interface shall be studied using IR Transmission microscopy. IR microscopy can reveal if any voids or delamination has occurred as a result of the thermal cycling. Efficiency of the cells shall also be monitored before and after thermal cycling. For this task, the Subcontractor shall use the triple junction wafer-bonded ELO cells with minimum efficiency of 25% under AM1.5D 1-sun conditions.

Milestone 6: The results of the reliability testing shall be provided in the Final Report.

Preliminary reliability measurements of the wafer-bonded interfaces were performed using thermal cycling of the fabricated solar cells. The tests consisted of 200 cycles between -25 °C and +40 °C, and 500 hours exposure to 80 °C.

Wafer-bonded triple-junction cells were first mounted onto ceramic carriers and wire bonded. The cells were tested before being placed in the thermal cycling chamber.

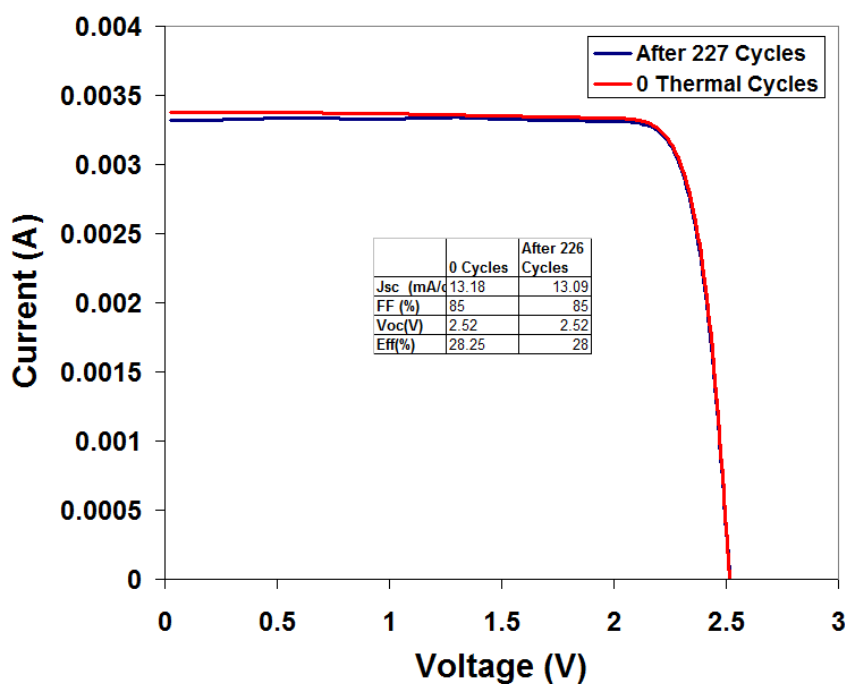


Figure 33: I-V curves measured before and after wafer-bonded triple-junction cells subjected to thermal cycling.

Figure 32 shows the IV curves measured before and after the wafer bonded cells were subjected to thermal cycling. It is clear from Figure 32 that thermal cycling has a very small effect on the performance of the cells. Specifically, Voc remained unchanged at 2.52 V after 227 thermal cycles.

Task 7 – Prototype Fabrication

The Subcontractor shall fabricate a prototype of a receiver for concentrator applications using wafer-bonded InGaP/GaAs-on-GaAs/InGaAs-on-InP triple-junction ELO solar cells.

Characterization shall be performed in a flash tester at 300 suns.

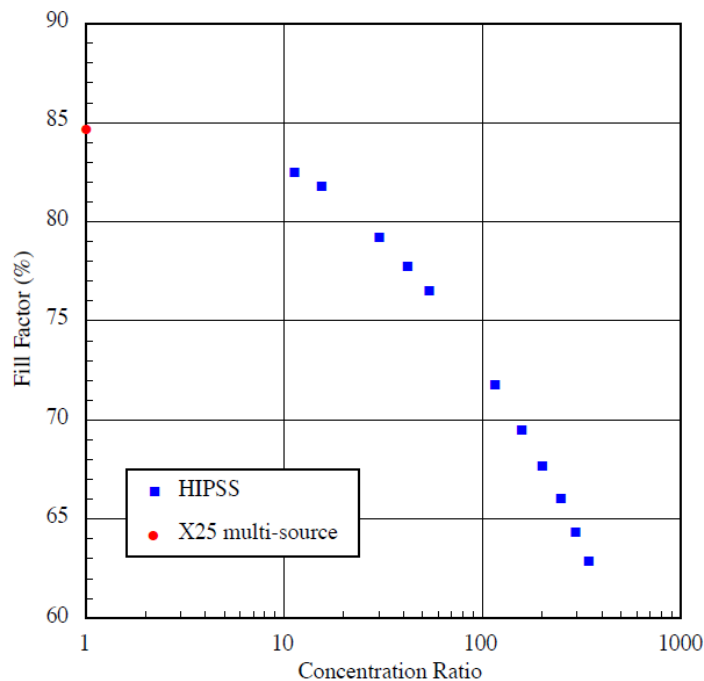
Final Deliverable: Three prototype receivers (metallized ceramic substrates of 1 inch x 1 inch) containing InGaP/GaAs-on-GaAs/InGaAs-on-InP wafer-bonded ELO solar cells of area $0.5 \times 0.5 \text{ cm}^2$. The receivers shall be capable of operating at intensities of at least 300 suns, fill factors $> 60\%$. Wafer bonded ELO cells with efficiencies $> 25\%$ @ AM1.5D under 1 sun shall be used for testing.

After processing the wafer-bonded triple-junction InGaP/GaAs/Ge structure into 0.25 cm^2 cells, the wafer is diced and individual cells are separated. Each cell is then mounted onto a ceramic carrier with epoxy or solder. Following that, wire or metal strip bonding is performed from the top of the bus bars onto probing pads on the ceramic carrier. Next, the wafer-bonded triple-junction cell is mounted in flash tester and tested for LIV performance as a function of intensity. The flash tester intensity is varied from 10 suns up to >300 suns.

FF vs. Concentration Ratio

Microlink WB-0053-H09
GaInP/GaAs/Ge Triple
April 13, 2011

HIPSS Data
Temperature: 25°C



Spectrum: ASTM G173 Direct
HIPSS PFN trigger settings: 263.8
Concentration = $\text{HIPSS } I_{sc} / \text{X25 1-sun } I_{sc}$

Figure 34: Wafer bonded triple junction cell bonded and tested under concentration.

LIV analyses were then performed to evaluate the efficiency, fill factor and Voc. The prototype cells were sent to NREL for measurements. In Figure 33, NREL measured data is plotted for fill factor versus illumination intensity for wafer-bonded triple-junction InGaP/GaAs/Ge cells. All the receiver prototypes were tested under flash testing conditions at NREL and operated up to 300 suns. It can be noted from Figure 33, that the fill factor of wafer-bonded cells decreased with increasing concentration. The fill factor value of close to 85% at 1 sun fell to 63% at 300suns. The deliverable milestone for this task was to demonstrate prototype bonded cells, which operate at 300suns with a minimum fill factor value of 60%. The data shown in figure 33 clearly indicates that the deliverable milestone for prototype cells has been achieved. However, the monotonic decrease of fill factor with increasing sun concentration indicates that the device resistance is controlling the cell performance at higher concentration. This could be due to imperfections or impurities at the bonded interface acting as resistive elements.

Additional Work:

MicroLink Simulators and Flash Tester Spectrum Measurements:

Andreas Afshin from NREL Solar Resource Characterization group measured the optical spectra of MicroLink's Alpha-Omega flash tester, Newport single source simulator, and TS Space Systems 3 lamp simulator. The Alpha-Omega flash tester produces optical pulses of 1 ms duration with constant illumination for 500 μ s near the middle of the pulse. The period between the flashes can be varied from 0.5 s to 1 s. Andreas Afshin used a customized photo-radiometer developed at NREL to measure the flash simulator spectrum at 50, 250, and 500 suns. These were the first such measurements made on the Alpha-Omega system and gave us good confidence regarding the spectral content of the optical pulse. Based on the measurements, the flash tester has been certified to be operating as Class A for spectral match under standard ASTM E-927-04. In Figure 34, the measured spectrum is compared in different wavelength zones with ASTM E-927-04 data.

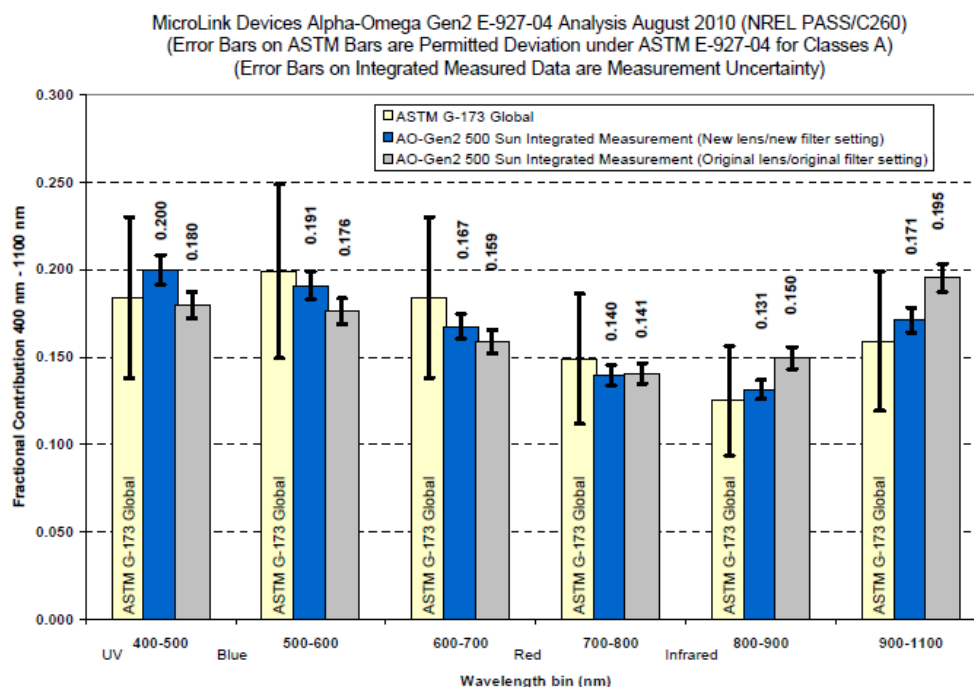


Figure 1. ASTM E-927-04 Class A band analysis of Spectral Irradiance data from the PASS for GEN2 pulsed simulator in August 2010 (blue). The measurement made using the original lens and filter position (gray) is shown for comparison.

NOTE: As long as the measurement error bars and "permitted Class A range error bars" overlap, one must conclude that the simulator is Class A. ONLY if the "error bars" do not overlap can one claim the simulator is not Class A.

Figure 35: Comparison of output spectrum of MicroLink's Alpha-Omega flash tester with ASTM E-927-04 data. Data courtesy of NREL.