

Solid-State Fault Current Limiter Development

Design and Testing Update of a 15kV SSCL Power Stack

DOE Report / Product Number - DOE/CH/11354

DOE Contract Number - DE-FC02-06CH11354

Solid-State Fault Current Limiter Development

Design and Testing Update of a 15kV SSCL Power Stack

DOE Report / Product Number - DOE/CH/11354

DOE Contract Number - DE-FC02-06CH11354

Technical Update, April 2012

DOE Project Manager

Mr. Stephen Waslo

EPRI Project Manager

Dr. Ram Adapa

Silicon Power Corporation Project Manager

Mr. Dante Piccone

DISCLAIMER OF WARRANTIES AND LIMITATION OF LIABILITIES

THIS DOCUMENT WAS PREPARED BY THE ORGANIZATION(S) NAMED BELOW AS AN ACCOUNT OF WORK SPONSORED OR COSPONSORED BY THE DEPARTMENT OF ENERGY (DOE). NEITHER DOE, ANY COSPONSOR, THE ORGANIZATION(S) BELOW, NOR ANY PERSON ACTING ON BEHALF OF ANY OF THEM:

(A) MAKES ANY WARRANTY OR REPRESENTATION WHATSOEVER, EXPRESS OR IMPLIED, (I) WITH RESPECT TO THE USE OF ANY INFORMATION, APPARATUS, METHOD, PROCESS, OR SIMILAR ITEM DISCLOSED IN THIS DOCUMENT, INCLUDING MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, OR (II) THAT SUCH USE DOES NOT INFRINGE ON OR INTERFERE WITH PRIVATELY OWNED RIGHTS, INCLUDING ANY PARTY'S INTELLECTUAL PROPERTY, OR (III) THAT THIS DOCUMENT IS SUITABLE TO ANY PARTICULAR USER'S CIRCUMSTANCE; OR

(B) ASSUMES RESPONSIBILITY FOR ANY DAMAGES OR OTHER LIABILITY WHATSOEVER (INCLUDING ANY CONSEQUENTIAL DAMAGES, EVEN IF EPRI OR ANY EPRI REPRESENTATIVE HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES) RESULTING FROM YOUR SELECTION OR USE OF THIS DOCUMENT OR ANY INFORMATION, APPARATUS, METHOD, PROCESS, OR SIMILAR ITEM DISCLOSED IN THIS DOCUMENT.

THE FOLLOWING ORGANIZATION(S), UNDER CONTRACT TO DOE, PREPARED THIS REPORT:

Electric Power Research Institute

3420 Hillview Ave

Palo Alto, CA 94304

Silicon Power Corporation

275 Great Valley Parkway

Malvern, PA 19355

ACKNOWLEDGMENTS

The following organization(s), under contract to the Department of Energy (DOE), prepared this report:

Electric Power Research Institute
3420 Hillview Ave
Palo Alto, CA 94304

Principal Investigator
Dr. Ram Adapa

Silicon Power Corporation
275 Great Valley Parkway
Malvern, PA 19355

Principal Investigator
Mr. Dante Piccone

This report describes research sponsored by DOE.

DOE is thankful to following participants in this program for technical inputs, feedbacks and financial support. Without their vision and interest the SSCL would not have reached the stage where it is today. Looking forward to their continued support to finish the program and put the reliable, compact, and cost effective product in the market. This product targets the needs of utilities of today and tomorrow.

- EPRI
- Con Edison
- TVA
- Center Point Energy
- Mid American Energy
- PP&L Corporation
- Central Hudson
- First Energy
- Southern Company
- South Carolina Gas & Electric
- NYPA
- San Diego Gas and Electric

ABSTRACT

The Solid-State Fault Current Limiter (SSCL) is a promising technology that can be applied to utility power delivery systems to address the problem of increasing fault currents associated with load growth. As demand continues to grow, more power is added to utility system either by increasing generator capacity or by adding distributed generators, resulting in higher available fault currents, often beyond the capabilities of the present infrastructure.

The SSCL is power-electronics based equipment designed to work with the present utility system to address this problem. The SSCL monitors the line current and dynamically inserts additional impedance into the line in the event of a fault being detected. The SSCL is based on a modular design and can be configured for 5kV through 69kV systems at nominal current ratings of 1000A to 4000A.

Results and Findings

This report provides the final test results on the development of 15kV class SSCL single phase power stack. The scope of work included the design of the modular standard building block sub-assemblies, the design and manufacture of the power stack and the testing of the power stack for the key functional tests of continuous current capability and fault current limiting action.

Challenges and Objectives

Solid-State Current Limiter technology impacts a wide spectrum of utility engineering and operating personnel. It addresses the problems associated with load growth both at Transmission and Distribution class networks. The design concept is pioneering in terms of developing the most efficient and compact power electronics equipment for utility use. The initial test results of the standard building blocks are promising. The independent laboratory tests of the power stack are promising. However the complete 3 phase system needs rigorous testing for performance and reliability.

Applications, Values, and Use

The SSCL is an intelligent power-electronics device which is modular in design and can provide current limiting or current interrupting capabilities. It can be applied to variety of applications from distribution class to transmission class power delivery grids and networks. It can also be applied to single major commercial and industrial loads and distributed generator supplies. The active switching of devices can be further utilized for protection of substation transformers. The stress on the system can be reduced substantially improving the life of the power system. It minimizes the voltage sag by speedy elimination of heavy fault currents and promises to be an important element of the utility power system.

DOE Perspective

This development effort is now focused on a 15kV system. This project will help mitigate the challenges of increasing available fault current. DOE has made a major contribution in providing a cost effective SSCL designed to integrate seamlessly into the Transmission and Distribution networks of today and the future.

Approach

SSCL development program for a 69kV SSCL was initiated which included the use of the Super GTO advanced semiconductor device which won the 2007 R&D100 Award. In the beginning, steps were identified to accomplish the economically viable design of a 69kV class Solid State Current Limiter that is extremely reliable, cost effective, and compact enough to be applied in urban transmission. The prime thrust in design and development was to encompass the 1000A and the 3000A ratings and provide a modular design to cover the wide range of applications.

The focus of the project was then shifted to a 15kV class SSCL. The specifications for the 15kV power stack are reviewed. The design changes integrated into the 15kV power stack are discussed. In this Technical Update the complete project is summarized followed by a detailed test report. The power stack independent high voltage laboratory test requirements and results are presented.

Keywords

Solid State Current Limiter, SSCL, Fault Current Limiter, Fault Current Controller, Power electronics controller, Intelligent power-electronics Device, IED

CONTENTS

1 INTRODUCTION	1-1
The Motivation for Solid-State Fault Current Limiter Development	1-1
Project Overview	1-1
SSCL Applications	1-2
Project Status	1-4
2 SOLID-STATE CURRENT LIMITER SPECIFICATIONS	2-1
Overview of Specifications	2-1
System Functional Description	2-2
3 SOLID-STATE CURRENT LIMITER DESIGN OVERVIEW	3-3
Overview of course of the project	3-3
Initial Design	3-3
New Concept.....	3-5
Design changes over the course of the project.....	3-11
4 TEST REQUIREMENTS AND PROCEDURES.....	4-1
Factory Test	4-1
KEMA Current Limiting Tests for the Power Stack	4-2
Measurement Details.....	4-2
Test Details	4-3
KEMA Continuous Current Test for the Power Stack.....	4-4
Measurement Details.....	4-4
Test Details	4-4
5 TEST RESULTS	5-1
Current Limiting Test Results	5-1
Test Waveforms	5-2
Conclusion	5-8
Continuous Current Test Results.....	5-8
Test Waveforms	5-9
Temperature Stability Data	5-13
Conclusion	5-13
Summary of Test results and Compliance Table	5-14
6 SUMMARY	6-1
A REFERENCE	A-1

LIST OF FIGURES

Figure 1-1: Bus Tie Application	1-3
Figure 1-2: Radial Feeder Application	1-3
Figure 3-1: SSCL Circuit Concept	3-4
Figure 3-2: Standard Building Block for SSCL - Initial	3-5
Figure 3-3: Negative Voltage Rail during resonant Turn off (Ch1: yellow waveform)	3-6
Figure 3-4: Negative Voltage Rail during Hard Turn off (Ch1: yellow waveform)	3-7
Figure 3-5: Revised SSCL Concept	3-8
Figure 3-6: Modified Standard Building Block.....	3-8
Figure 3-7: 15kV, 1200A Power Stack (48" (W) X 62" (D) X 70" (H)).....	3-9
Figure 3-8: Busbar Hole Pattern Detail.....	3-10
Figure 3-9: Left – Chiller used for the continuous current test: Right – Building Blocks mounted on the frame with the cooling circuit connections made.....	3-11
Figure 3-10: Bus bar connection changes – left: previous arrangement – right: new arrangement	3-12
Figure 3-11: Frame modification and CLR placement	3-13
Figure 4-1: Unit under test at factory (Silicon Power, Malvern, PA)	4-2
Figure 4-2 SBB Test Circuit for Power Stack.....	4-3
Figure 4-3: Test Circuit for Continuous Current Carrying Test for the Power Stack	4-5
Figure 5-1: Unit under test at KEMA high voltage lab facility (KEMA, Inc. Chalfont, PA)	5-1
Figure 5-2: Screen shot of the 11.6kA sym RMS available fault current trial (first attempt)- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage.....	5-3
Figure 5-3: Screen shot of the 11.6kA sym RMS available fault current trial (second attempt)- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage.....	5-4
Figure 5-4: Screen shot of the 17.4kA sym RMS available fault current trial- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage	5-5
Figure 5-5: Screen shot of the 23.2kA sym RMS available fault current trial- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage	5-6
Figure 5-6: Zoomed in view of turn-off– 11.6kA sym RMS available fault current	5-7
Figure 5-7: Zoomed in view of turn-off- 17.4kA sym RMS available fault current.....	5-7
Figure 5-8: Zoomed in view of turn-off- 23.2kA sym RMS available fault current.....	5-8
Figure 5-9: Current Sharing Run 1 – Block – 1(Ch 1)*, 2(Ch 3), 3(Ch 4)* and the main current (Ch 2).....	5-10
Figure 5-10: Current Sharing Run 1 – Block –4(Ch 1)*, 5(Ch 3), 6(Ch 4)* and voltage across SSCL (Ch 2)	5-10
Figure 5-11: Current Sharing Run 2 - Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 2).....	5-11
Figure 5-12: Current Sharing Run 2 - Block –4(Ch 2), 5(Ch 3), 6(Ch 4) and voltage across SSCL (Ch1).....	5-11
Figure 5-13: Current Sharing Run 3- Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 2)	5-12
Figure 5-14: Current Sharing Run 3- Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 2)	5-12

LIST OF TABLES

Table 1-1: Project Deliverables	1-2
Table 2-1: SSCL Specifications Overview	2-1
Table 3-1: SSCL Power Stack Details	3-10
Table 5-1: Test results – Current Limiting test for the 15kV power stack	5-2
Table 5-2: Test results - Continuous Current Test for the 15kV stack.....	5-8
Table 5-3: Temperature measured on each building block – run 1	5-13
Table 5-4: Temperature measured on each building block – run 2	5-13
Table 5-5: Temperature measured on each building block – run 3	5-13

1 INTRODUCTION

The Motivation for Solid-State Fault Current Limiter Development

The increase in available fault current levels due to increased distributed generation capacity and increased load has stressed many transmission and distribution substations to their limits. In some cases, fault current levels are exceeding the interrupting capability of existing substation circuit breakers. This increase in fault current levels either requires the replacement of large numbers of substation breakers or the development of some means to limit fault current.

The Solid State Current Limiter, or SSCL, is a power-electronics based system designed to limit the fault current in Transmission and Distribution applications. The SSCL monitors the current in the main bus of the system and dynamically inserts additional impedance into the line in the event of a fault. The SSCL responds rapidly to fault events, within 100 μ s, and is capable of responding to successive fault events. As a power-electronics based system, the SSCL does not require a separate cryogenics plant and this enables the SSCL to be designed as a compact, efficient unit. The SSCL includes a closed circuit forced cooling system with an external heat exchanger. A control cabinet or panel with a Human Machine Interface (HMI) is mounted on the exterior of the system. The SSCL power stack under development in this project was fabricated and tested on an open-air frame.

The ultimate objective of this project is to develop a Solid State Current Limiter (SSCL) to mitigate fault current issues and to take advantage of benefits such as the ability to support new capacity and to allow grid operations alternatives.

Project Overview

The scope of work of this stage of the EPRI SSCL development project is to design and manufacture a 15kV, 1200A RMS rated, single phase SSCL power stack capable of limiting a fault current of 23kA symmetric RMS to 9kA for a duration of 30 cycles and then demonstrate the continuous current and current limiting capabilities of the power stack through factory testing and independent high voltage laboratory testing. The development of the next generation SGTO power electronics device is also being undertaken as part of the SSCL project under separate funding; this device level development will be discussed in a separate report.

A summary of the deliverables for this project may be found in Table 1-1.

Table 1-1: Project Deliverables

Phase	Description	Deliverable
1	Build and factory test 15kV 1200A 1 phase Power stack	Test report on power stack
1(a)	Demonstrate symmetric SGTO component	Report on symmetric SGTO component

The scope of work for phase 1 of this project is to build and factory test a single phase power stack rated for 1200A that would be suitable for 15kV class applications. The scope also includes testing of the key functionalities of the power stack which include continuous current and current limiting test, with the results being provided in a test report contained within this Technical Update.

SSCL Applications

The SSCL can be used in the following applications:

- Bus tie applications
 - The SSCL may be used directly in a transformer bus, as substation bus tie (sync bus; see Figure 1-1 where the SSCL is shown in yellow) and in a high capacity tie for asset/load tie between substations.
- Radial feeder applications
 - The SSCL may be applied in the output of an Independent Power Producer, or a radial feeder application (see Figure 1-2), where a specific level of let-through current will be required to support downstream relay protection coordination.

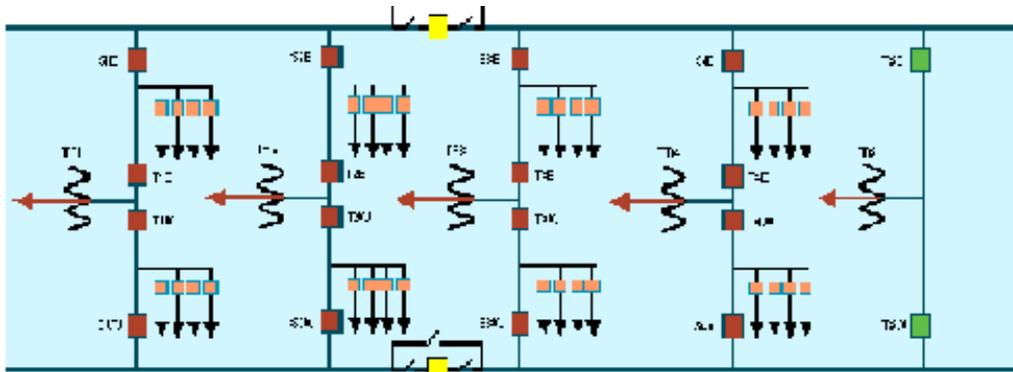


Figure 1-1: Bus Tie Application

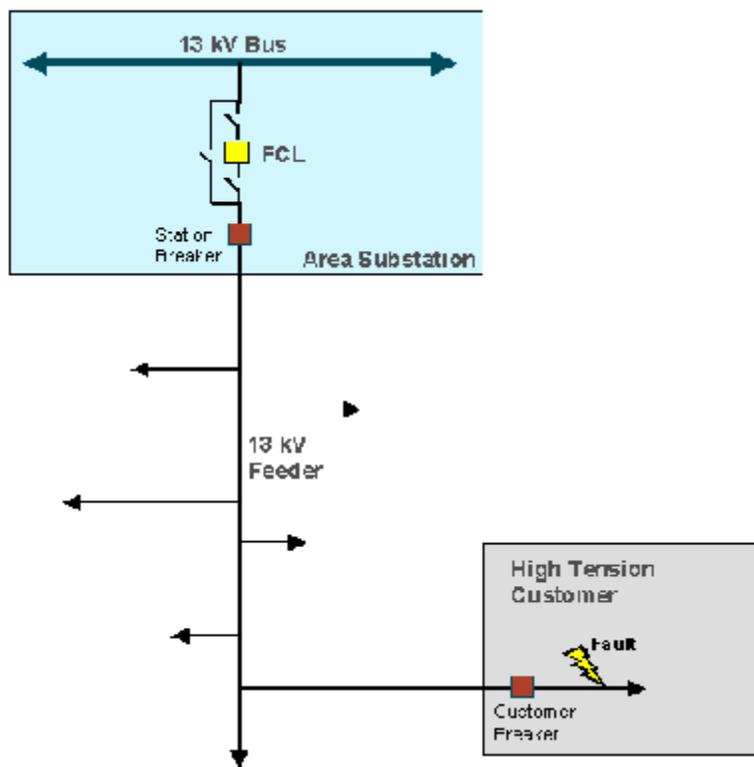


Figure 1-2: Radial Feeder Application

The primary use of the SSCL is to limit fault currents to a level that will support downstream protection coordination. The SSCL carries additional potential benefits, including the ability to facilitate:

New Capacity - Solid-state current limiters could be applied to new capacity additions and/or “surgically” at strategic locations, such as substation bus ties, to effectively mitigate the fault current from multiple generation sources. This would provide a flexible tool that could be used to accommodate new capacity from generation or transmission distributed or aggregate generation energy storage.

Grid Operations Alternatives - The new functionality made possible by the flexibility of power electronics will also enable innovative alternatives in operation of the grid. For example, power electronics can mitigate unexpected load increases or major asset failures with temporary generation, protect “line commutated” FACTS devices from close proximity faults and improve the performance of superconducting cables.

Superconducting Cables - A solid state current limiter added in series with a superconducting cable can improve the cable's performance and enable design of smaller cable sizes, as well as eliminate loss of superconducting cable operation during cryogenic recovery time following an external fault. The insulation system of a superconducting cable is likely to have limited strength because of the need for minimal mechanical cross section bracing spanning the vacuum segment. It may not be capable of handling the magnetic forces occurring in the worst case of a high current fault, particularly in transmission applications, which will draw fault currents from higher impedance parallel paths. The solid state current limiter will be an essentially enabling adjunct to the regular use of superconducting cables.

Inrush Current - The Solid State Current Limiter has a unique capability to limit inrush current. This may be of particular benefit in mitigating stress on generator shafts, while preserving the reliability benefits of multi-shot re-closure on generator buses, particularly as distributed generators are deployed at various voltage levels and locations across utility grids.

Open Access - Because of the critical role of solid state current limiting as an early enabler within EPRI/DOE’s Roadmap Document to support “open access,” transmission and generation capacity increases, energy storage needed for improved asset utilization and renewable economics, distributed and aggregate generation, this new functionality is also being pursued in a parallel development effort for transmission level solid state current limiters using superconducting and other technologies.

The SSCL also has the capability to provide real time monitoring and control and can function as an element of the Smart Grid.

Project Status

The design and test of the modular sub-assemblies for the SSCL has been completed, followed by Factory Acceptance Tests and an Independent High Voltage Laboratory (KEMA, Inc.). These tests have proven that the SSCL power stack has met the test plan and requirement.

2 SOLID-STATE CURRENT LIMITER SPECIFICATIONS

Overview of Specifications

The primary use of the SSCL is to limit fault currents to a level that will support downstream protection coordination. The SSCL interrupts or limits fault current from new generation or transmission, reduces switching surges, and offers an environmentally benign alternative to circuit breakers. The SSCL also has the capability to provide real time monitoring and control and may function as an element of the Smart Grid.

An overview of the SSCL specifications for this project may be found in Table 2-1. Note that there are no explicit dielectric requirements other than the power stack design must adhere to appropriate strike and creepage distances for a 15kV class unit. The power efficiency goal of the SSCL is >99%.

Table 2-1: SSCL Specifications Overview

Parameter	Value
Rated Maximum Voltage, kV RMS	15.5
Rated Maximum Continuous Current, Ampere RMS	1200
Rated Power Frequency, Hz	60
Available fault current, kA symmetric RMS	23
Available fault current, kA peak asymmetric	55
Rated Let-thru Current, kA RMS	9 (+0%/-10%)
Rated Let-thru Current, kA peak	21.6 (+0%/-10%)
Rated Let-thru Current Duration, cycles	30
Power Frequency 1 min dry kV, RMS	N/A ¹
Impulse, Full-wave Withstand, kV peak	N/A ¹
Impulse, Chopped Wave (2uS) Withstand, kV peak	N/A ¹
Partial Discharge at 16.5kV, pC	N/A ¹
Rated Power Factor Measurement	N/A ¹

Rated Insulation Resistance at 1000V DC Megohmmeter	13000 M-ohm	N/A ¹
Ambient Temp, Degree C		-30 to +40
Storage temp, Degree C		-30 to +40
Relative Humidity		TBD ²
Rated Control Power, V DC		125
Audible Noise at 6 feet, dB		N/A ³
System response time, detection to initiation of limiting behavior, μ s		100

¹ The SSCL Power Stack design shall observe all strike and creepage distances for a 15kV class unit but no dielectric tests will be performed on the power stack

² The relative humidity specification for the tests is still to be determined. A preliminary value is 15%-95% non-condensing for indoor units and 15%-100% non-condensing for outdoor units

³ No audible noise tests will be performed on the SSCL power stack

A complete set of specification for this project can be found in [5].

System Functional Description

The main purpose of the SSCL is to sense and limit fault current to a level that downstream protective equipment can handle. In normal operation, the SSCL transmits the bus current to downstream elements through a low impedance path. In the event of a fault, the SSCL senses the fault current and when the magnitude of the fault current and the rate of rise of the fault current exceeds the preset, programmable thresholds, the SSCL acts to rapidly (within 100 μ s) limit the current to a level that the downstream protective devices can withstand until they trip or open up as designed. This limited level of current is called the let-through current. The SSCL is capable of withstanding the let-through current for a limited number of cycles (30 cycles), until the downstream protective devices act to interrupt the current. The SSCL is capable of supporting a re-closure within a half-second (30 cycles) and can support a total of three sequential re-closure events before the SSCL system suspends its operation to allow the fault to clear.

Under the current scope of the project, the single phase SSCL power stack was designed as a 15kV class, 1200A RMS system capable of limiting a 23kA symmetric RMS fault current to a let-thru current of 9kA for 30 cycles.

3 SOLID-STATE CURRENT LIMITER DESIGN OVERVIEW

Overview of course of the project

The Current Limiter design went through changes in the course of this project and this chapter describes the initial changes, the new concept and final design changes in order to develop a working 15kV, 1200Arms single phase Solid State Current Limiter (SSCL). The following were important events and milestones that led to various changes and details of each phase of changes are discussed in the sections to follow.

- Single Building Block design test – The initial design concept which uses a resonant turn-off topology (more details to follow) was tested and it resulted in unwanted turn-off of the devices. This resulted in change in concept of circuit from resonant turn-off to hard turn-off.
- High Voltage Laboratory testing in September 2010 – The varistors were not able to clamp the voltage during this test which led to the change in design value of this element of the circuit.
- High Voltage Laboratory testing in Jan 2011 – The system was able to turn-off but was not able to sustain the turn-off and the mechanical stresses and wear and tear after the attempt led to changes in the placement and bracing of the Current Limiting Reactor's (CLR) and certain design changes in the power supply and gate drive board, snubber circuit and the busbar configuration.

Initial Design

The Solid-State Current Limiter, or SSCL, consists of a series of Super-GTO (SGTO) power electronic devices. In the design concept at the commencement of the project, the SSCL consisted of two current paths: a normal operation path of low impedance and a fault current response path of high impedance. An auxiliary circuit was used to assist in the transfer of the current from the low impedance path to the high impedance path.

In this circuit, in normal operation, the current passes through the low impedance path associated with the main SGTO switches as shown in Figure 3-1. Upon detection of a fault, the auxiliary circuit acts to quickly reduce the current in the main branch to zero. The SGTOs then turn off and current is forced to flow through the current limiting inductor. This effectively inserts additional impedance into the circuit and reduces the fault current from its peak value to a lower value (the let-through current) that the existing downstream circuit breakers can handle.

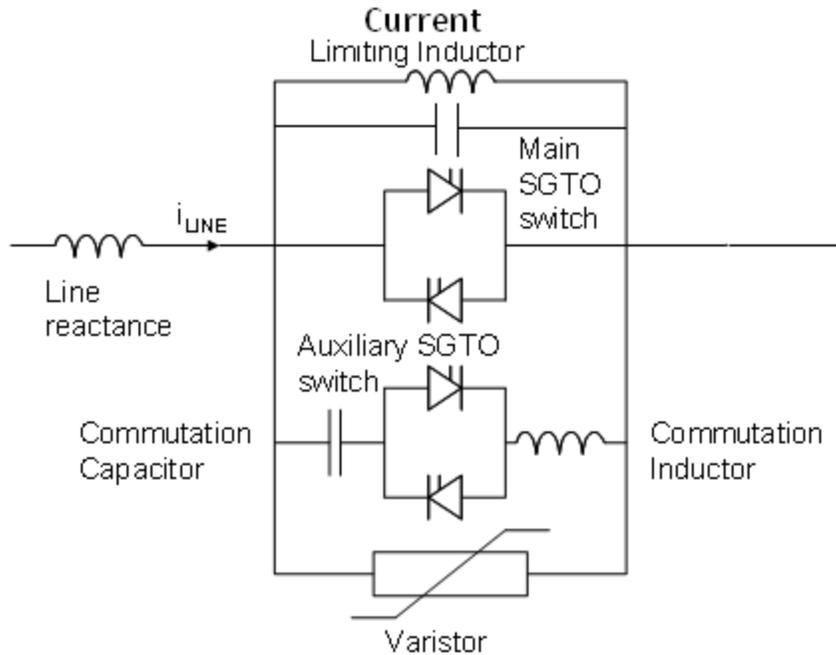


Figure 3-1: SSCL Circuit Concept

The SSCL is based on a modular design, featuring standard building blocks. The standard building blocks are rated for 4kV and 2000Arms continuous.

An example of the initial design building block is shown in Figure 3-2. Each building block consists of six (6) main SGTO modules and four (4) auxiliary modules, along with the required control boards, power supplies, varistors, commutation capacitor and snubber capacitors. Each building block was then connected to a current limiting inductor. Note that the only function of the current limiting inductor shall be to limit the fault current to an acceptable value; it is not designed to carry the normal operating current in a building block bypass mode.

These building blocks were then meant to be connected in series to achieve the required voltage rating for the system.

The main electrical connection to the SSCL will be achieved through the bushings on the top of the enclosure. The system control cabinet is mounted on the exterior of the SSCL enclosure and provides a local operator interface. A remote operator interface can also be supported.

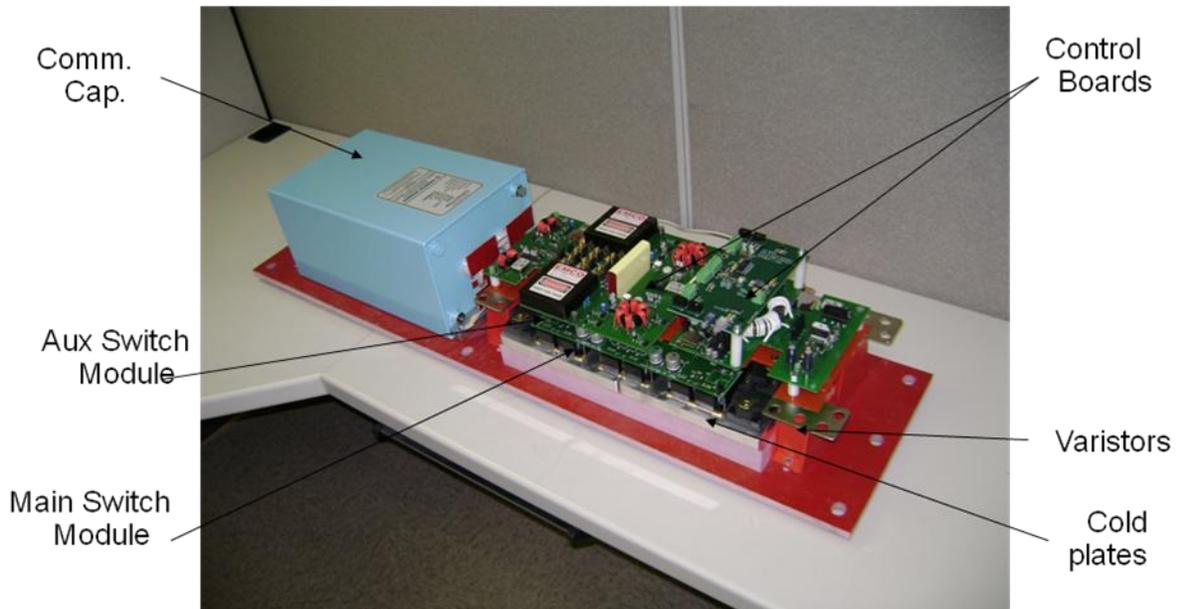


Figure 3-2: Standard Building Block for SSCL – Initial Concept

New Concept

The initial testing of the SSCL sub-assemblies revealed that some of the SGTO modules suffered from inadvertent, unwanted, turn on events. Because of these issues, the SSCL underwent certain design changes during the course of the project.

These unwanted turn-on events were extensively investigated and several modifications to the circuit were implemented to mitigate the noise issues that appeared to be causing these events. The gate drive boards were re-designed to utilize fiber-optic connectors rather than the hard wired connection originally envisioned. The snubber circuits on the auxiliary modules were enhanced and a series of chokes installed to limit noise. These changes did not completely eradicate the unwanted turn on events.

The next stage of the investigation revealed that the gate board power supply was being pulled to a level that was unable to maintain the modules in the off state. Multiple attempts were made to increase the capabilities of the power supply to correct this. Even with a DC bench power supply, the gate board negative voltage rail would still collapse (Figure 3-3) and allow the modules to turn on intermittently. The remaining limiting factor seemed to be the gate buffer board within the modules themselves.

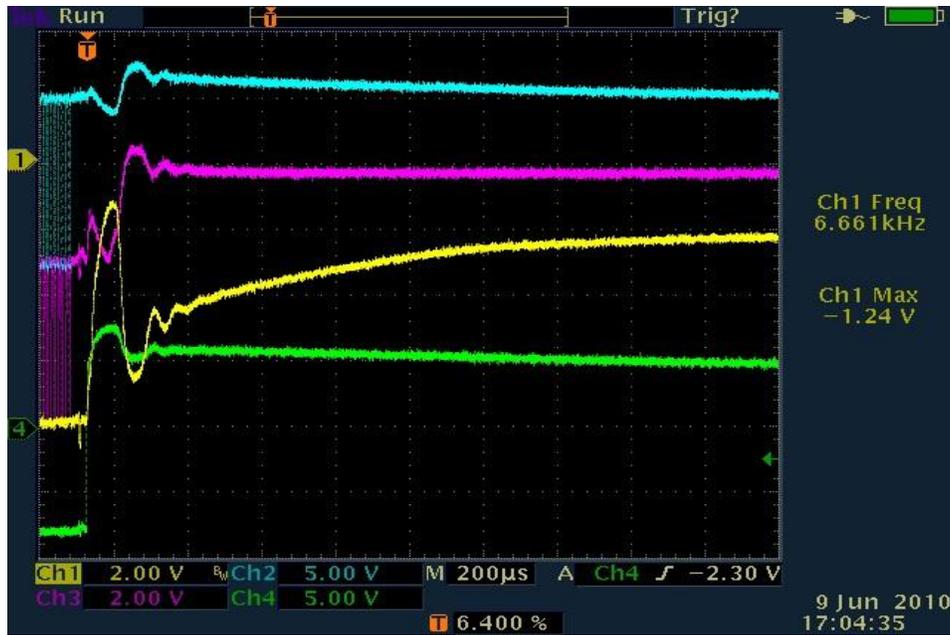


Figure 3-3: Negative Voltage Rail during resonant Turn off (Ch1: yellow waveform)

Faced with a re-design of the gate buffer board and the corresponding schedule implications, other solutions were reviewed. The decision was made to alter the SSCL circuit to remove the auxiliary modules, commutation capacitor and commutation inductor and to adopt a hard turn off based approach for the SSCL. This approach has the advantage of removing some of the load on the negative power rail of the gate drive boards (Figure 3-4), because four of the SGTO modules in the sub-assembly are removed. The removal of the commutation capacitor allows the capacitor trickle charge board to be removed and also reduces the load on the sub-assembly floating power supply board. These changes significantly reduce the size of the modular sub-assemblies, or standard building blocks.

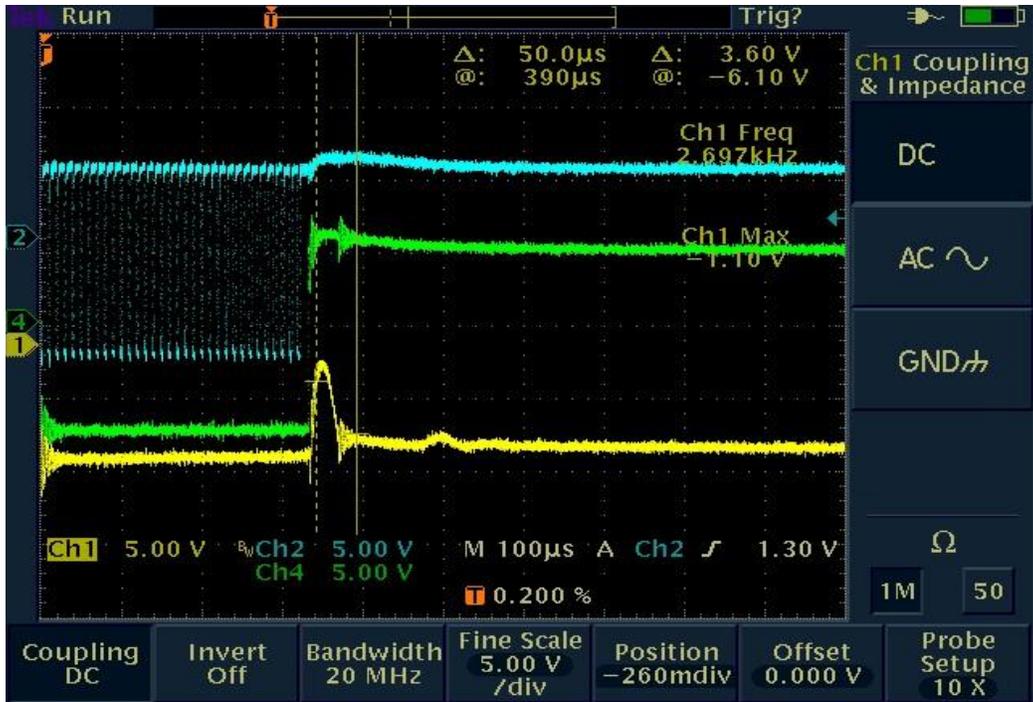


Figure 3-4: Negative Voltage Rail during Hard Turn off (Ch1: yellow waveform)

The SSCL now consists of a series of Super-Gate Turn Off thyristor (SGTO) power electronic devices that carry the current in normal operation, as shown in Figure 3-5. Upon detection of a fault, the SGTOs then turn off and current flows through the current limiting inductor. This effectively inserts additional impedance into the circuit and reduces the fault current from its peak value to a lower value (the let-through current) that the existing downstream circuit breakers can handle.

The sub-assemblies are now simplified compared to the previous approach (see Figure 3-6). The modification to use the hard turn off approach carries other implications. In particular, the hard turn off capability of a single building block is 1000A. In order to provide appropriate margin above the nominal rated current of the system (1200A RMS), the design was modified to use two parallel strings of building blocks, giving a hard turn off capability at the system level of 2000A. The controls were also modified to provide a projection of the current based the derivative of the current to provide additional margin for turn off.

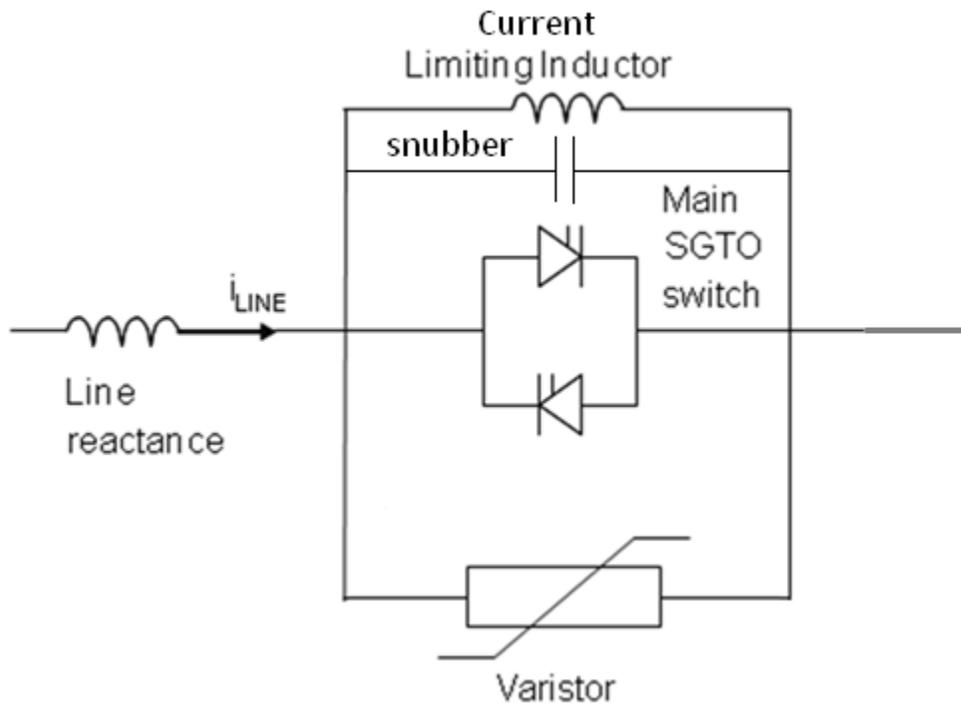


Figure 3-5: Revised SSCL Concept

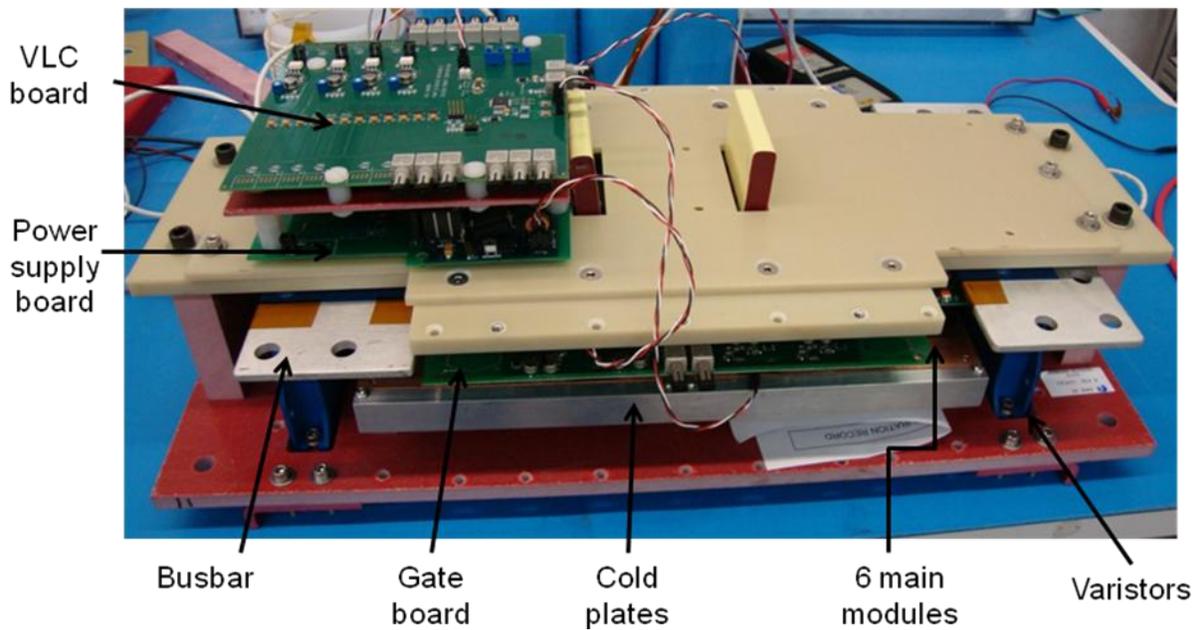


Figure 3-6: Modified Standard Building Block

The use of two parallel strings of building blocks also has implications for the thermal management system. In this case, the nominal current per string drops to 600A RMS, compared with the original concept of 1200A RMS passing through every building block. This reduces the losses per building block to approximately 1kW and significantly reduces the thermal load on the system. This allows the SGTO power electronics modules to operate at a lower junction temperature which in turns boosts their reliability.

The final power stack consists of a series and parallel array of building blocks as shown on the left hand side of Figure 3-7. The Current Limiting Reactors (CLRs) are in the centre of the unit. The free-standing control cabinet is shown on the left of the open-air frame. A de-ionized water / glycol closed circuit cooling system is used to maintain the temperature of the building blocks.

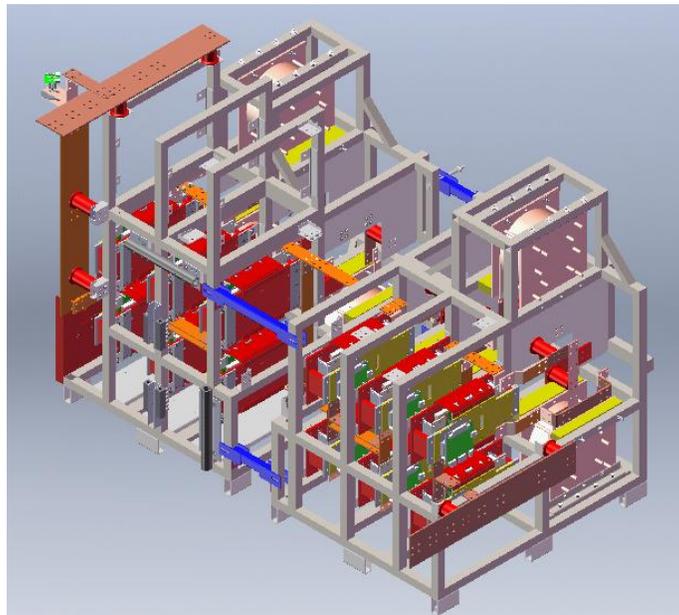


Figure 3-7: 15kV, 1200A Power Stack (48" (W) X 62" (D) X 70" (H))

In the final unit, these power stacks will be placed inside an enclosure; in this phase of the project, the blocks are mounted on an open air frame to allow the key functional testing to proceed. An external radiator bank and pump allows forced cooling of the standard building blocks.

The SSCL construction is rugged and durable and consists of a set of sub-assemblies mounted on an aluminum or steel frame. This same frame has been transported in and out of the KEMA test facility without any mechanical damage to the device or sub-assemblies. The building block and CLR mountings were designed to be securely mounted to the frame and withstand all forces associated with the weight of the assembly, the continuous operation current and the fault current event. The buswork for the power stack was designed to carry the continuous operating current indefinitely and the fault and let thru currents for 30 cycles. The buswork has been designed to provide sufficient bracing to withstand the mechanical stresses of the continuous operation current and the fault current. The power stack and building block buswork are designed to

standard NEMA bolt-hole pattern using 1/2" hardware for connection to other circuit elements as shown in Figure 3-8.

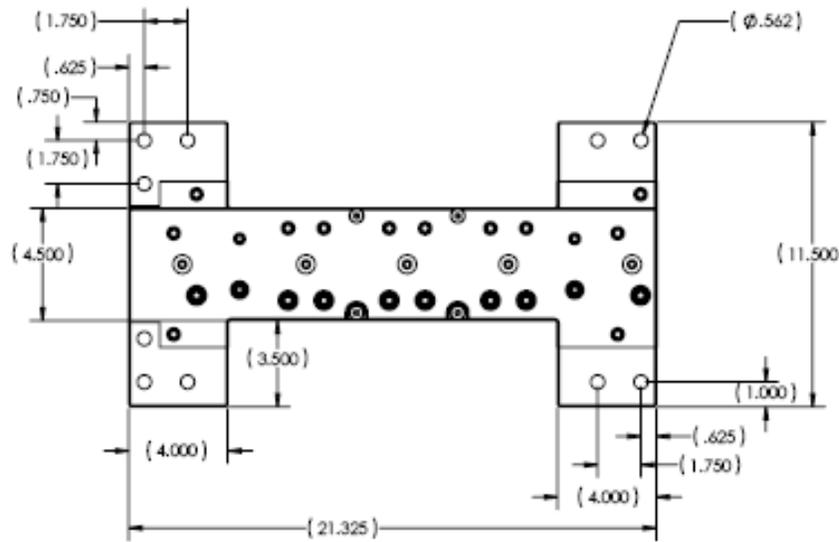


Figure 3-8: Busbar Hole Pattern Detail

The SSCL power stack thermal design includes a closed circuit, forced cooling system to remove heat from, and regulate the operating temperature of, the SGTO modules such that their operating temperature remains at or below the manufacturer’s rated operating temperature of 125°C. The closed circuit cooling system utilizes an external heat exchanger to dissipate the heat load to the ambient air. The closed circuit cooling system was chosen such that it is capable of removing the energy associated with the conduction and switching losses of the power electronics modules in normal operation plus a 20% overload capability. The closed circuit cooling system utilizes a cold-plate based approach (the SGTO modules are mounted on the cold-plates) with coolant circulating from a feed manifold, through the passages of the cold plate before returning to a drain manifold and the external heat exchanger and pump station. The cooling system that was chosen (Coldshot Chiller) includes a valve, flow gauge, pressure gauge and temperature gauge to monitor the status of the fluid. The flow rate of the fluid is sufficient as to provoke a turbulent flow in the cold plates to ensure optimum thermal efficiency. The heat exchanger shall provide sufficient cooling fans as to accommodate the full thermal load of the system plus 20% overload. Figure 3-9 shows the chiller used for the cooling system and the building blocks mounted on the frame with the connections to the cold plates made. The power stack details are presented in the table below:

Table 3-1: SSCL Power Stack Details

Item	Value
12 SBB Stand dimensions	48" (W) X 62" (D) X 70" (H)
Heat exchanger dimensions	61" (D) x 40" (W) x 75" (H)
Control cabinet dimensions	72" (h) x 42" (w) x 28" (d)
Combined weight	4000 lbs (approx)
Busbar connection tab dimensions	2 each: 0.562" hole, 1 3/4" center to center spacing, on 1/4"

	thick copper bus (nickel/silver coated tab). Tab is 4" x 2" x 1/4"
Control cabinet power	120V RMS, 1 phase, 20A RMS
Heat Exchanger power	3 phase, 460/3 PHASE, 35 KW

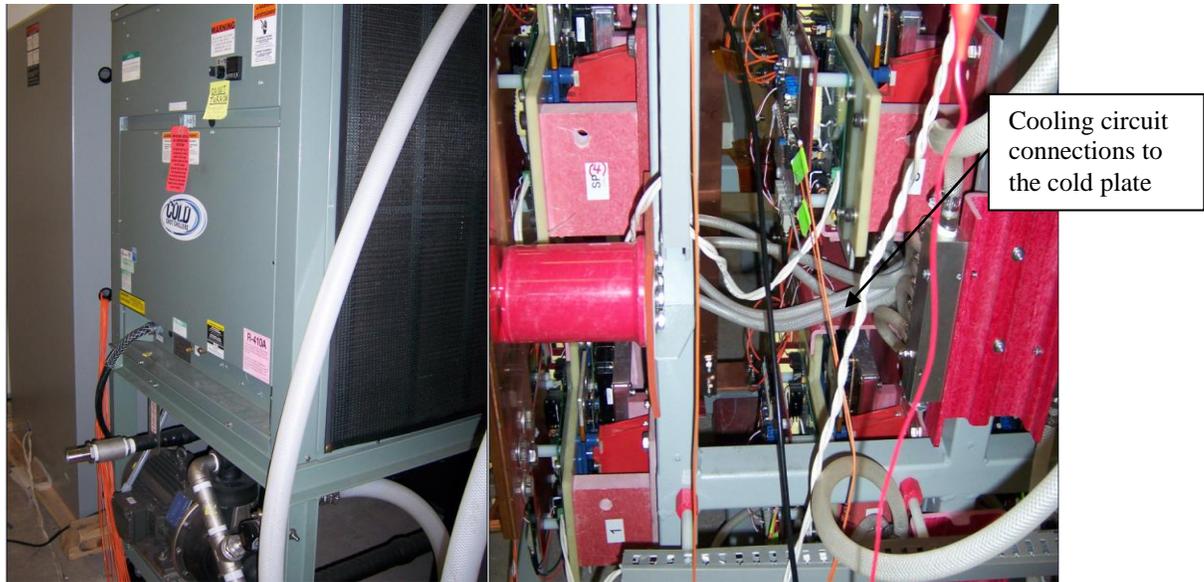


Figure 3-9: Left – Chiller used for the continuous current test: Right – Building Blocks mounted on the frame with the cooling circuit connections made

Design changes over the course of the project

As mentioned in the beginning of this chapter, after an attempt at testing the system in KEMA during September 2010, it was observed that the varistors were damaged in attempt to turn-off fault current. The varistors selected were adequate for the clamping of the voltage spike associated with the hard turn off. However, they were undersized with respect to the long term AC withstand voltage that was asserted across the SSCL while the let-thru current was following. The lack of cross tie bus connections between the CLR's and the building block added to the stress on the varistors. The recommendations for modifications to the SSCL included utilizing higher voltage varistors, with additional series building blocks if required. Cross tie bus bar connections should be installed and the connections to the CLR's should be corrected. More detailed explanation is available in the technical update submitted in December 2010[5]. It was decided that 12 building blocks will be used in all 6 in series and 2 in parallel as the final design for the 15kV unit.

After all the above changes were incorporated the stack was retested in January 2011. It was observed during this test that the building blocks turned off the current but were not able to sustain the turn-off and attempted to turn back on. Mechanical stresses and damage on the CLR's were observed. A detailed failure analysis was done at that point and a detailed report was submitted with further recommended changes to be made to the system. A summary of the changes made include:

- Additional snubber capacitance to the building block to provide more margin for turn-off
- Changes in the bus connections – earlier the incoming and the outgoing connections to the building block were made across the bus bar (figure 3-10- left) which more intuitively aided current sharing but further testing showed that this was not true. The mutual flux linkage between the incoming and outgoing bus resulted in unequal distribution of current between the three parallel modules. Hence the connections to the incoming and outgoing bus of the building block are made on the same side (figure 3-10-right).

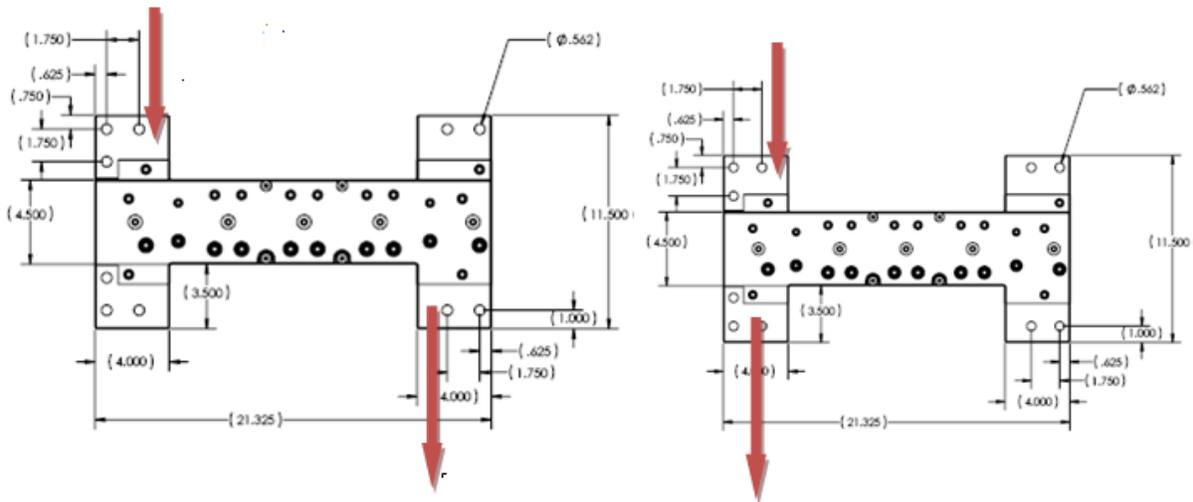


Figure 3-10: Bus bar connection changes – left: previous arrangement – right: new arrangement

- Software modifications to improve input filtering and prevent re-firing after turn-off
- Hardware modifications to prevent back-feeding of the power supplies and to increase filtering capacitors on the power supply board and additional protection logic on the gate distribution board to prevent unintentional turn-on signal being sent to the modules.
- Frame modifications to separate the CLR's to reduce the forces between them. Figure 3-11 shows the new CLR arrangement.
- Modules and building blocks were matched based on voltage rise, storage time and fall time.

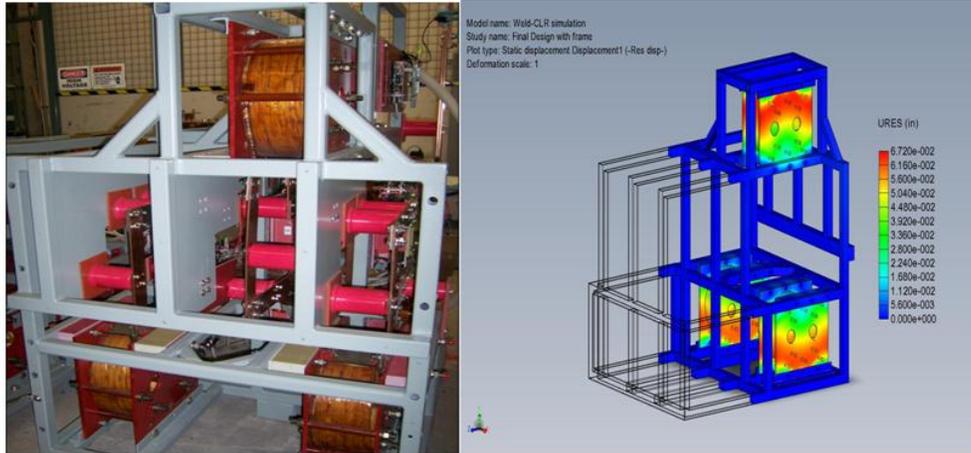


Figure 3-11: Frame modification and CLR placement

After all the above changes were incorporated the system was taken to the high voltage lab facility (KEMA) for testing in May 2011. This test was successfully completed and detailed test results are discussed in the chapters to follow.

4 TEST REQUIREMENTS AND PROCEDURES

The SSCL power stack was subjected to a series of factory tests. The factory inspections and tests were conducted in accordance with the manufacturer's standard test procedures and other tests as required to allow verification of full compliance to these specifications.

This chapter enumerated the test requirements that were set for the building blocks and the stack. The test procedures followed for the independent lab testing of the 15kV stack is listed below. All the component level testing and factory testing has been discussed in the Technical Update, in December 2010 [5].

The power stack underwent all the factory level tests as described in [5] before it was shipped to KEMA for the final independent testing. The factory test proved the functionality of the unit and the pass fail criteria is the same as the final testing in KEMA. The power stack passed the continuous current factory test and the current limiting tests on May 5th, 2011. A customer demonstration was held at the factory to demonstrate the working of the unit before shipping it to KEMA. Independent lab tests at KEMA were conducted on May 16th through May 24th.

Factory Test

Before taking the completely built test stack to KEMA for final verification test, the stack underwent the factory continuous current and factory interruption test. It was proven that the blocks carry continuous current of 1200Arms (@24V) and reach temperature stability in 1.5 hours and that the stack is capable of limiting current. It was tested that the system is capable of responding to a fault event and interrupt current with current measurement made on each string (one of the parallel blocks) to ensure that all of the blocks turned off and that the corresponding reactor took over during a fault event. The following (figure 4-1) is a picture of the stack undergoing the factory test.



Figure 4-1: Unit under test at factory (Silicon Power, Malvern, PA)

KEMA Current Limiting Tests for the Power Stack

The objective of the Current Limiting Test is to demonstrate that the stack responds to fault events at different levels (50%, 75% and 100% of rated fault current) and limits it desirable levels (as mentioned in the table below) within 100 μ s of initiation of fault.

To perform this test, 2 parallel and 6 series building blocks were used. The VLC and FPGA boards were programmed and the high speed current sensor was operational and capable of interrupting within 50 μ s of the start of the test. The control cabinet was connected and fully operational before beginning the test. The cooling system was not connected for this test.

The test facility provided a fault current of up to 23kA symmetrical RMS, from a 15kV RMS (8.6kV L-N) generator (15kV RMS +0V/-100V). The generator provided 1200A RMS for 7 cycles before supplying the 23kA RMS fault current. This was accomplished through a load bank controlled by a separate breaker.

All measurements were made as shown below which would provide a good verification of the current limiting functionality of the SSCL. The test was conducted at different fault current levels by varying the generator voltage between 50% – 100% of the rated value.

Measurement Details

The following measurements were made:

- The current flowing in the main bus of the SSCL (1 channel)
- The voltage across the SSCL (1 channel)

- The voltage across each inductor (6 channels)

Test Details

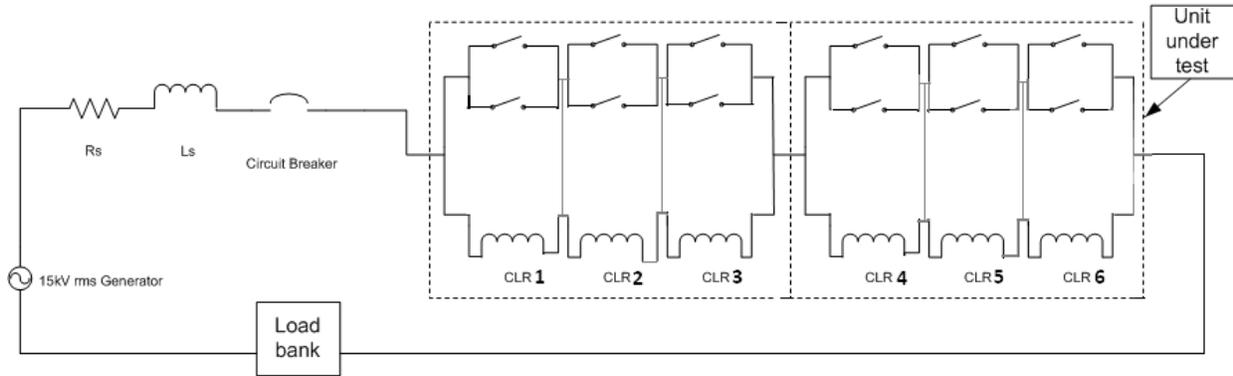


Figure 4-2 SBB Test Circuit for Power Stack

Figure 4-2 shows the test circuit used to test the SSCL stack. The power stack had 2 blocks in parallel and 6 in series. The source impedance was such that the available fault current through the power stack and load bank is limited to 23kA symmetrical RMS (55 kA peak asym.). Further, a load bank was set such that the system draws 1200A RMS initially and the fault current generator was set to produce the desired fault current after 7 cycles by shorting the load bank.

The following conditions were evaluated before conducting the test:

- 1) The circuit breaker was set such that it allows the let-thru current for max of 30 cycles.
- 2) All the required instrumentations were attached.
- 3) The control power was applied to the SSCL and it was also verified that the unit is operational.

Once all the above conditions were checked the main bus was energized and measurements were taken. The voltage was gradually stepped up to obtained multiple levels of fault current. This test was repeated 4 times with different fault current levels (11.6kA sym (2), 17.4kAsym and 23.2kA). Test observations and waveforms are presented in the sections to follow.

Pass/Fail Criteria for Current Limiting Test

Based on the test plan SSCL shall be considered to have passed the test if the system limits a 23kA sym. RMS (55kA peak asym.) fault current to 9kA sym RMS (9kA sym. RMS +0%/-10%; 21.6kA peak asym. +0%/-10%) for 30 cycles.

KEMA Continuous Current Test for the Power Stack

The objective of this test was to functionally test the system to be able to carry a continuous current of 1200A RMS or greater and to test until thermal stability is reached. The test was performed with 2 parallel and 3 series building blocks. The sensors were attached and the cooling system was in place.

The test facility provided 1200A RMS, 30V, at 60Hz for the duration of the test. The continuous current test was continued for a period of time such that the temperature rise of any monitored point in the assembly had not changed by more than 1°C as indicated by three successive readings at 30 minute intervals. The current sharing and voltage balancing of the power stack were measured. Temperature measurements were made on each building block.

Measurement Details

The following measurements were made:

- The current flowing in the main bus of the SSCL (1 channel)
- The current through each parallel string of building blocks (2 channels)
- The voltage across the SSCL (1 channel)
- The voltage across each building block (3 channels)
- The temperature of each building block (6 channels)

Test Details

The detail of the test performed at KEMA is presented below. The source impedance and load bank was set such that the current flowing through the SSCL unit under test is 3000A RMS. The total forward drop of the SGTOs within the SSCL is approximately 9V. Figure 4-3 shows the continuous current test circuit.

For the continuous current test, control power was turned on before the main bus was energized. The current sharing and voltage balancing of the power stack were measured. Instrumentation was attached to record the line current and system voltage. The temperature of each building block was measured using thermocouples placed on the cold plate. The cooling system was operational throughout the test. The main bus was energized and reading temperature monitored continuously for 1.5 hrs.

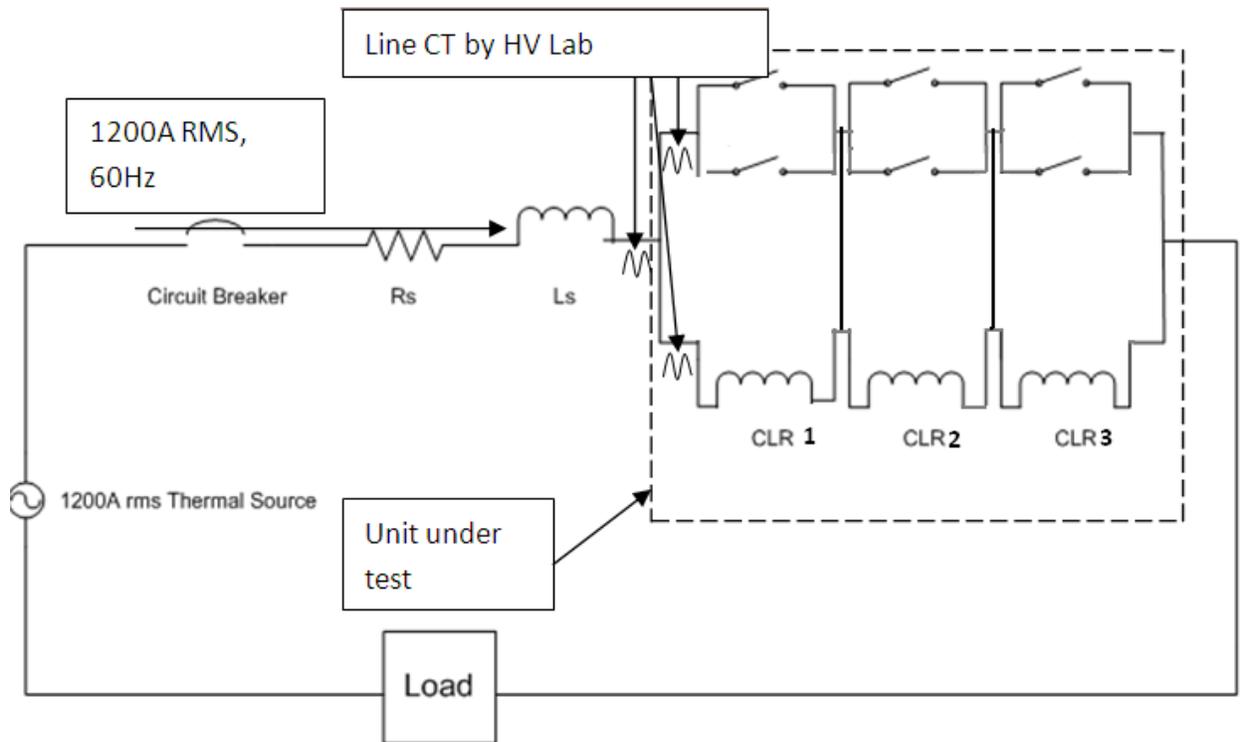


Figure 4-3: Test Circuit for Continuous Current Carrying Test for the Power Stack

Once enough readings were taken to ensure stability of the thermal system, the main bus was de-energized before the control power for the SSCL is removed. The results and waveforms obtained for this test are listed in the section to follow.

Silicon Power monitored the main voltage, main current and the current sharing between blocks. Current through each building block in the stack was monitored using a PEM Rogowski Current Sensor. The scales for these measurements are listed in the waveform presented in the section to follow.

Pass/Fail Criteria for Continuous Current Test

The SSCL shall be considered to have passed the test if the system carries 1200A RMS at low voltage for 1 hour with stable temperature measurements (i.e. the temperature rise of any monitored point in the assembly has not changed by more than 1°C as indicated by three successive readings at 30 minute intervals) with all measured temperatures remaining below 100°C.

5 TEST RESULTS

The SSCL power stacks were tested for both current limiting and the continuous current carrying capability. This chapter reports the results obtained from the current limiting and continuous current test held at KEMA, an independent high voltage lab facility.



Figure 5-1: Unit under test at KEMA high voltage lab facility (KEMA, Inc. Chalfont, PA)

Current Limiting Test Results

The stack underwent the current limiting test on May 16th and 17th, 2011. This test was successfully completed with the stack limiting 23.2kA sym RMS fault current down to 9.8kA RMS.

The results can be tabulated as follows:

Table 5-1: Test results – Current Limiting test for the 15kV power stack

Test	Available Fault Current level / kA sym RMS	Let Through current sym (KA)	Main bus current at interruption / A	dI/dt prior to turn off / A / μ s	Turn off time / μ s	Voltage across the building blocks /k V		Comments
						1	2	
Current Limiting Test	11.6	4.9	527.3	2.61	50us	1	0.599	
						2	0.655	
						3	0.768	
						4	0.625	
						5	0.595	
						6	0.621	
Current Limiting Test	17.4	7.3	117.2	3.89	50us	1	0.898	
						2	0.972	
						3	1.080	
						4	0.940	
						5	0.873	
						6	0.914	
Current Limiting Test	23.2	9.8	589.9	5.22	50us	1	1.20	
						2	1.30	
						3	1.37	
						4	1.25	
						5	1.17	
						6	1.20	

Test Waveforms

Figure 5-2, 5-3, 5-4 and 5-5 show the screen shots taken during the test in KEMA. In total 4 trials were conducted after calibration which include 2 trails for 11.6kA available fault current followed by 17.4kA and 23.2kA available fault current. The voltage across the reactor coils 1(Ch3), 2 (Ch4), 3(Ch 5), 4(Ch 6), 5(Ch7) and 6(Ch8) indicate that the current was interrupted through the SGTO devices and limited by the reactors.

Figure 5-6, 5-6, 5-7 show a zoomed in view of the limiting action.

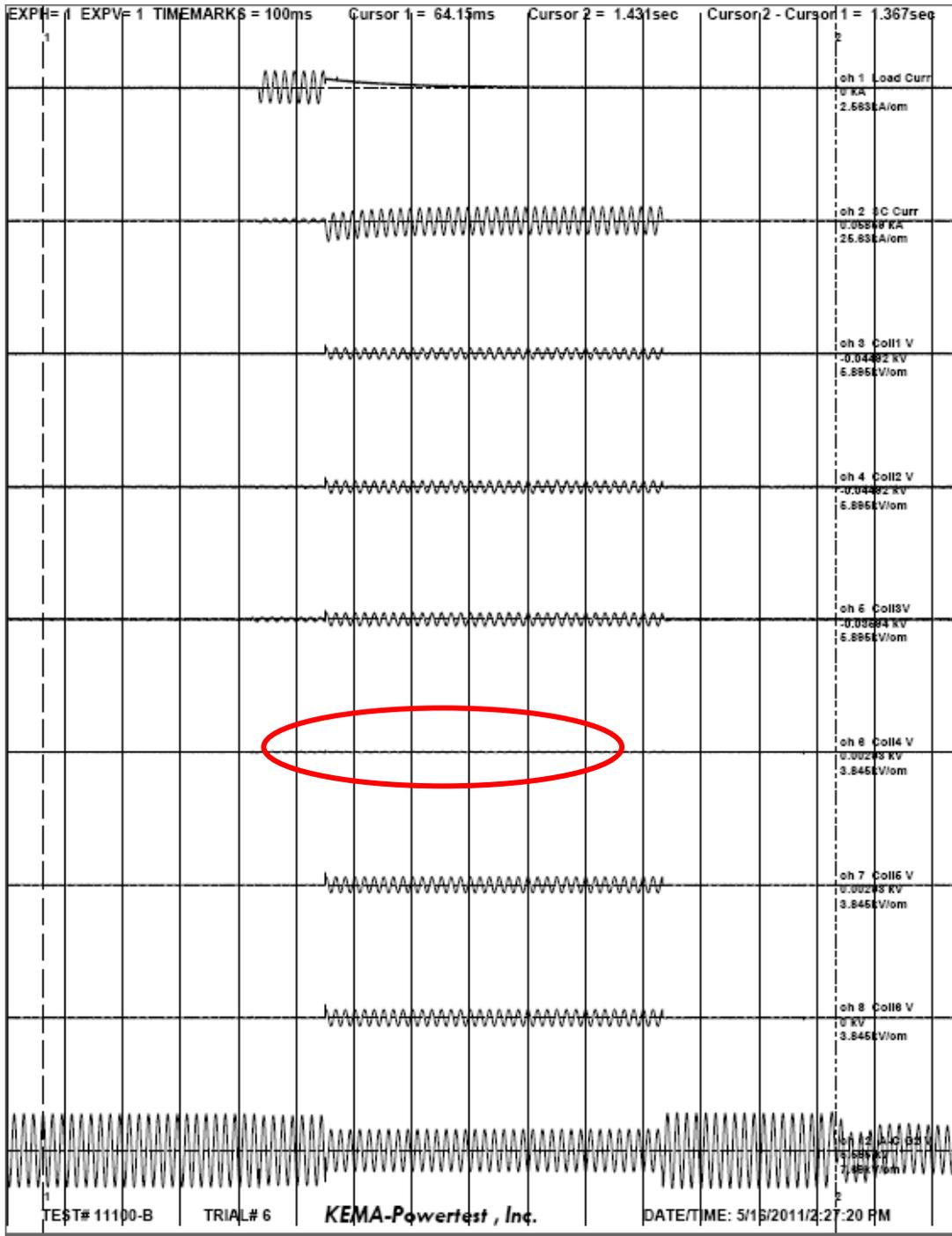


Figure 5-2: Screen shot of the 11.6kA sym RMS available fault current trail (first attempt)- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR’s respectively, Ch9 is the generator voltage

In the above trial it can be observed that Ch6 has no voltage recorded after the fault event. This was later diagnosed to be a bad fiber optic connection to one particular building block that was parallel to the coil # 4. Once the fiber optic cable was replaced a repeat trial was run and the following result was obtained.

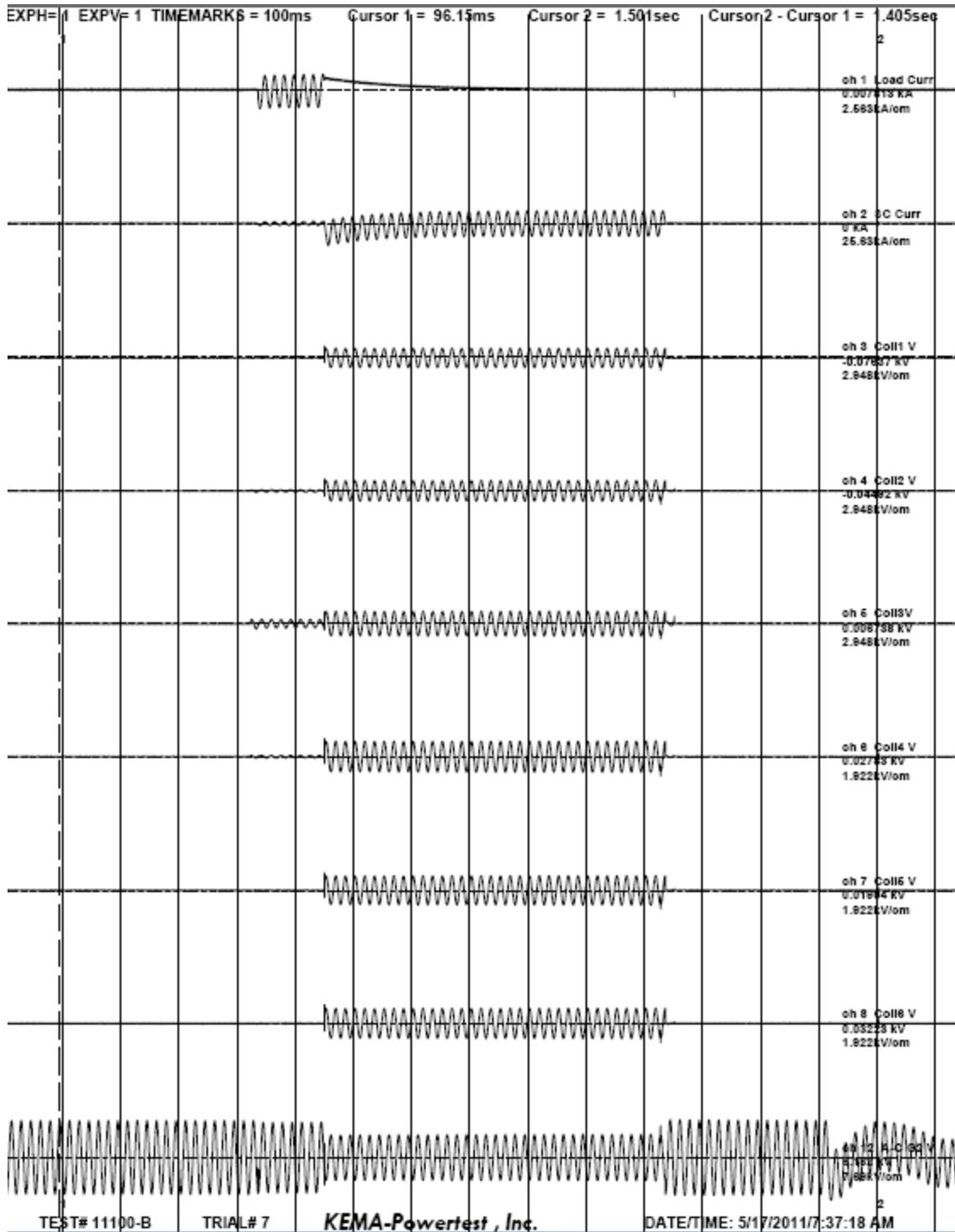


Figure 5-3: Screen shot of the 11.6kA sym RMS available fault current trial (second attempt)- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage

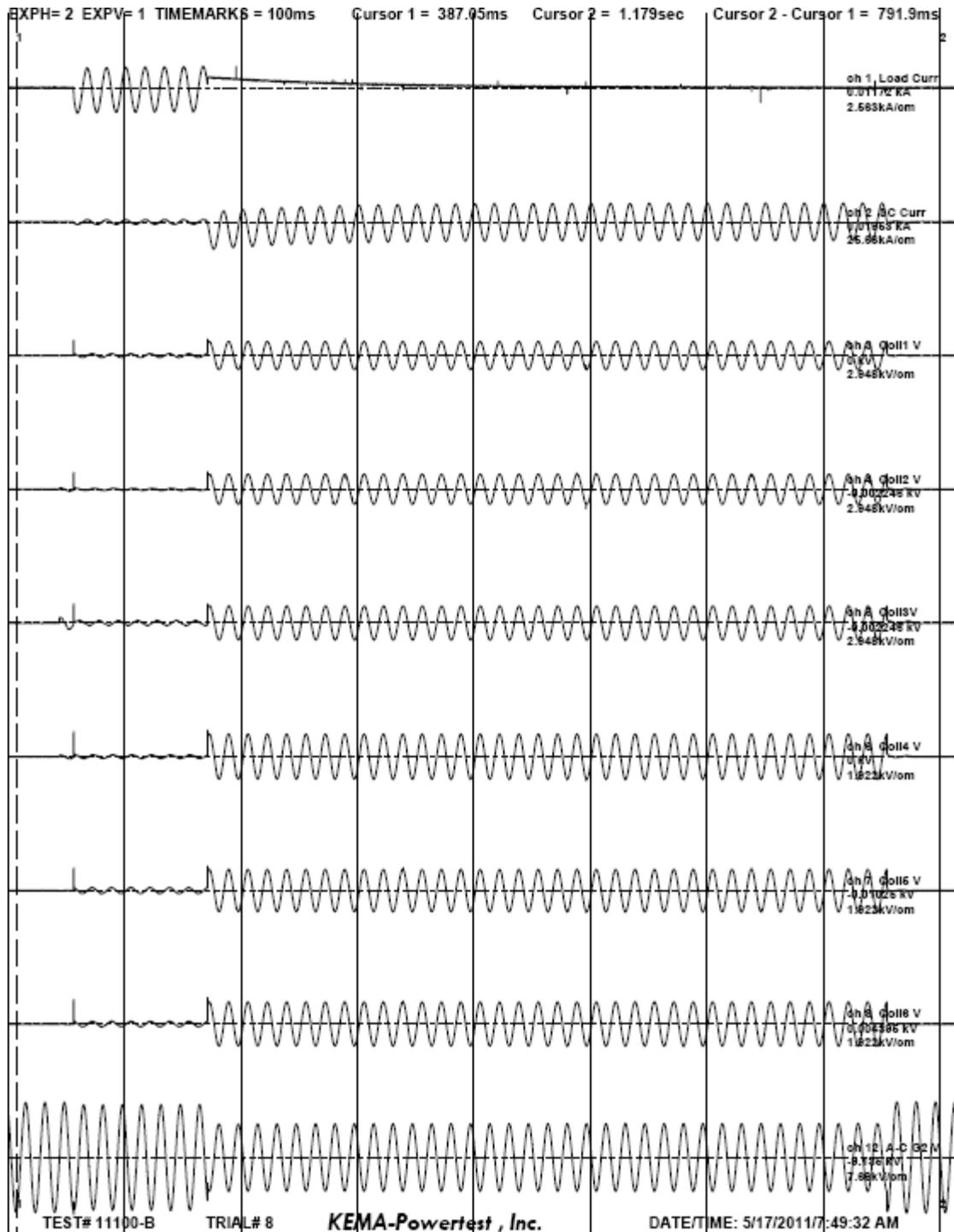


Figure 5-4: Screen shot of the 17.4kA sym RMS available fault current trial- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage

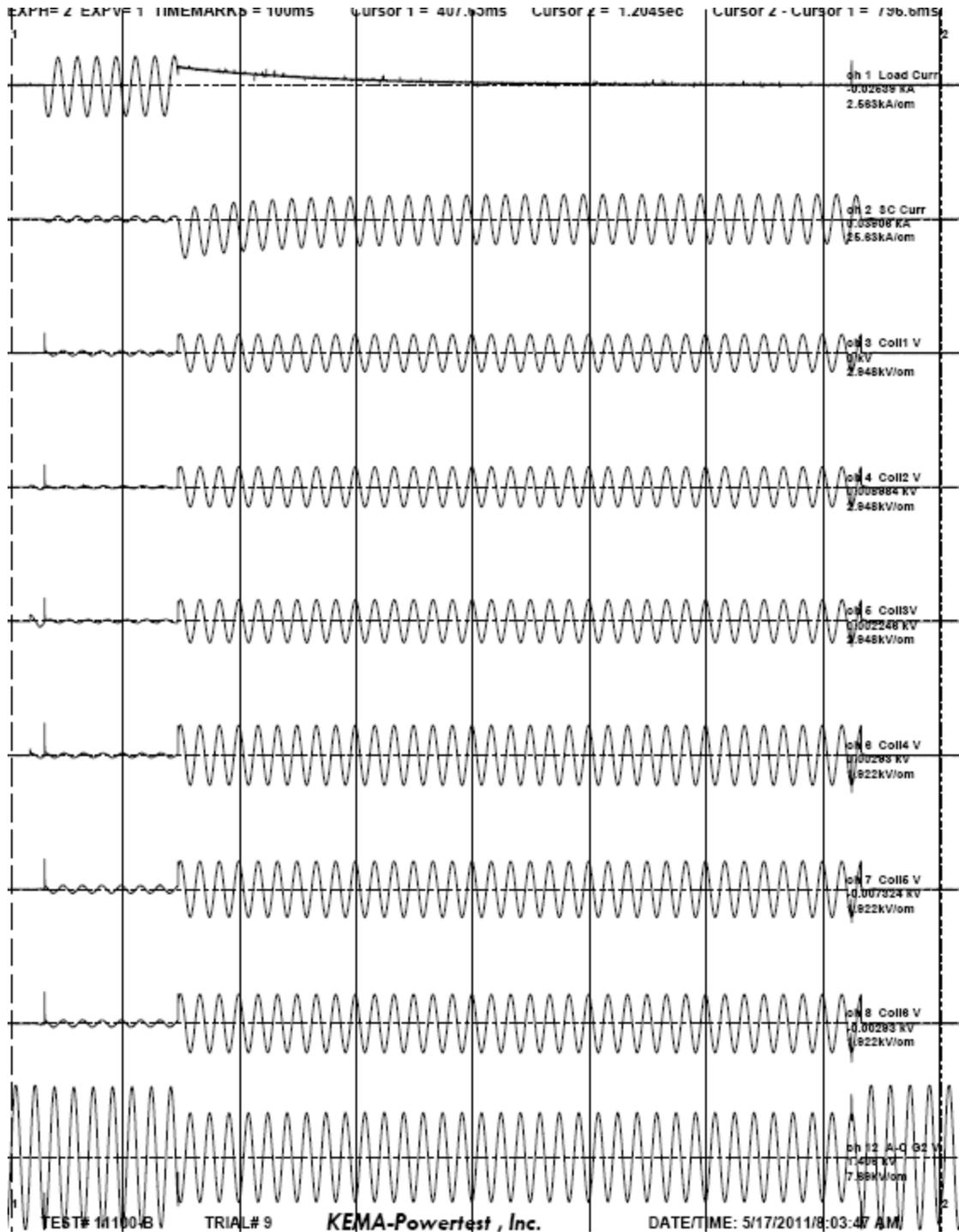


Figure 5-5: Screen shot of the 23.2kA sym RMS available fault current trial- Ch1 is the load current, Ch2 is the SC Current, Ch 3 – Ch 8 are the voltage across the 6 CLR's respectively, Ch9 is the generator voltage

After studying the raw data obtained from KEMA and plotting them the table 3 has been filled and the waveforms below have been obtained.

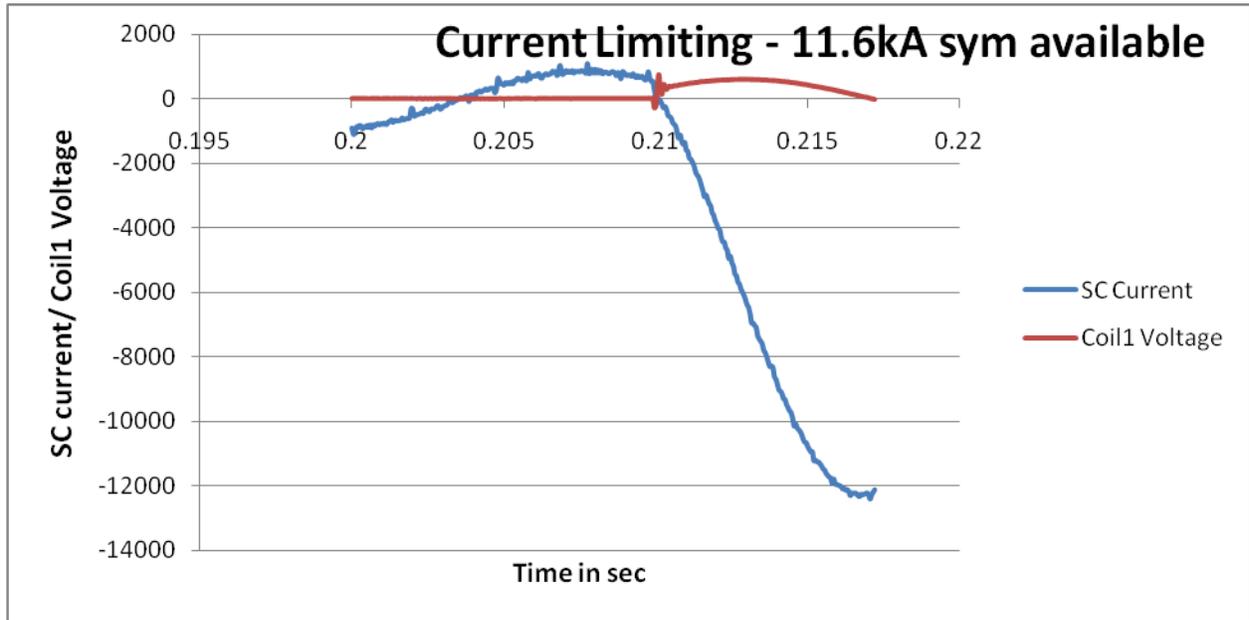


Figure 5-6: Zoomed in view of turn-off- 11.6kA sym RMS available fault current

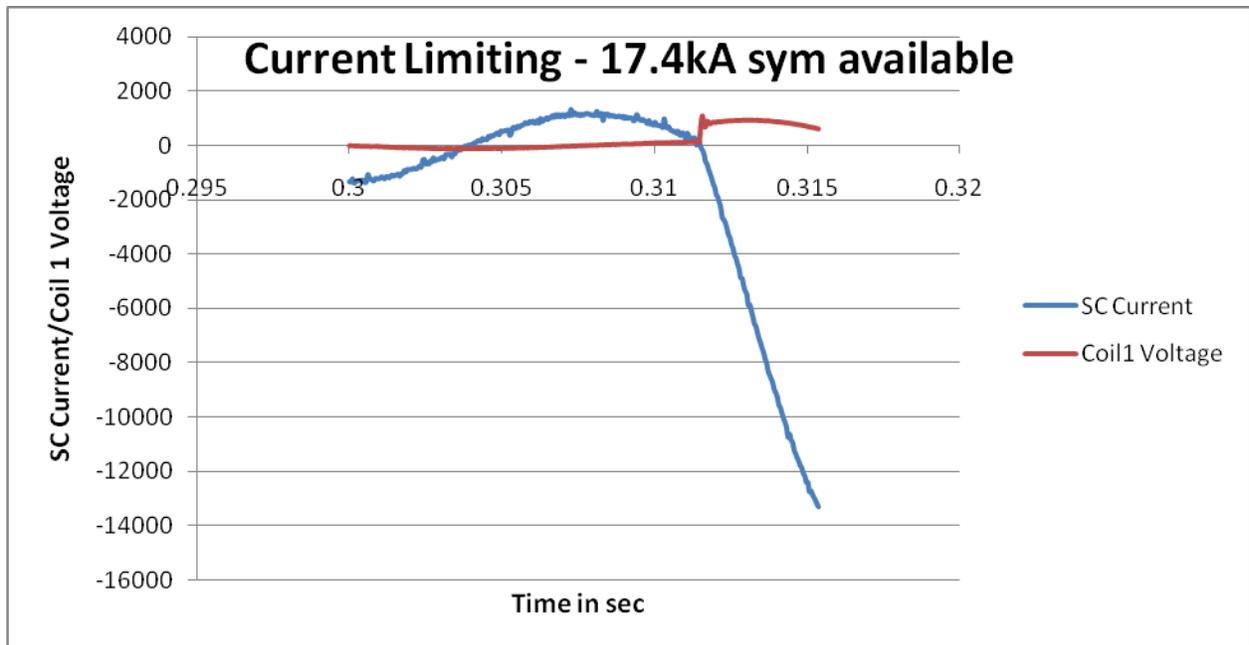


Figure 5-7: Zoomed in view of turn-off- 17.4kA sym RMS available fault current

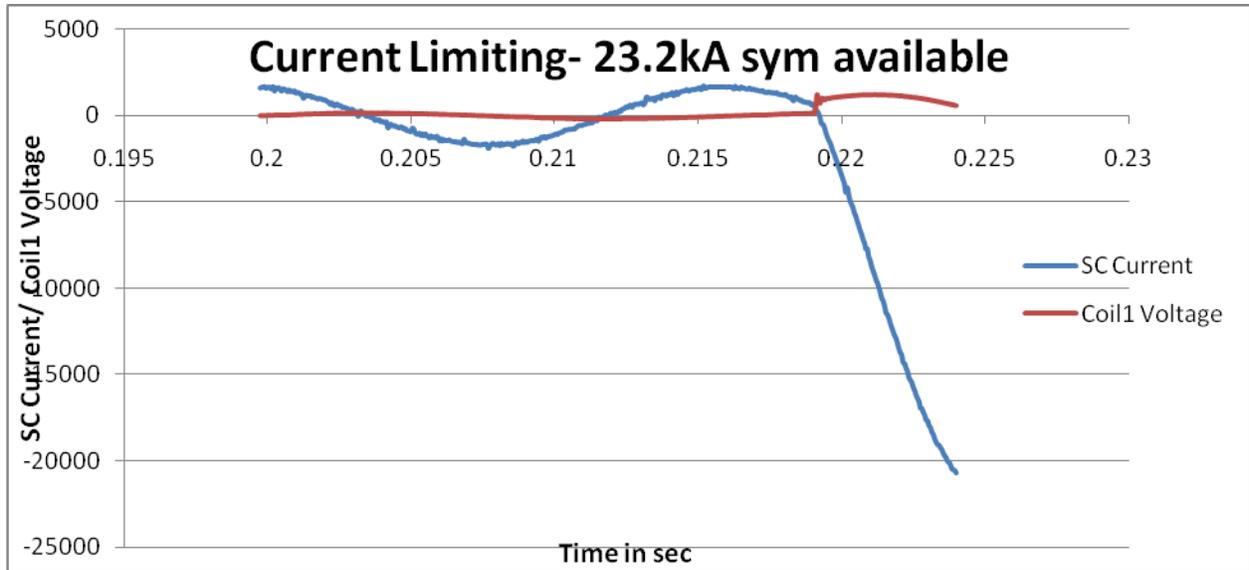


Figure 5-8: Zoomed in view of turn-off- 23.2kA sym RMS available fault current

Conclusion

From the data obtained from KEMA it has been proved that devices turned off well within 50us and the current was transferred to the current limiting reactor hence limiting the required 23.2kA available sym RMS fault current to 9.8KA sym RMS. Current limiting was achieved in all three steps - 50%, 75% and 100% of available fault current. All three trials were successful (as can be seen from KEMA snap shots in figure 5-3, 5-4 and 5-5).

Continuous Current Test Results

The stack underwent the continuous current test on May 20th and 23rd, 2011. This test was successfully completed with stability requirement satisfied. The results of this test are reported below:

Table 5-2: Test results - Continuous Current Test for the 15kV stack

Test	System RMS Current /k A	System voltage / V	Building block current		Voltage across building block		Temperature of building block after stabilization		Comments
			String	Value/ A RMS	Block	Value / V	Block	Value / °C	
Continuous current test run 1	3.01	10.8	String 1	1505	1	2.66	1	24.7	1hr reading
					2	2.66	2	23.1	

					3	2.66	3	23.2	
			String 2	1505	4	2.66	4	22.9	
					5	2.66	5	22.9	
					6	2.66	6	23.9	
Continuous current test run 2	3.01	10.6	String 1	1505	1	2.64	1	24.3	1hr mark
					2	2.64	2	21.6	
					3	2.65	3	22.2	
			String 2	1505	4	2.64	4	23.2	
					5	2.64	5	22.8	
					6	2.65	6	22.1	
Continuous current test run 3	3.02	10.7	String 1	1510	1	2.66	1	24.9	1hr mark
					2	2.66	2	22.6	
					3	2.67	3	22.5	
			String 2	1510	4	2.66	4	24.6	
					5	2.66	5	24.5	
					6	2.67	6	23.0	

Test Waveforms

The waveforms below show equal current sharing between the parallel block (SPCO data):

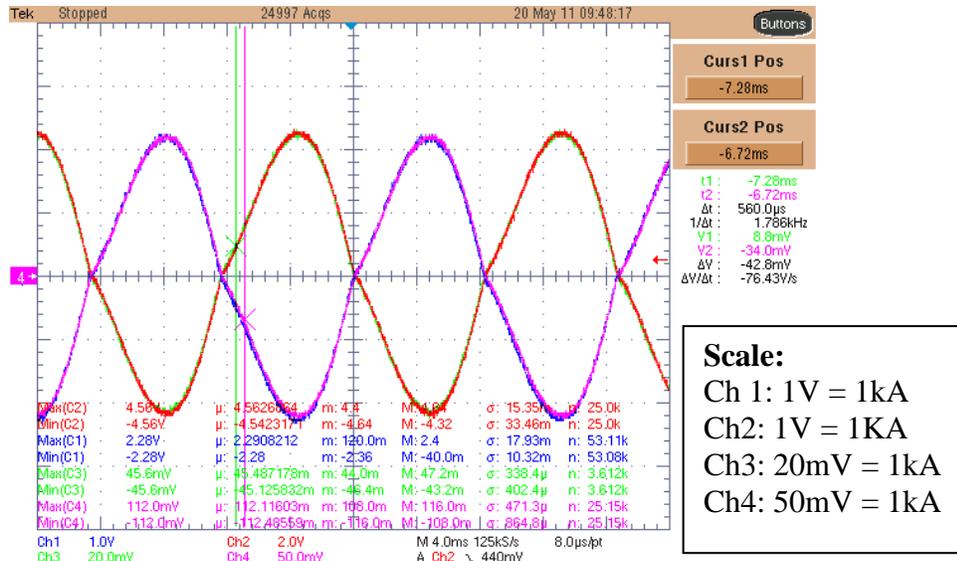


Figure 5-9: Current Sharing Run 1 – Block – 1(Ch 1)*, 2(Ch 3), 3(Ch 4)* and the main current (Ch 2)

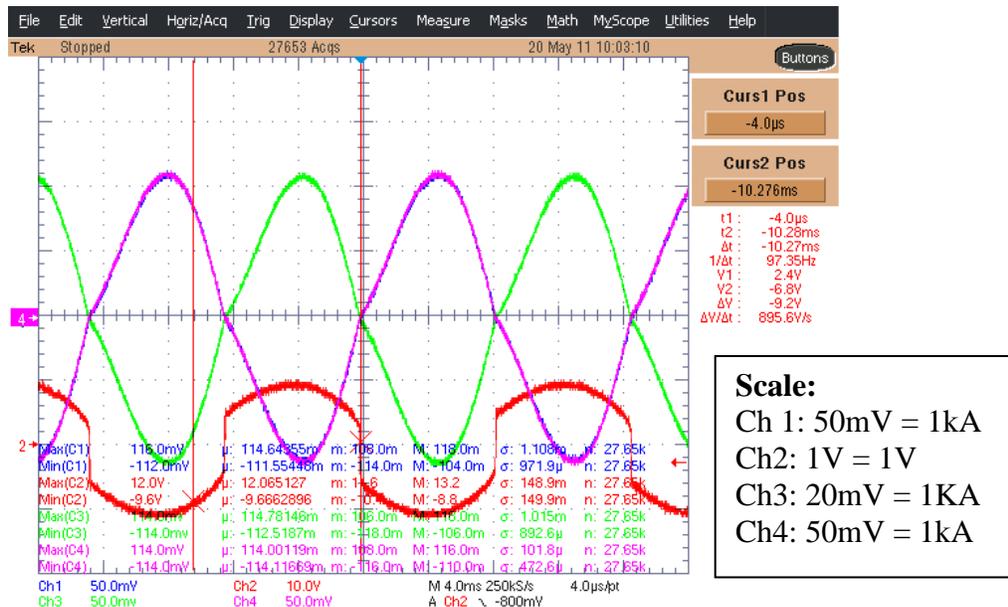


Figure 5-10: Current Sharing Run 1 – Block –4(Ch 1)*, 5(Ch 3), 6(Ch 4)* and voltage across SSCL (Ch 2)

*Note – The waveform inversion in these channels is a result of reversal in direction of the Rogowski current sensor

The waveforms taken for Continuous Current Test Run 2 are below:

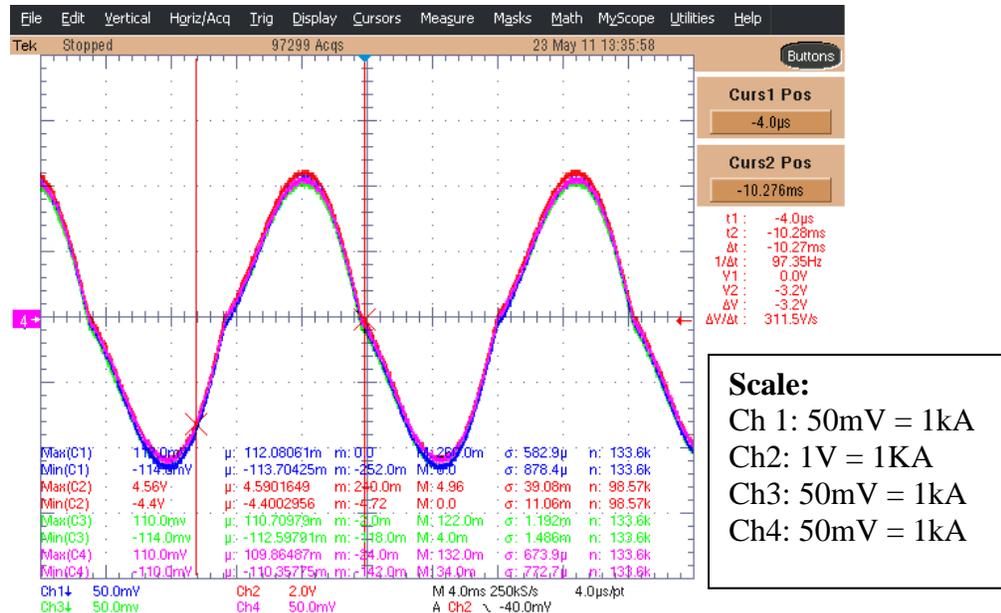


Figure 5-11: Current Sharing Run 2 - Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 2)

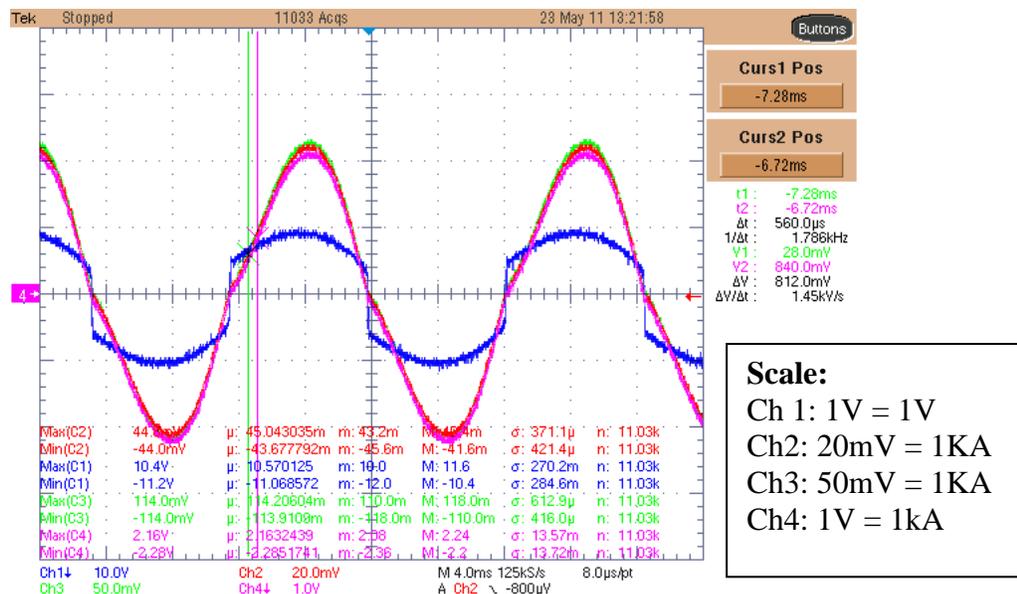


Figure 5-12: Current Sharing Run 2 - Block –4(Ch 2), 5(Ch 3), 6(Ch 4) and voltage across SSCL (Ch1)

The waveforms taken for Continuous Current Test Run 3 are below:

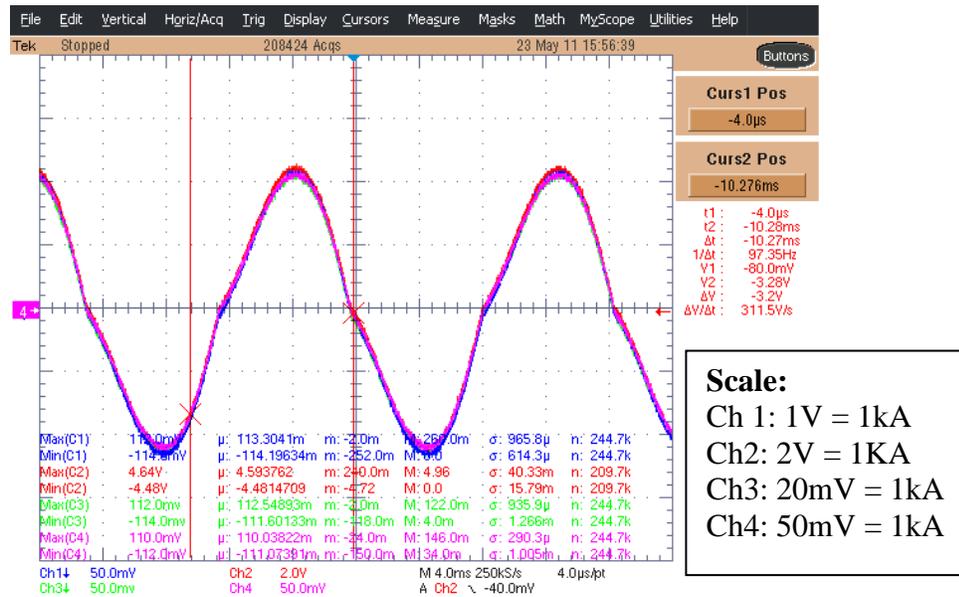


Figure 5-13: Current Sharing Run 3- Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 8)

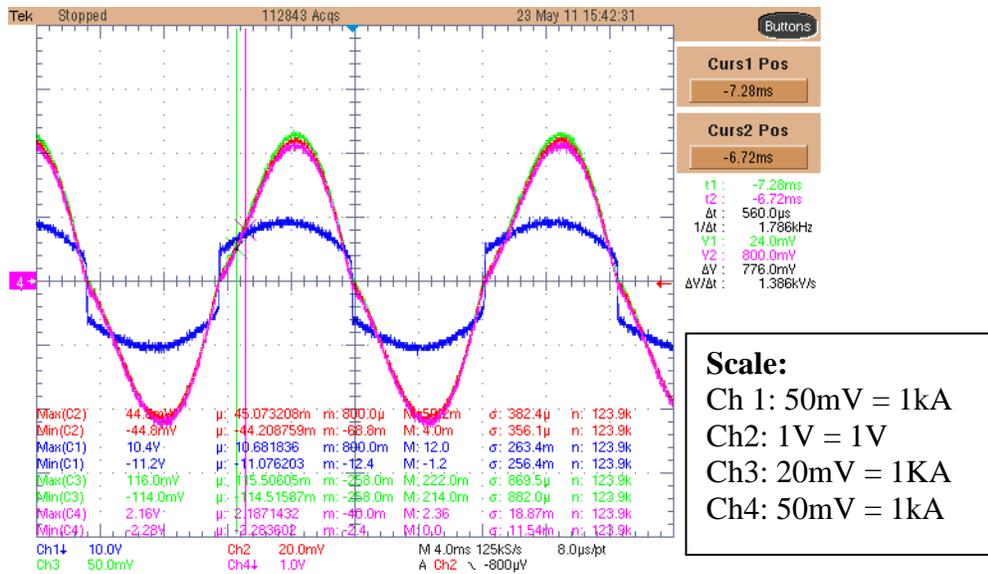


Figure 5-14: Current Sharing Run 3- Block – 1(Ch 1), 2(Ch 3), 3(Ch 4) and the main current (Ch 8)

Temperature Stability Data

The tables below show the temperature measurement data every half hour into the test on each Building Block (BB) for 3 runs.

Table 5-3: Temperature measured on each building block – run 1

Time	Temperature	Temperature	Temperature	Temperature	Temperature	Temperature
5/20/2011	BB1 (°C)	BB2 (°C)	BB3 (°C)	BB4 (°C)	BB5 (°C)	BB6 (°C)
10:06 AM	24.7	23.1	23.2	22.9	22.9	23.1
10:36 AM	25.1	23.2	23.3	23.1	22.5	23.3
11:06 AM	25.4	23.5	23.7	23.5	22.7	23.7

Table 5-4: Temperature measured on each building block – run 2

Time	Temperature	Temperature	Temperature	Temperature	Temperature	Temperature
5/23/2011	BB1 (°C)	BB2 (°C)	BB3 (°C)	BB4 (°C)	BB5 (°C)	BB6 (°C)
1:58 PM	24.4	21.7	22.4	23.5	23.3	22.2
2:28 PM	24.5	21.7	23.2	23.7	23.6	22.3
2:58 PM	25.4	22	21.9	23.9	23.5	22.5

Table 5-5: Temperature measured on each building block – run 3

Time	Temperature	Temperature	Temperature	Temperature	Temperature	Temperature
5/23/2011	BB1 (°C)	BB2 (°C)	BB3 (°C)	BB4 (°C)	BB5 (°C)	BB6 (°C)
3:36 PM	24.9	22.8	22.5	24.3	24.3	23.3
4:06 PM	24.9	22.6	22.5	24.6	24.5	23.0
4:26 PM	25.3	22.8	22.1	24.6	24.7	23.2

Conclusion

From the above test tabulation and waveforms, it can be concluded that the thermal run or continuous current test was successfully performed with temperature readings taken every minute for the complete run of the test. The power stack carried 3000A RMS at low voltage for 1.5 hour with stable temperature measurements (i.e. the temperature rise of any monitored point in the assembly had not changed by more than 1°C as indicated by three successive readings at 30 minute intervals) with all measured temperatures remaining below 100°C.

Summary of Test results and Compliance Table

Test	Condition desired	Condition provided at test lab	Result / Comments
6 SBB Current limiting test	Available fault current of 23kA sym. RMS, limited to 9kA RMS +0%/-10%for 30 cycles. Voltage not to exceed 15kV RMS. Measure main bus current and current through each parallel string of SBB for current sharing. Measure the voltage across the SSCL and each SBB. Verify limiting current value and measure voltage response	15kV L-L RMS +0/-100V, 23kA sym. RMS available fault current from generator (may use current limiting reactors to drop down to 15kV RMS, 23kA sym. RMS). For 6 CLR's of 238 μ H, this will let us limit to: I_let_thru=9kA RMS	Passed – based on Pass/Fail Criteria
6 SBB Continuous current test	1200A RMS at low voltage, any power factor, for >1 hour (until temperature stabilizes).Measure module temperatures at baseplate of each SBB. Temperature not to exceed 100°C. Measure main bus current, voltage across SSCL. Measure current through each parallel string of SBB, and voltage across each building block for current sharing / voltage balancing	3000A RMS, <30V RMS	Passed- based on Pass/Fail Criteria

6 SUMMARY

The increase in available fault current levels due to increased distributed generation capacity and increased load has stressed many transmission and distribution substations to their limits. In some cases, fault current levels are exceeding the interrupting capability of existing substation circuit breakers. This increase in fault current levels either requires the replacement of large numbers of substation breakers or the development of some means to limit fault current.

The Solid State Current Limiter, or SSCL, is a power-electronics based system designed to limit the fault current in Transmission and Distribution applications. The SSCL monitors the current in the main bus of the system and dynamically inserts additional impedance into the line in the event of a fault. The SSCL responds rapidly to fault events and is capable of responding to successive fault events. As a power-electronics based system, the SSCL is a compact, efficient unit.

Phase 1 of the EPRI SSCL Development Project, design, manufacture and test of a 15kV, 1200A RMS rated single phase power stack been completed. Initial factory tests and subsequent independent high voltage laboratory tests were successful.

The present phase has helped prove the functionality of the unit. The next phase of the project will see the manufacture and factory testing of a three phase, 15kV class SSCL to further demonstrate the performance of the current limiter and to indicate the dielectric withstand performance. A subsequent phase of the project will then subject the SSCL to a field test at a suitable host site.

The Solid State Current Limiter remains a promising addition to the tools available to Utility companies to combat the anticipated growth in Fault Current. The SSCL has the ability to become a key component of the Smart Grid of tomorrow in both the Transmission and Distribution sectors. The completion of the functional tests for this phase of the project will further illustrate the capabilities of the SSCL and will augur well for the next phase of the project.

A

REFERENCES

[1] *69kV Solid State Current Limiter Scoping Study*: EPRI, Palo Alto, CA: 2006. 1012370.

[2] *Solid-State Fault Current Limiter/Circuit Breaker Development: Design and Development Document*. EPRI, Palo Alto, CA: 2007. 102105.

[3] *Solid-State Fault Current Limiter/Circuit Breaker Development: Design and Testing Update of a 69kV SSCL*. EPRI, Palo Alto, CA: 2008. 1015949.

[4] *Development of a 15kV Class Solid-State Current Limiter*. EPRI, Palo Alto, CA: 2009. 1017757.

[5] *Solid-State Fault Current Limiter Development: Design and Testing Update of a 15kV Power Stack*. EPRI, Palo Alto, CA: 2010. 1020028.

