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Presented at the 23rd Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes
Breckenridge, Colorado
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Abstract

The extent of potential-induced degradation of crystalline silicon modules in an environmental chamber is estimated using *in-situ* dark *I-V* measurements and applying superposition analysis. The dark *I-V* curves are shown to correctly give the module power performance at 200 W/m^2, 600 W/m^2, and 1,000 W/m^2 irradiance conditions, as verified with a solar simulator. The onset of degradation measured in low light in relation to that under one sun irradiance can be clearly seen in the module design examined; the time to 5% relative degradation measured in low light (200 W/m^2) was 28% less than that in full sun (1,000 W/m^2 irradiance). The power of modules undergoing potential-induced degradation can therefore be characterized in the chamber, facilitating statistical analyses and lifetime forecasting.

Introduction

The high system voltage of modules in series strings is a stress factor that leads to power degradation. Conventional crystalline (n^+/p) silicon modules are well understood to be sensitive in negative potential strings. The term potential-induced degradation (PID) has been applied to this observed degradation, whereby junction failure and fill factor degradation are dominant [1]. There are many reports of PID around Europe and Asia where neither terminal of the array is connected to ground and segments of the string exist at negative potential [2]. As for the United States, UL 1747 stipulated in the past that photovoltaic (PV) inverters have one terminal of the module string connected to ground, and the strings have been, fortuitously, at positive potential (negative terminal grounded) by convention. However, code was modified in 2011 to allow systems with both terminals ungrounded. More consideration must therefore be given to PID in the United States.

While the mechanisms for system voltage degradation are still being clarified, it is understood that ionic transport occurs through the glass and encapsulant, and those ions are involved in the degradation itself [3]. The most important ionic species candidate is the sodium ion present because of the 13–14 weight percent NaO_2 that is a constituent of the soda-lime glass module superstrate. NaO_2 is used to lower the glass melting point and thus the cost. Such positive ions have been discussed as creating electric fields in the antireflective coating or passivation layer [4]. Sodium has also been found in high concentrations in stacking faults penetrating the junction [5]. It has also been speculated that ions accelerated over an insulating dielectric or antireflective coating under an electric field may embed and damage the junction [6] in view that corona discharge over cells has been found to induce PID-like junction failure [7]. Considering that both reversible and irreversible components of junction failure are associated with system voltage stress [8], it is conceivable that multiple mechanisms are active.

We seek to forecast the lifetime of modules in the field using accelerated testing. Collection of sufficient data from modules undergoing indoor accelerated lifetime testing to enable statistical analyses and lifetime predictions has been difficult, and data are lacking. Measurement of power degradation generally involves intermittently removing the module from the environmental chamber and measuring power on a solar simulator, which is a time-consuming process when numerous samples are involved. Methods are therefore sought to characterize the state of degradation of the module *in-situ* during stress testing.

Efforts have been made to correlate module shunt resistance with the extent of PID. Shunt resistance was first used as an indicator; however, PID does not primarily manifest as a simple shunt that can be extracted from the *I-V* curve at V ≈ 0 such as can be simulated with a low resistance placed in parallel with a solar cell. The degradation at the knee of the curve, the maximum power point (P_{max}), must be included in the analysis. While not yet establishing any certainty about the mechanistic origin, fitting of the degraded curves was achieved with increased (degraded) second (non-ideal) diode ideality factor and pre-exponential. Simple translation of the dark *I-V* curve to the fourth quadrant to recreate the *I-V* curve under illumination, usually by I_{sc} itself, was found to suitably estimate the fraction degradation of the power of the module undergoing PID stress tests in an environmental chamber [9].

It has been pointed out that the relative degradation of modules undergoing PID is more pronounced under low-light conditions than under full sun or the standard test conditions of 1,000 W/m^2 [10]. Low-light module performance is desired for favorable energy yield. It is therefore necessary to fully characterize the onset of the power loss under low light for modules undergoing PID. Anticipated benefits include more accurate determination of acceleration factors, better durability assessment of modules to PID for qualification testing, and improved forecasting of durability in the field.

Experiment

Environmental chamber testing was carried out on two replicas each of two module designs: (1) 60 15.6 cm x 15.6 cm conventional n^+p front-junction multicrystalline silicon (mc-Si) cell modules and (2) 72 12.5 cm x 12.5 cm conventional monocrystalline silicon (c-Si) cell modules. The environmental chamber conditions were 60°C and 85% relative humidity (RH). The module nameplate system voltage bias of –1,000 V was applied continuously to the cells in the module by connecting the shorted leads to a high-voltage (negative) power supply and grounding the module frame. Dark *I-V* curves were obtained with an *I-V* curve tracer capable of resolving five orders of magnitude in current up to 8 A. Curves for each module were obtained periodically *in-situ* of the chamber after stabilization of the module temperature to standard test conditions temperature of 25°C and between 40% and 50% RH and manual disconnection of the high voltage. Ramp rates (up and down) were 1°C/min, during which a –1,000 V bias was also applied. Dark *I-V* measurements were carried out within 1 h of the module reaching 25°C. To confirm the relationship between the maximum power (P_{max}) derived from the dark *I-V* curves and that determined with a solar simulator, modules were less frequently measured *ex-situ* of the chamber for *I-V* testing with a solar simulator. Modules were generally returned to the chamber for the continuation of stress testing within 4 h considering that some power recovery from PID has been indicated to be thermally activated [11].

The principle of superposition [12] was applied to the measured dark *I-V* curves—the simplifying assumption that the current obtained in the dark per the diode equation (1), with saturation current I_0, electronic charge q, Boltzmann constant k, diode ideality factor n, series resistance R_s and temperature T, can be translated from the first quadrant to the fourth quadrant by subtracting the photocurrent I_L for obtaining an *I-V* curve mimicking that which would be obtained for the device under illumination.

$$I = I_0 \left\{ \exp\left[\frac{q}{nkT} (V - IR_S) \right] - 1 \right\} - I_L \qquad (1)$$

P_{max} was then evaluated on the translated *I-V* curve as is conventionally done for curves obtained with solar simulators.

In our previous work [9], we showed how superposition could be used to determine power under standard test conditions (25°C, 1,000 W/m^2) substituting I_{sc} obtained by the solar simulator for I_L in equation (1) to translate the *I-V* curve to the fourth quadrant. The calculated degradation of power is relatively weakly dependent on the I_{sc} used for the translation, and this value may be fine-tuned to achieve better correspondence to the actual power degradation for the points that are tested with the solar simulator, such as at the end of the test or around the failure point of interest [9]. In this work, we test the utility of this technique to characterize the low-light performance of modules undergoing PID in chamber, simply using the initial I_{sc} of the module measured with a solar simulator at the low light levels of interest for the dark *I-V* curve translation factor I_L. In addition to the 1,000 W/m^2 level, we extend the analysis to determine the power performance at 200 W/m^2 and 600 W/m^2 within the dark environmental chamber, briefly interrupting the test and returning the chamber to 25°C for the measurement of the dark *I-V* curves and solar simulator testing at the various intensities for the comparisons. Considering that warranty failure is often defined to be a 20% relative drop in power, the analyses are carried out somewhat beyond, to about 30% relative degradation.

Results and Discussion

Examples of the dark and light (solar simulator-determined) *I-V* curves over the course of PID stress testing in the environmental chamber are given in Fig. 1. I_{sc} values are matched at each irradiance level because the dark *I-V* curves are translated by the I_{sc} determined at the beginning of the test. I_{sc} is seen in the figure to not degrade significantly even as fill factor and open circuit voltage (V_{oc}) degrade by PID. The dark and light *I-V* curves for a given module state are not coincident—they are displaced laterally as indicated by an arrow placed at the maximum power point for the case of the *I-V* curves measured at the start of the test with 1,000 W/m^2 irradiance. At this point in the dark *I-V* curve, the current is very small (recall, the curve is translated by I_{sc} in Fig. 1), so the series resistance term in equation (1) and power loss represented here in the dark *I-V* curve are very low. The voltage drop represented by the span of the arrow divided by the current at maximum power I_{mp}, $(V_{Light} - V_{dark})/I_{mp}$ typically represents the series resistance of a solar cell at P_{max} under illumination [12, 13]. For a given illumination condition during the course of PID, the effects of series resistance and the resulting curve offsets remain approximately constant and thus can be neglected in the analysis.

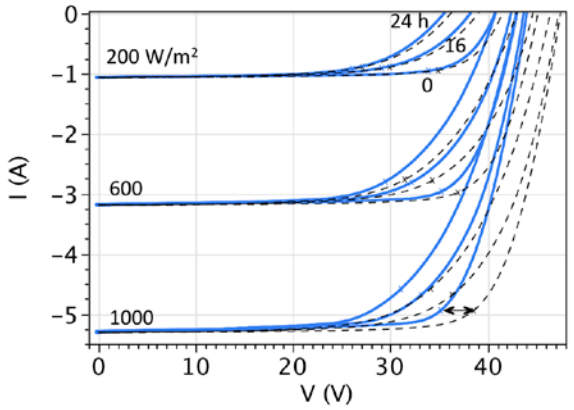

Figure 1. Light (solid) and fourth-quadrant-translated dark *I-V* curves (dashed) at three levels of illumination for the c-Si module undergoing potential induced degradation. The family of curves at a given intensity measured at 0 h, 16 h, and 24 h of stress (60°C 85% RH, –1,000 V) shows the reduction in fill factor and V_{oc} over the course of degradation. The double-tipped arrow indicates the difference in the dark and light (1,000 W/m^2 irradiance) *I-V* curves at the maximum power points at 0 h of stress.

The comparison between the solar simulator-determined power of the c-Si silicon modules (two replicas) and that determined from the dark *I-V* measurements is shown in Fig. 2, left. The dark *I-V* curves from which we estimate P_{max} at the various intensities (1,000 W/m^2, 600 W/m^2, or 200 W/m^2 irradiances) were translated by the I_{sc} values determined on the flash tester before stress testing at the corresponding irradiances. P_{max} determined from the dark *I-V* curves over the course of degradation is normalized to the initial power also obtained from the translated dark *I-V* curves (P_{max0}). The degradation in power determined by dark *I-V* curves corresponds very well to that measured with the solar simulator. It is seen that the dark *I-V* curves also accurately estimate the low-light performance of the modules degrading by PID.

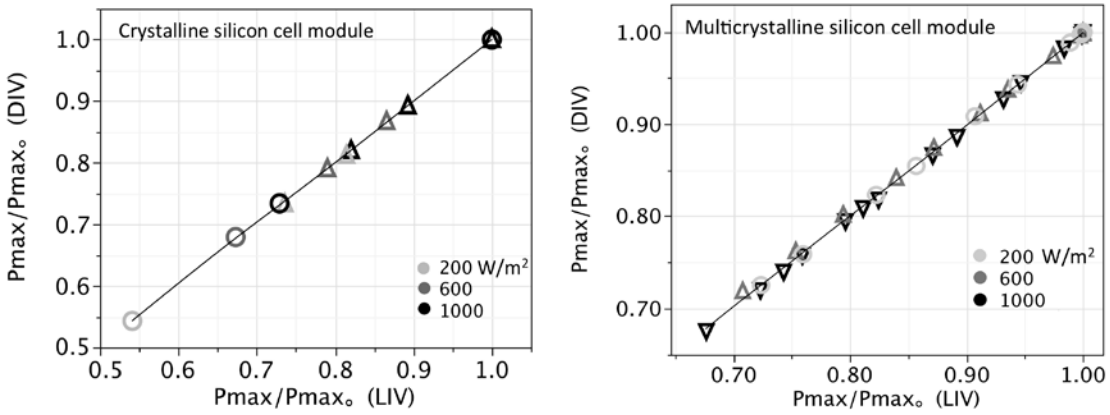

Figure 2. Correlation between module power normalized to the initial power (P_{max}/P_{max0}), determined from the 25°C dark *I-V* (DIV) curves translated to the fourth quadrant (i.e., superposition) and the solar simulator (LIV) for the c-Si module design, left, and the mc-Si module design, right (two replicas, as indicated by circles and triangles) over the course of PID at 60°C, 85% RH, and –1,000 V. The correlation is found to be excellent over the whole range of degradation examined for all indicated irradiances. The root mean square error for both lines of fit is 0.00.

Fig. 2, right, shows the correlation between the normalized power of the mc-Si modules obtained by dark *I-V* measurements to that obtained with the flash tester for the three different irradiance values. For the case of 1,000 W/m^2, it was found that the use of I_{sc} determined by the module tester as I_L gave satisfactory results (within 2% relative of the solar simulator results) for the range shown. Correlation could be improved when also considering greater extents of degradation (not shown in Fig. 2) by reducing the assumed I_L by 15% to 20%.

The PID versus time under stress in the environmental chamber (60°C, 85% RH) and –1,000 V bias of the mc-Si modules tested in this study is given in Fig. 3. Having established its utility, the dark *I-V* analysis is used here because a greater number of such curves were taken *in-situ* in the environmental chamber than those using the solar simulator. The two mc-Si modules are lumped together for line-of-fit purposes at each of the three irradiance levels. We previously found that the normalized power drop could be fit linearly for simplified statistical analysis and data visualization by transforming the time axis scale to the power of two. The data are formatted as such here. The analysis on the time axis scaled to the power of two is found to be relevant for fitting the data obtained here for all the examined irradiances. The fit to this function may be a useful parameter to further understand the degradation mechanism. The first data points taken

after 8 h of stress in the environmental chamber indicate possible degradation considering the 200 W/m^2 condition, but this is at most 1% relative loss from the pre-stress power level. After 16 h of stress, the modules clearly exhibit PID, and the extent of the degradation on the normalized power basis is differentiated by the irradiance level. For 5% relative degradation, a level commonly used as the failure point in many PV module test standards, the times are 13.6 h and 18.8 h for the 200 W/m^2 and 1,000 W/m^2 conditions, respectively, using the lines of fit drawn in Fig. 3. The failure when measured at the low light level occurs in 28% less time than that at full irradiance. This is comparable to the lesser time observed for 5% degradation at low intensity compared to that at one sun for modules undergoing PID outdoors; for example, 17%, 35%, and 42% less time [14].

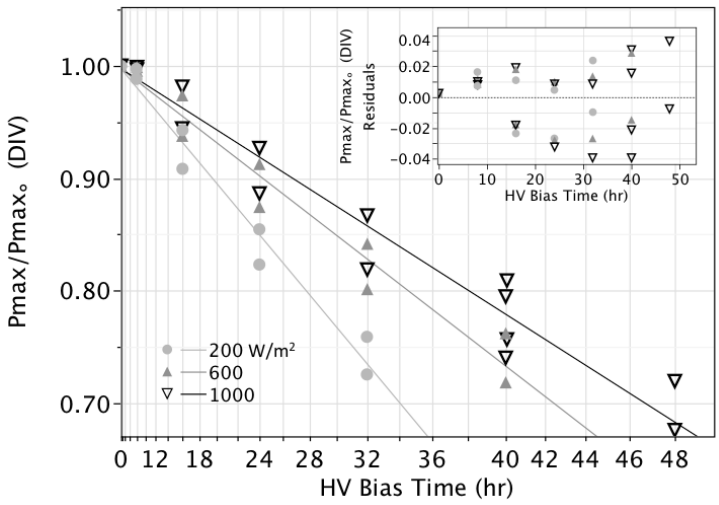

Figure 3. Normalized power of two mc-Si module replicas undergoing PID as a function of test irradiance (using the dark *I-V* curve analysis) and stress time, which is scaled to the power of two in the plot. Lines of fit are drawn for the degradation for the two modules (grouped), normalized to their power at the start of the test for each irradiance level. The deviations from the line of fit are given in the inset.

Summary and Conclusions

The principle of superposition using dark *I-V* curves was successfully applied to estimate the power of modules undergoing PID under low-light conditions in an environmental chamber. The extent of PID determined from the dark *I-V* measurement and that indicated by a solar simulator showed excellent correspondence up to the 30% relative degradation that was examined in this study. Failure at the 5% relative degradation level measured under low irradiance (200 W/m^2) occurs in 28% less time than that at full (1,000 W/m^2) irradiance for the conventional c-Si modules undergoing PID in an environmental chamber with conditions of 60°C, 85% RH, and –1,000 V system bias. Modules undergoing PID can therefore be well characterized in the chamber, facilitating statistical analyses and lifetime forecasting, inclusive of low-light performance.

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