# Final Technical Report for DOE Advanced Detector Research Grant DE-SC0007054 UTA:26-0801-36
# Electronics for a Picosecond Time-of-Flight Measurement
Awarded to University of Texas, Arlington Professor Andrew Brandt (the PI and project director)
and to Stony Brook Professor Michael Rijssenbeek (co-PI)

## Executive Summary

Time-of-flight (TOF) detectors have historically been used as part of the particle identification capability of multi-purpose particle physics detectors. Such detectors measure the particle flight time with a time resolution on the 100 ps scale, or in other words, an uncertainty of one ten billionth of a second. This accurate time measurement, combined with a momentum measurement in a magnetic field, is often sufficient to determine the particle's mass, and thus its identity. Another use of TOFs is to measure the vertex position of an interaction with very far forward tracks on both sides of the collision. If the vertex is displaced to one side, the time will be shorter in that direction and longer in the opposite direction. For the LHC and other future experiments, an order of magnitude improvement to the 10 ps scale is desired, as well as high rate capability on the 10 MHz scale, and radiation tolerance. The ability to accurately measure the flight time depends on three key elements: the radiator, the photo-sensor, and the electronics. Our attempts to solve this problem utilizes quartz bars to generate light (when energetic particles pass through the bars they radiate a prompt so-called "Cherenkov" radiation), and special photomultiplier tubes (micro-channel plate PMTs) that convert the light to an electrical signal more quickly and with much better resolution than traditional methods, typically in the 30-40 ps range. Multiple measurements could then reduce the overall uncertainty by another factor of three or so, bringing the resolution to 10 ps, which allows position uncertainties on the mm scale instead of the cm scale. The ability to maintain this superior resolution through the full readout chain from the output pulse of the photo-sensor to the digitized signal recorded in the data stream of the detector requires the development of suitable fast electronics, and that has been the focus of this proposal.

The goal of this R&D effort was to not only develop and demonstrate a full electronics chain, but to do this cost effectively and with a modular approach such that the whole chain or components could be easily adapted for use in particle physics experiments or in other areas where precise timing is required, such as medical and homeland security devices. In this successfully executed proposal, we have developed from scratch or improved upon existing designs resulting in a full electronics chain for a time-of-flight particle detector with an extremely precise resolution of 20 ps/channel.

4. ***Comparison of the goals and objectives of the project with actual accomplishments.*** The main goal of the ADR was to develop all the components of a full electronics readout system with an intrinsic time resolution of 20 ps per channel or better. This primary goal was accomplished and demonstrated in bench tests and test beam. The secondary goal, to develop the electronics as a series of "building blocks" that can be used as is, or can be individually adapted to a particular application was incorporated into the design of the new elements. A brief discussion of the main objectives and their level of completion are given in this section, with more details in the following section.

**Objective 1:** Develop a radiation-tolerant, 8-channel pre-amplifier board, including protection of the amplifiers against large input pulses. This amplifier development required a few iterations, but was ultimately completed. A stable low noise amplifier is a critical part of the system, and our new amplifier meets all the design requirements including radiation tolerance.

**Objective 2:** Replace the existing CFD board with an upgraded module which also outputs a low-resolution ADC for monitoring the gain of the photo-sensors. Rather than build in ADC functionality, we found a simpler approach using the time over threshold function of the HPTDC chip, which will provide the same basic functionality when completed. This information can be used for monitoring the PMT gain, rejecting background events with large multiplicity, and making corrections for residual time walk effects. Simulation and design of a new prototype CFD daughter card has been completed, and the prototype phase is about to begin.

**Objective 3:** Develop an ultra-stable reference clock to precisely synchronize several time-of-flight detectors with a jitter less than 5 ps uncertainty. We achieved this objective, developing a new synchronization circuit with about 2ps jitter.

**Objective 4:** Finally, we are developing a board capable of generating a level-1 trigger based on the CFD outputs, and provide a scaled reference clock signal to the existing HPTDC board. This trigger board has evolved since our original plans, and is in the prototyping phase.

***5. Summary of project activities including original hypotheses, analysis, problems encountered, and an assessment of their impact on project results.***

# 1 Introduction

Time-of-flight (TOF) detectors have historically been used as part of the particle identification capability of multi-purpose particle physics detectors. Such detectors measure the particle flight time with a time resolution on the 100 ps scale. For the LHC and other future experiments, an order of magnitude improvement to the 10 ps scale is desired, as well as high rate capability on the 10 MHz scale, and radiation tolerance. The ability to accurately measure the flight time depends on three key elements: the radiator, the photo-sensor, and the electronics. Our attempts to solve this problem utilizes quartz bars to generate light from Cherenkov radiation, and MCP-PMTs (micro-channel plate photomultiplier tubes) with transit time spread (single photoelectron jitter) of 30–40 ps. For a typical radiator/photo-detector the photon statistics are limited. Thus, the signal amplitude can fluctuate significantly from one event to another resulting in large amplitude-dependent time shifts (known as time-slewing or time-walk) if a simple fixed threshold discriminator is used, precluding accurate timing. Consequently, there are two basic options given a detector with limited photo statistics: 1) employ a constant-fraction discriminator (CFD) followed by a time to digital converter (TDC) or 2) determine the time by sampling, storing, and analyzing the full signal shape. While this is a promising approach for lower rate applications, it is much more challenging for high flux use. The approach we have chosen and successfully demonstrated is low-noise amplification followed by constant-fraction discrimination (CFD) and high-precision time digitization (HPTDC) and readout, see Fig. 1 where the various components are depicted.

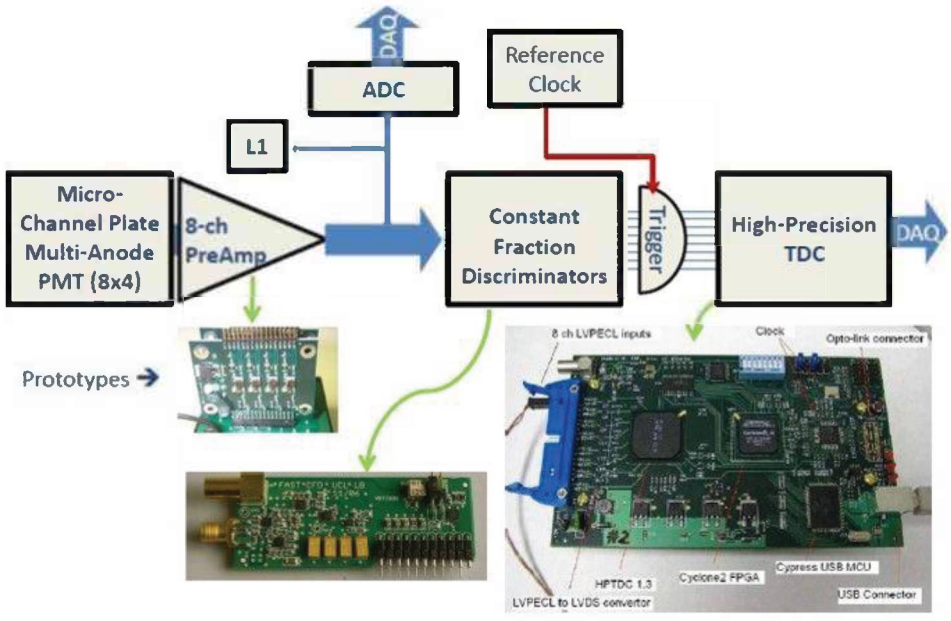


Figure 1: A functional diagram of the components of the fast timing electronics chain described in the text, along with photographs of some of the key elements.

Several types of Cerenkov photon detectors are currently available that deliver the required timing resolution including MCP-PMTs and avalanche photo-diode arrays, also known as Silicon photomultipliers (SiPMs). These detectors feature rise times of 100 to 400 ps and transit time jitter

of better than 30 ps when combined with a radiator that produces O(10) detected photoelectrons. In this ADR we do not address the radiators or photo-detectors, but focus on simulating, developing, and demonstrating a full electronics chain with a resolution of less than 20 ps/channel, consistent with our overall system goal of 10 ps for the whole detector.

# 2 University of Texas at Arlington Activities

This fast timing electronics development project was led by University of Texas, Arlington (UTA) Professor Andrew Brandt. UTA's primary deliverable for this proposal was the stabilized low jitter reference clock, used to tie together measurements hundreds of meters apart, as required for the LHC forward proton use case of the fast timing electronics. UTA was also responsible for testing individual components and the full system at the Picosecond Test Facility. This laser lab, established with previous ADR funds, employs a pulsed picosecond laser (405 nm and 632 nm) to simulate the Cherenkov radiation produced when a of a fast particle through a quartz bar. This facility provides a tremendous research opportunity for undergraduate researchers that perform most of the tests. In addition, Brandt was in charge of planning and leading the execution of two test beam runs that took place during the project period, and also helped plan and execute the radiation testing of various components.

## 2.1 Reference Clock Development

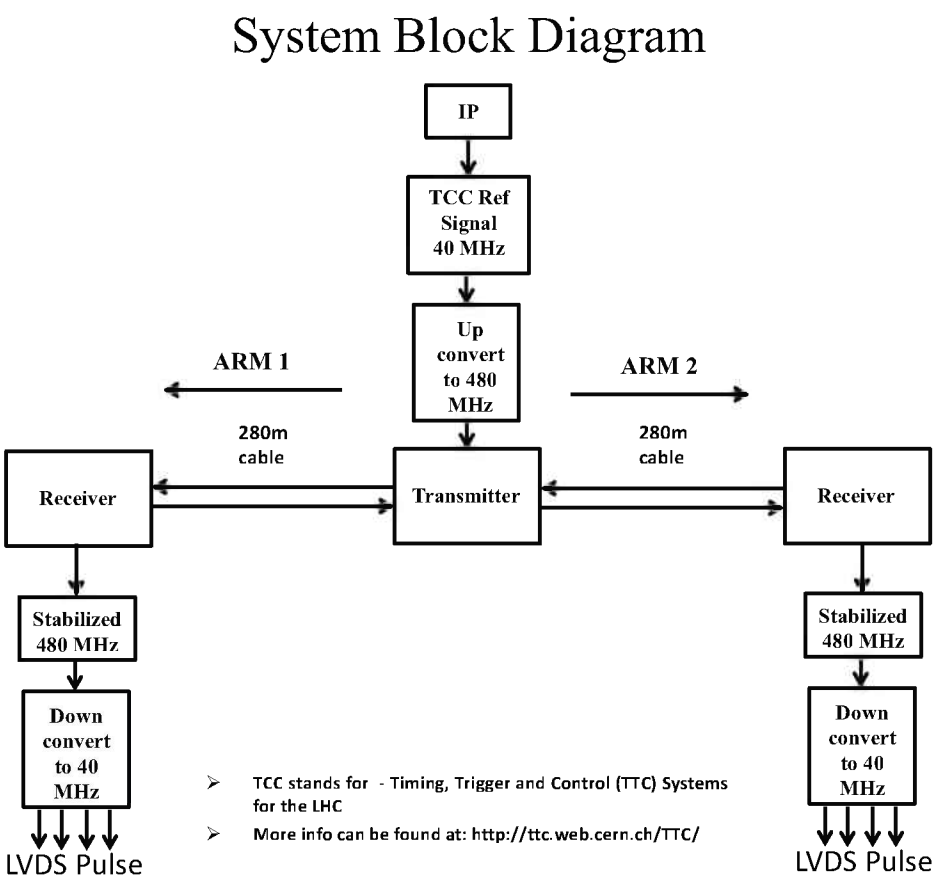


Figure 2: Overview of the reference timing system.

A major component of any time-of-flight system using two widely separated detector arms is a low jitter reference clock. The physics topology being studied has outgoing protons in both

directions with an associated central system, and is prone to pile-up background where the protons and central system originate from different collisions in the same bunch crossing. The time difference of the protons can be used to measure a vertex position and discard events where the vertex does not match the tracking vertex of the central system. The low jitter clock is necessary, since the quantity measured is the time with respect to the clock on either side. If the common clock signal (reference clock) does not have low jitter, the uncertainty could be dominated by the clock jitter, and the detector would be ineffective. The block diagram of the system to achieve low jitter (less than 5 psec), stabilized output clock signal is shown in Fig.2.

The approach we pursued was to follow as closely as possible the SLAC design and develop additional components as necessary. In this design a voltage controlled oscillator (VCO) on the receiver board (Fig.3(a)) launches a signal down the cable from the remote location of the time of flight detector (in the tunnel near the proton or other near beam detector) to the interaction point (IP), where the transmitter board (Fig. 3(b)) reflects it back, starting an iterative feedback process. After the first return trip to the transmitter board the signal is sampled with a directional coupler where it is compared in the mixer with the 400 MHz Master Reference, provided in this example from the LHC RF signal. The result is a DC voltage level that is fed back to the VCO to maintain synchronization. Changes in the cable's electrical length cancel when the original and returned signal are added.

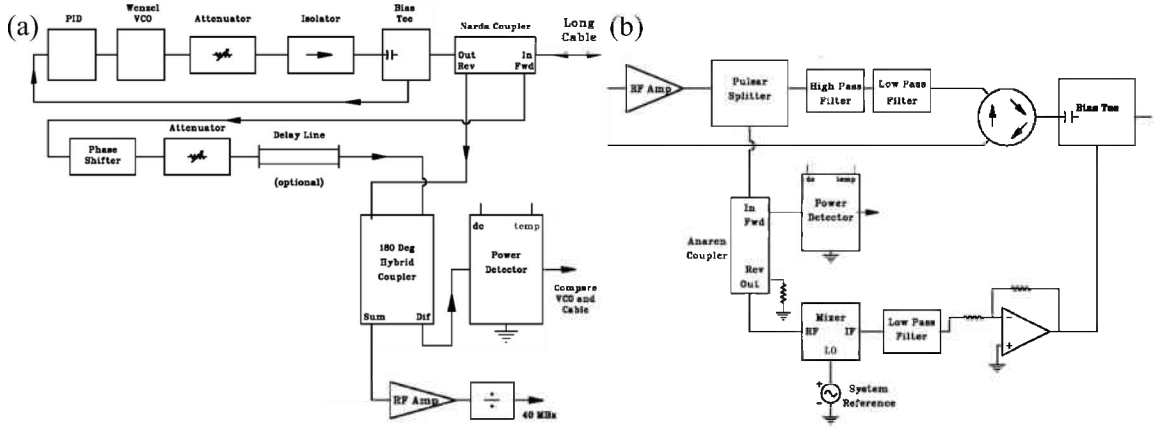


Figure 3: A functional diagram of (a) the receiver board (b) of the transmitter board.

The LHC clock used by the experiments is 40 MHz compared to the SLAC 476 MHz. Since adapting the SLAC design to 40 MHz was impractical if not impossible, due to frequency limitations on some of the components, a new approach was necessary: first we multiply the signal frequency by 12, then we stabilize the resulting 480 MHz signal, and finally, we divide the stabilized signal by 12. This required the development of divider and multiplier boards in addition to the stabilization circuit (phase lock loop). The main activities of the clock development group are listed below:

- Draw the complete circuit diagrams of the receiver and transmitter boxes based on the SLAC design.
- Simulate the phase locked loop circuit.
- Order the components.
- Construct and debug the receiver and transmitter boards.
- Demonstrate the phase locked loop performance.

- Develop the circuit boards for multiplying and dividing the input signal by a factor 12.
- Developed several other PCB boards for voltage control and logic inputs etc.
- Design a circuit to convert the sine wave output to a pulsed output at 40 MHz.

Many tests were performed and many problems debugged on the way to developing the working clock circuit. To verify the performance, a 40 MHz signal from the signal generator was plugged into a fast oscilloscope, yielding an initial jitter of 120 ps as shown in Fig. 4(a). The signal generator was then plugged into the receiver/transmitter circuit where it was multiplied by 12 and passed through the phase lock loop. The jitter on the 480 MHz stabilized signal prior to the divider was measured to be 8 ps. Finally the divider board was added to the circuit, producing the desired 40 MHz clock signal shown in Fig. 4(b), with a jitter of about 2 ps. Figure 4(c) shows unwanted harmonics that necessitated the construction of a band pass filter. The main challenges of the project was that there were not sufficient funds to support the engineering student for the full duration of the project, so he was only part-time, and in addition had a steep learning curve, leading to schedule delays. Part of the reason for the no-cost extension was to allow the student to complete the project, and the final result was excellent.

While an experiment would need a two-arm clock, one arm is good enough for demonstration purposes, so the remaining funds that had been earmarked towards a second arm, were used to partially fund a scope upgrade, which was essential to some of the testing portion of the UTA responsibilities. The testing is discussed in a later section after the fast electronics components have been presented.

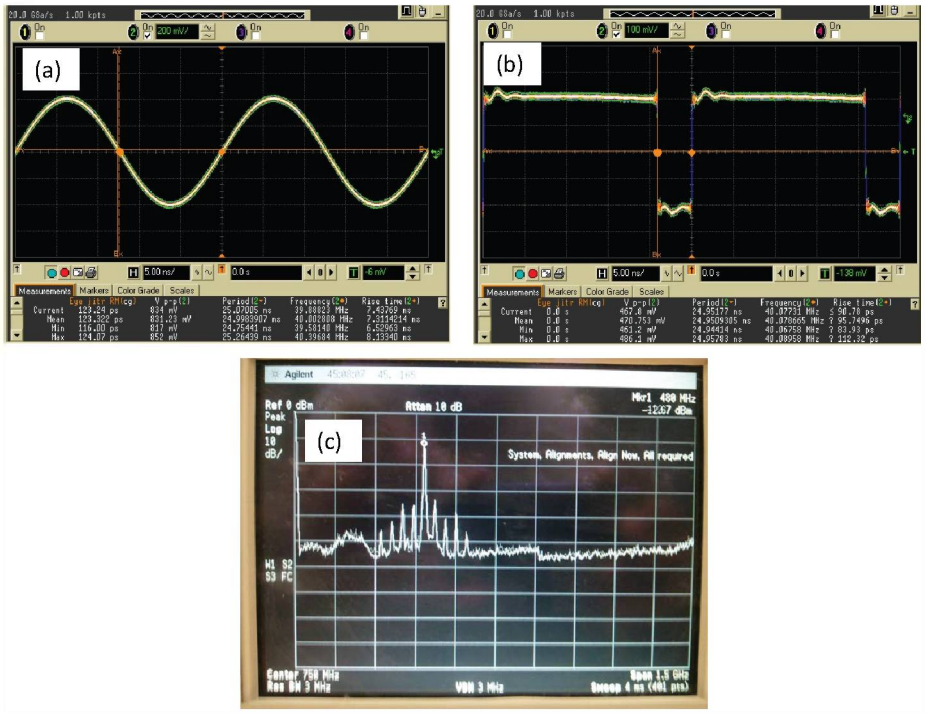


Figure 4: (a) jitter of the 40 MHz input signal (b) the output stabilized 40 MHz signal (c) harmonics resulting from the multiplier circuit

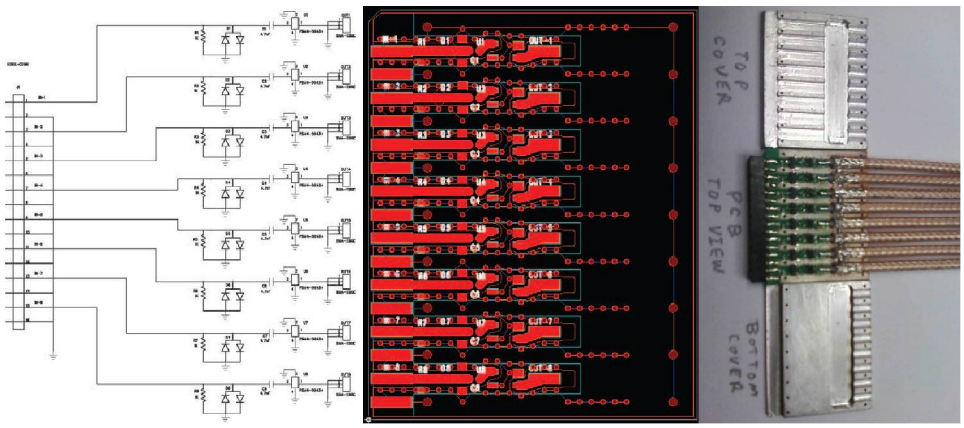


Figure 5: The schematic diagram, layout, and photo of the low noise pre-amplifier, to be located on the photodetector base in the secondary vacuum.

# 3 Stony Brook University Activities

Stony Brook had responsibility for the development of the Picosecond Time-of-Flight electronics. The goal of the program supported by this grant was to develop 8-channel fast timing modules that perform the following functions:

1. Low-noise preamplification of 40 dB, with programmable attenuation of up to 20 dB for the purpose of gain equalization.
2. Majority trigger on groups of 8 channels in order to provide early and fast trigger information to a central trigger system.
3. Discrimination and digitization of the analog signals based on a constant-fraction discriminator and the fast digitizer chip HPTDC developed by CERN.
4. Low-resolution fast pulse charge digitization in order to provide the possibility for off-line correction of residual time slewing.

## 3.1 Preamplifiers

The PMT is used at a low gain of about $5 \times 10^4$ to maximize its lifetime in the high-rate LHC environment close to the circulating beam. The typical PMT output signal at this gain is about 8 mV for 10 photoelectrons. The version of CFD performs best for signals in the range from 250 - 1200 mV (a new design is in progress with a further improvement anticipated in dynamic range).

In order to match the CFD dynamic range, and to provide for gain variations as a function of PMT pixel and ageing, the pre-amplification is done in two 20 dB stages. The first stage PA-a is located directly on the base of the PMT. The 8-channel preamplifier PCB is based on the PSA4-5043+ low-noise (NF=0.7 dB) InGaP E-PHEMT MMIC gain block (gain 18.6 dB at 1 GHz) from MiniCircuits.com, see Fig. 5. The PA-a has been tested under power and demonstrated to be radiation tolerant to at least 9 kGy at a February 2014 irradiation run at Los Alamos National Lab with 800 MeV protons, $2.2 \times 10^{13}$ p/cm$^2$); this corresponds to the dose expected at the preamplifier location for 300 fb$^{-1}$, (three years of data taking at a luminosity of $10^{34}$ cm$^{-2}$s$^{-1}$).

The first preamplifier stage is connected by coaxial cable to the second pre-amplification stage (PA-b) located at floor level below the detector, where the high-energy proton flux is expected to be reduced by a factor of 20 (the low energy neutron flux is a factor 10 lower there).

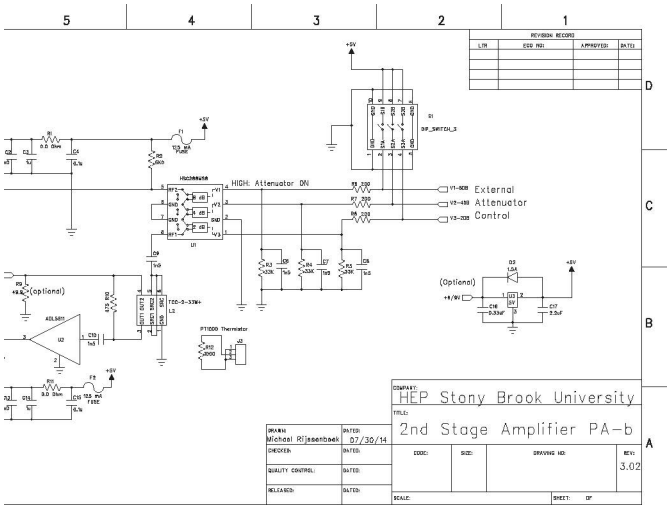


Figure 6: The schematic diagram of the new second-stage variable-gain amplifier PA-b, to be located below the detector at floor level.

The PA-b provides DC power (5 V) to the PA-a via the coaxial connection. The PA-b further includes (in order): a programmable 3-bit attenuator (Hittite HMC288MS8 2 dB LSB GaAs MMIC, range 1 dB - 15 dB ), a 2 Way-$0^o$ splitter (MiniCircuits TCP-2-33W+, $-4$ dB insertion loss) providing a trigger pick-off, and a ADL5611 gain block (Analog Devices, gain 22(20) dB at 1(4) GHz), see Fig. 6. The PA-b has successfully survived the same irradiation runs and doses as PA-a.

### 3.2 Trigger

A trigger board has been designed and will be produced in the near future. The design is based on the 8-channel GaAs Discriminator MMIC 'NINO' (developed and produced by CERN, see http://knowledgetransfer.web.cern.ch/technology-transfer/external-partners/nino), followed by programmable majority circuitry to form a 'N out of M' type trigger combination on two LVPECL outputs. The option to include a (properly timed) bunch crossing gate from the Reference clock (LVPECL) is implemented. The PCB has been simulated and laid out, but not yet produced.

The trigger signals from several adjacent quartz bar sequences are combined into a bit stream and sent over fast air-core coax cables to the ATLAS Central Trigger Processor. The trigger information from the two AFP arms can be used for a simple coincidence trigger or a more sophisticated configurable proton-proton 'missing mass' trigger, either of which could be combined with various central ATLAS trigger terms.

### 3.3 Constant Fraction Discriminator

The Constant Fraction Discriminator (CFD) principle has long be used to correct for time walk in cases where the signal fluctuates in amplitude but is constant in shape. The AFP design was initially developed for FP420 by Luc Bonnet of the Université Catholique de Louvain, and was

further refined for AFP by the HEP group (J. Pinfold, S-L. Liu) at the University of Alberta at Edmonton (Alberta). The measured residual time-walk is a few ps or less over the range 250 - 1200 mV, and even for lower values is not the dominant component of the timing resolution. The design has been revisited to obtain a larger dynamic range and to implement a time-over-threshold functionality, which will allow off-line timing corrections if so required. Moreover, the new CFD design includes an optional bunch crossing gate to reduce output rates/input rates to the HPTDC.

Each single CFD channel is implemented on a small $28 \times 70$ mm$^2$ daughter board, with RF I/O connectors for signal in and signal NIM out, and differential LVPECL outputs. A CFD NIM module has a simple motherboard which filters and regulates the NIM crate low voltage and provides the appropriate low voltage to 8 of these CFD channels.

### 3.4 High Precision Time Digitizer

The High Precision Time Digitizer board, HPTDC, was developed by Alberta. The 12-channel board uses 4 HPTDC ASICs developed and produced by CERN in 0.25 $\mu$m CMOS technology (HPTDC, J. Christiansen et al., http://tdc.web.cern.ch/tdc/hptdc/hptdc.htm). The four ASICs are controlled by an on-board FPGA which also handles the flow of data and controls. This and previous versions of the HPTDC board have been used successfully at various beam tests.

The intrinsic resolution of the current HPTDC is 16 ps, which is a significant contributor to the per-channel resolution. However, new HPTDC ASIC development with smaller feature size are ongoing at CERN and may lead to significant improvements in the near future. Note that the 16 ps resolution of the HPTDC is per channel and that the contribution for a system of four quartz bars in sequence would only be 8 ps.

The radiation tolerance of the HPTDC is not guaranteed. The HPTDC ASIC is expected to be radiation tolerant to a degree sufficient for it to be located on the tunnel floor, near the detectors. The FPGA firmware must be re-designed to provide the appropriate checking of HPTDC registers for upsets. Moreover, the FPGA itself has to be radiation tolerant, which can be done by choosing an expensive radiation-hard version, or by using a fuse-programmable part. Alternatively, the FPGA can be programmed to do self-checking and organized with majority decisions in critical paths. Studies of the latter choice are in progress.

## 4 Testing

A major part of this R&D proposal was various levels of testing of the components, individually and in system tests. Except for the initial in situ testing of the amplifiers at Stony Brook, the testing was coordinated and carried out primarily with UTA personnel under the direction of Brandt, either at the Picosecond Test Facility at UTA, or at test beam. UTA students also helped carry out the irradiation of components described earlier.

Several iterations of the fast amplifier were designed, simulated, built and constructed at Stony Brook. Each iteration was first tested at Stony Brook with a fast pulse generator, and then sent to UTA for detailed measurements using a blue (405 nm) pulsed picosecond laser to simulate the Cherenkov radiation, and a microchannel plate PMT to produce a realistic output pulse. A 6 GHz 20 Gs/s LeCroy Oscilloscope was used for data taking and some of the analysis.

Measurements at UTA including details of the input and output signals, gain, pulse shape, etc. were fed back to Stony Brook, resulting in new improved versions, which were then tested at UTA and then in test beam. Our analysis from previous test beam runs showed that it was important to protect the amps from big pulses with a diode, and that variable attenuation would be very useful in maintaining the timing performance of the system, by offsetting the decreased pulse height as the PMT aged by decreasing the attenuation, which could keep the pulse height in the best performing region of the CFD.

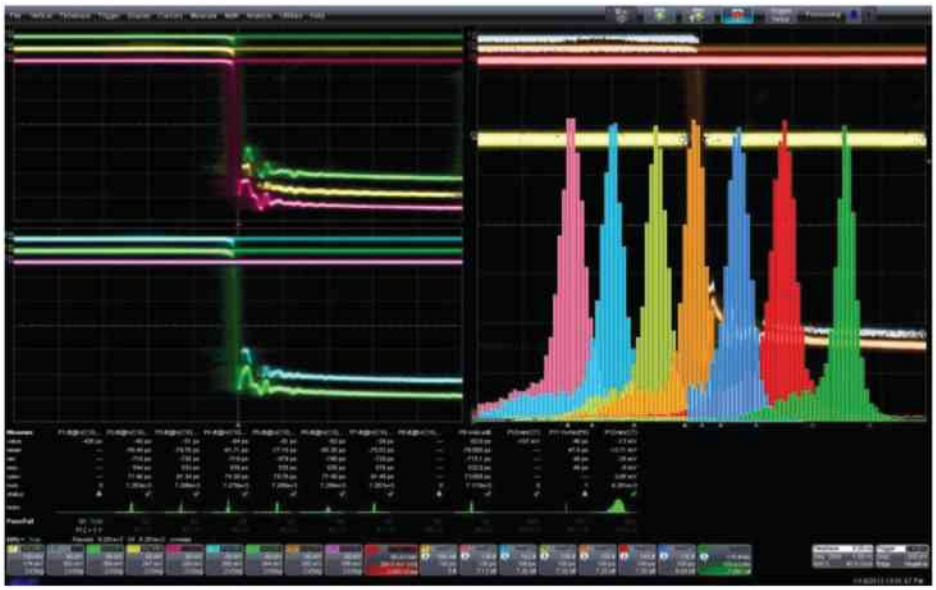

Figure 7: A screen capture of the Teldyne-Lecroy 9Zi oscilloscope after a test beam run in which the timing of a six quartz bar detector is measured. The first six peaks are the time of each channel, with respect to a reference SiPM, and the 7th is the sum of the six bars relative to the SiPM.

When this proposal was submitted, the single channel resolution of the timing detector had been measured to be 34 ps, of which about 28 ps was attributed to the PMT/amp/CFD part of the path and 20 ps to the HPTDC. For the 2012 Fermilab test beam, a new light tight box for testing the system was constructed at UTA to house the detector, MCP-PMT, prototype amplifiers, and SiPMs for triggering and reference timing (since the beam intensity is low, they could be placed in the beam with a quartz bar parallel to the beam, generating enough light to give 10 ps for a single channel). Figure 7 shows an online measurement of the time of the track using a Labmaster 9Zi $500,000 20 channel scope, loaned to us by Teldyne-LeCroy for the test beam; the histograms show the measured time of each of the six bars in line relative to the time of the track passing through the SiPM, and the measurement the six-bar average time with the 7th measurement taken as the average of the six for events with all bars having a signal. The final histogram has a "full-width at half max" (FWHM) of 47 ps, which gives a standard deviation of 20 ps, implying 14-15 ps for the detector/amp/CFD combination. The tail events are due to saturated pulses either from spray or from fluctuations. The improved dynamic range of the latest version of the amp would be useful to remove these events. Figure 8(a) shows a slightly more sophisticated offline analysis, of the 6 bar average time from the CFD outputs with respect to the SiPM, which is also measured using the CFD. These results are consistent with the online measurement, showing a mean of 20 ps, when combined with other constraints, this gives the six bar measurement of 14 ps. The only significant change was the improved amplifier board over the standard macroscopic mini-circuits amplifiers. Figure 8(b) is the same measurement after the HPTDC. The visible degradation in resolution is almost entirely due to the SiPM HPTDC, since the effect of the HPTDC on the measurement of the quartz bars is divided by six, but the SiPM HPTDC enters in quadrature with the SiPM resolution. The SiPM resolution is any case irrelevant since the reference clock will be used in its place. Clearly the effect of the electronics on the six channel measurement is well under control. A further test beam at CERN using a faster MCP-PMT and the final amplifier achieved 20 ps resolution after

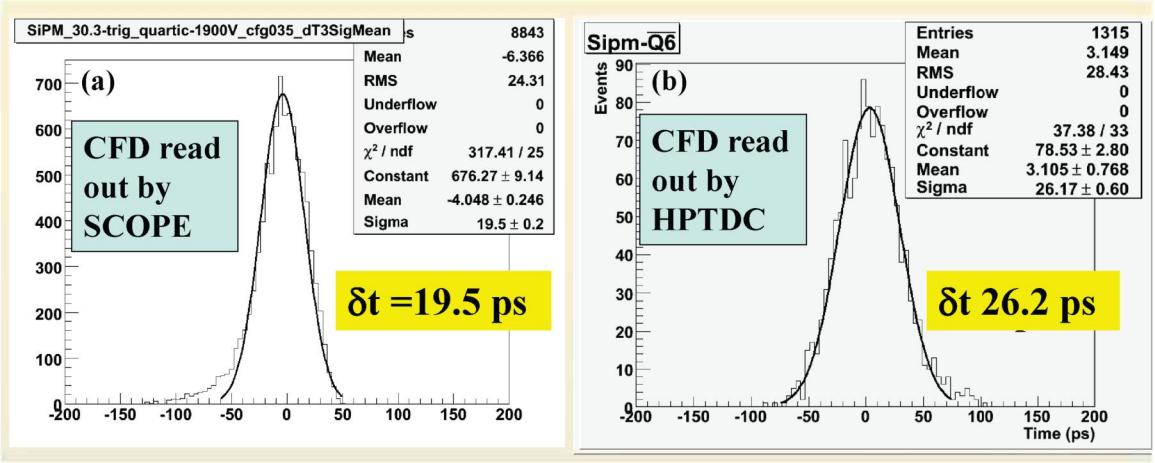


Figure 8: The time difference between the average time of a six bar detector and a SiPM as measured with (a) the Labmaster 9Zi oscilloscope operating on the CFD output pulse (b) the HPTDC operating on the CFD output pulse.

the CFD on a single bar, implying a four bar detector could reach the desired 10 ps resolution.

## 5 Problems Encountered

The main problems were not technical in nature, but resulted from manpower shortage. This was partly a budgetary issue, due to the limited funding of the ADR program, the potential grant size (averaging less than $100,000 per year a maximum of two years). This did not allow for professional engineering support. By necessity, we relied heavily on undergraduate student labor, and to a lesser extent graduate students, while no faculty members received compensation for work on this project, limiting their involvement. One of the key personnel, a senior technician at Stony Brook had a sudden debilitating illness, and was unable to continue part way through the first year. Obtaining a replacement took time, and the new technician did not have as much relevant experience. This was one of the main drivers of a no-cost extension, but there are of course no extra funds associated with the extension, so the third year was less productive than the first two. One of the two consulting UTA engineering professors retired, leading to some delays in the UTA clock studies, which in turn resulted in a lower rate of productivity as the funds earmarked for the student were depleted prior to completion of the project. Additional factors affecting the completion of the project included co-PI Michael Rijssenbeek being appointed Technical Coordinator of the ATLAS Forward Proton project, a very positive development on the whole, but his subsequent relocation to CERN understandably resulted in a decrease in the rate of progress of the new technician. Finally, in spring 2013, U.S. ATLAS support for the AFP project, was terminated despite the excellent performance of the primary U.S. contribution (the timing system). Although the timing R&D in this proposal is generic, the cancelation of the U.S. involvement in the main use case had many negative effects on the principals and the rate of progress of the project–nevertheless, the principal goals of the project were accomplished.

6. ***Identify products developed under the award and technology transfer activities.***

a)Numerous conference presentations have been made by Brandt, Pinfold, Rijssenbeek, and others about this work at fast timing workshops over the last three years. Most recently all three of us gave talks on various aspects of the results at the Clermont-Ferand timing workshop. List of publications and papers in progress:

- "The Workshop on Picosecond Photon Sensors for Physics and Medical Applications," March 12-14, 2014, with Michael Rijssenbeek providing a write-up for the proceedings.
- Report of Forward Physics Working Group at the LCPP (LHC Physics Center at CERN
- "ATLAS Letter of Intent for Phase-I Upgrade," CERN-LHCC-2011-012, LHCC-I-020.
- NIM papers in progress on the CFD and HPTDC.
- J Inst. papers in progress on tests performed at the Picosecond Test Facility
- J. Inst, paper in progress on test beam results

b) No web site dedicated to this work directly
c) Sharing the results of this work have helped established cooperative relationships within ATLAS, with CMS-Totem, and with Photonis.
d) Many techniques have been developed for fast timing electronics necessitated by the resolution goals.
e)Each component of the electronics chain could in principle be a marketable product. We have worked hard on controlling the costs and could potentially produce some of these items for less than the current price/channel of CAEN or Ortec. The IP is somewhat complicated, since many institutions have contributed value, and the size of the market is not clear. It would require substantial work and additional funding to get from our current position to one where we were selling these devices.